BLOCK II SSMEC TRAINING MANUAL

SPACE SHUTTLE MAIN ENGINE BLOCK II CONTROLLER TRAINING MANUAL

1.0 Introduction

This Manual is designed to serve as a training manual for people working on the Space Shuttle Main Engine Controller (SSMEC) Block II.

1.1 Purpose

The intent of this Manual is to provide a broad base understanding of the Space Shuttle Main Engine (SSME) and Space Shuttle Main Engine Controller. The manual will also pull together and define the reference material required for a more in-depth study of the SSMEC.

1.2 Scope

This Manual focused primarily on the SSMEC, the SSMEC Software and the SSMEC test equipment. The software and test equipment will further narrow down to concentrate on the Honeywell designed test software and factory test equipment. Flight software and ground check out will be covered but not in great detail.

1.3 Shuttle Main Engine Description

1.3.1 General Description

The SSMEC is reusable, variable thrust, high performance liquid propellent rocket. It is the most advanced rocket engine in use by the U.S.A. today. Each engine provides a phenomenol amount of thrust with relation to its size and weight of fuel and oxidizer consumed.

The SSME is the first rocket engine with Closed Loop Digital Control. This digital control allows the SSME to accept commands from the orbiter spacecraft and perform various engine function all the way from preflight checkout to post flight shutdown in addition to thrust variation during the flight.

As a digitally controlled pump fed engine the SSME represents a major advance in rocket engine technology. The SSME burns hydrogen, as fuel, with oxygen as oxidizer. These two propellants have the highest energy to weight ratio of any propellants and are non polluting in their combustion. The by-product of their combustion is heat and water in the form of steam.

The liquid hydrogen (LH2) in addition to being the fuel for the engine is also used as the cooling medium.

Liquid hydrogen is pumped thru cooling tubes and cavities to cool the manifold, main chamber and nozzle from temperatures that can reach over 2000°R hot gases we also have the cryogenic liquid oxygen (162.4°R, -397°F) and liquid hydrogen (36.3°R, -423.4°F). Not only do these temperature extremes exist within an engine they can exist within a single turbo-pump.

The turbine portion of the turbo-pump is driven by the hot gases while the pump section is pumping a cryogenic fluid. Generating a design that could withstand these temperatures and the temperature swings from room temperature to these extremes every time the engine is fired was a major accomplishment. The SSME was designed for 7.5 hours of accumulated firing time which is equivalent to 55 missions.

The SSMEC is not the first liquid hydrogen (LH2) and liquid oxygen (LOX) engine. It is however, the first to produce main chamber pressures in the 3000 pounds per square inch range. This is accomplished by pushing huge quantities of LH2 and LOX into the main chamber with high pressure pumps.

The SSME is the first LOX and LH2 engine to use a staged, or tandem, combustion cycle. Most of the fuel is preburned in two preburner (PB's) chambers. The PB exhaust gases are used as fuel for the main combustion chamber (MCC) and to provide the energy to drive the turbine stages of two high pressure turbo-pumps.

The High Pressure Fuel Turbo Pump Turbine (HPFT) extracts energy from one preburner and the High Pressure Oxidizer Turbo-pump Turbine (HPOT) extracts energy from the other preburner.

The exhaust gases from the pre-burner chambers are hydrogen saturated, super heated steam. This pre-heated fuel is combined with additional vaporized hydrogen and large quantities of oxygen to produce the high intensity burn of the main combustion chamber (MCC).

The concept of a two stage combustion cycle required the use of high speed and high capacity turbine driven pumps. It is the ability of these high speed turbopumps to deliver massive quantities of propellants to the three combustion chambers, that gives this relatively small engine such a powerful punch. At rated power level, each of three 7000 pound "mighty mites" produces 375,000 pounds of push at sea level and 470,000 pounds in the vacuum of space.

The structural backbone of the SSME is the hot gas manifold (HGM). It supports nearly all other engine components. The dome/injector mounts in the center of the HGM. An engine support bearing, in turn, mounts to the top of the dome/injector. It is through this attach point that the engine thrust vector pushes the orbitor.

The HGM carries hot exhaust gases from two preburner chambers to the main combustion chamber. It also contains cooling cavities through which the LH2 circulates.

Two other engine components, the Low Pressure Fuel Turbo Pump (LPFT) and Low Pressure Oxidizer Turbo Pump (LPOT) are supported by orbiter structure and supply propellants, through ducts which have flexible bellows joints. This allows movement, or gimbaling, of the engine to steer the entire launch vehicle by changing the direction of the thrust vector during ascent phase.

Figure 1 -1 shows the major components that make up the SSME and Figure 1- 2.1 through 1 - 2.5 define the liquid/ gas flow paths.

1.3.1.1 Turbo Pumps

The SSME has four turbine driven pumps, a tandem pair for fuel delivery and a tandem pair for oxidizer delivery. The first stage of each pair is a low pressure turbo pump. The Low Pressure Fuel Turbo Pump (LPFT) and the Low Pressure Oxidizer Turbo Pump (LPOT) are connected to the vehicle propellant ducting and supported by orbiter structure. The turbine stages of these are initially spun by the falling propellants that pass these turbine stages on their way to the combustion chambers.

The second stage of each pair are the high pressure turbopumps. The HPFT and HPOT are the real muscle of the SSME. They are masterpieces of rotating machinery and have the capacity to drain the average size backyard swimming pool in a matter of seconds. The following table 1-1 is a comparison of performance parameters for all four turbo pumps. The reader should take note that the HPFT operates at approximately 35,000 RPM at Rated Power Level (RPL) and must go as high as 37,000 RPM at Full Power Level (FPL). Where RPL is the engines rated thrust and FPL is 109% of the rated thrust.

The HPFT and the HPOT are centrifugal flow pumps, shaft driven by turbine stages at the tops of each turbopump. The turbine stages of each are surrounded by the preburner liners. This portion of the turbopumps is flange mounted to the bottom sides of either end of the hot gas manifold (HGM). The preburners are installed through the top of the HGM ends and welded in place.

SSME MAJOR COMPONENTS

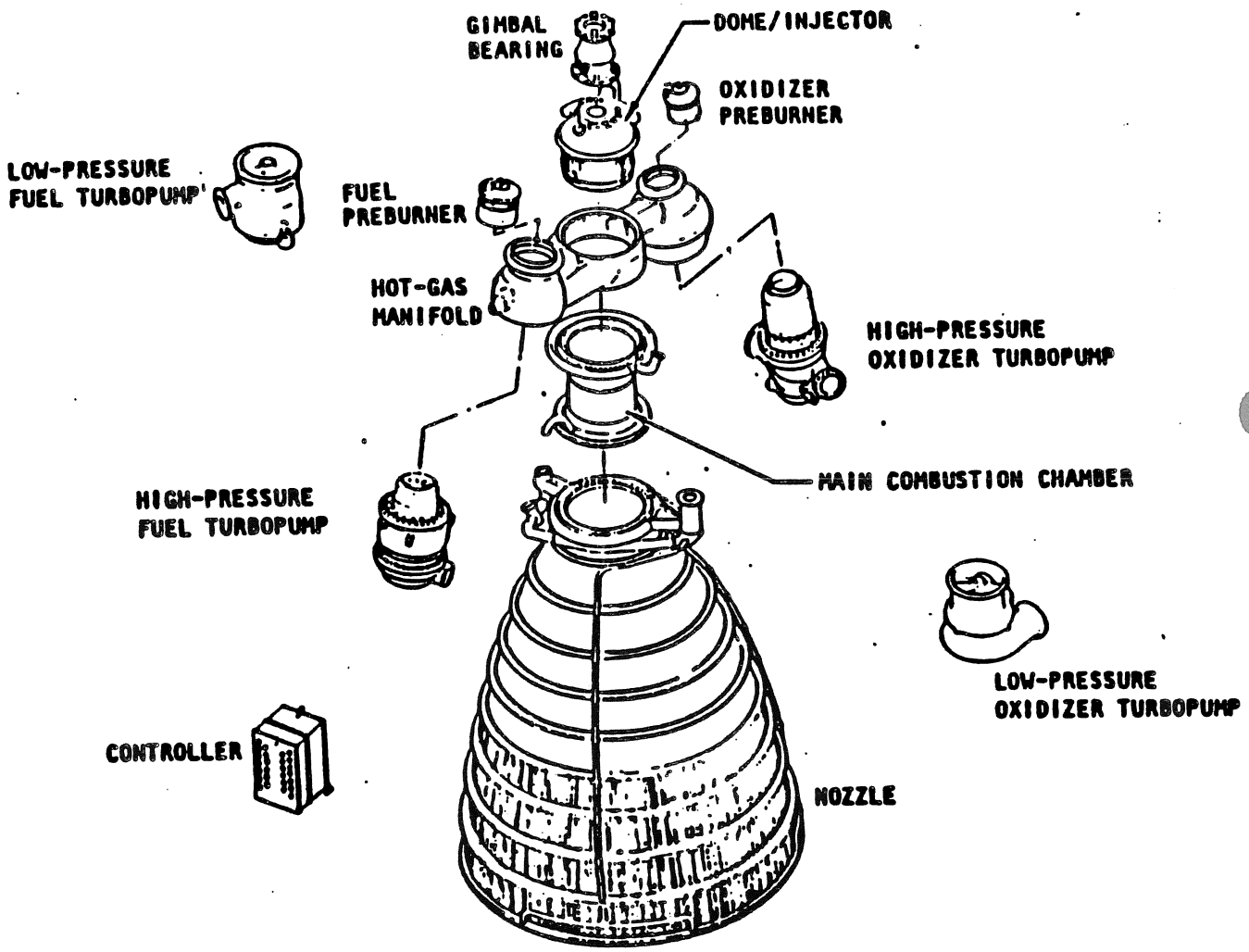


FIGURE 1 - 1

ENGINE FLOW SCHEMATIC

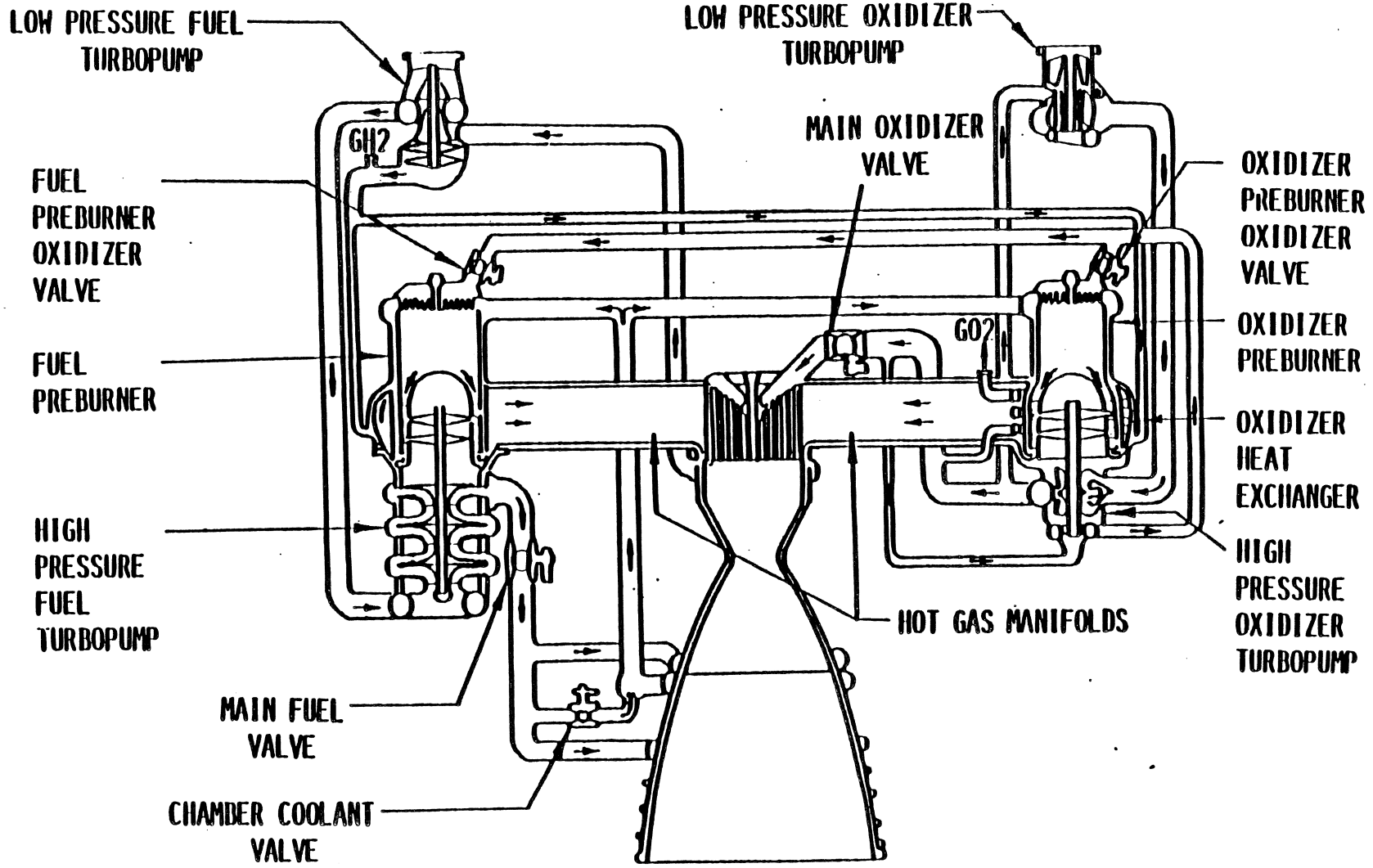


FIGURE 1 - 1.2.1

FIGURE 1 - 1.2.2
(6)

1 LOW PRESSURE FUEL TURBOPUMP (LPFTP)

2 HIGH PRESSURE FUEL TURBOPUMP (HPFTP)

3 MAIN FUEL VALVE

4 CHAMBER COOLANT VALVE

5 NOZZLE TRANSFER DUCTS (REGENERATIVE COOLING OF NOZZLE)

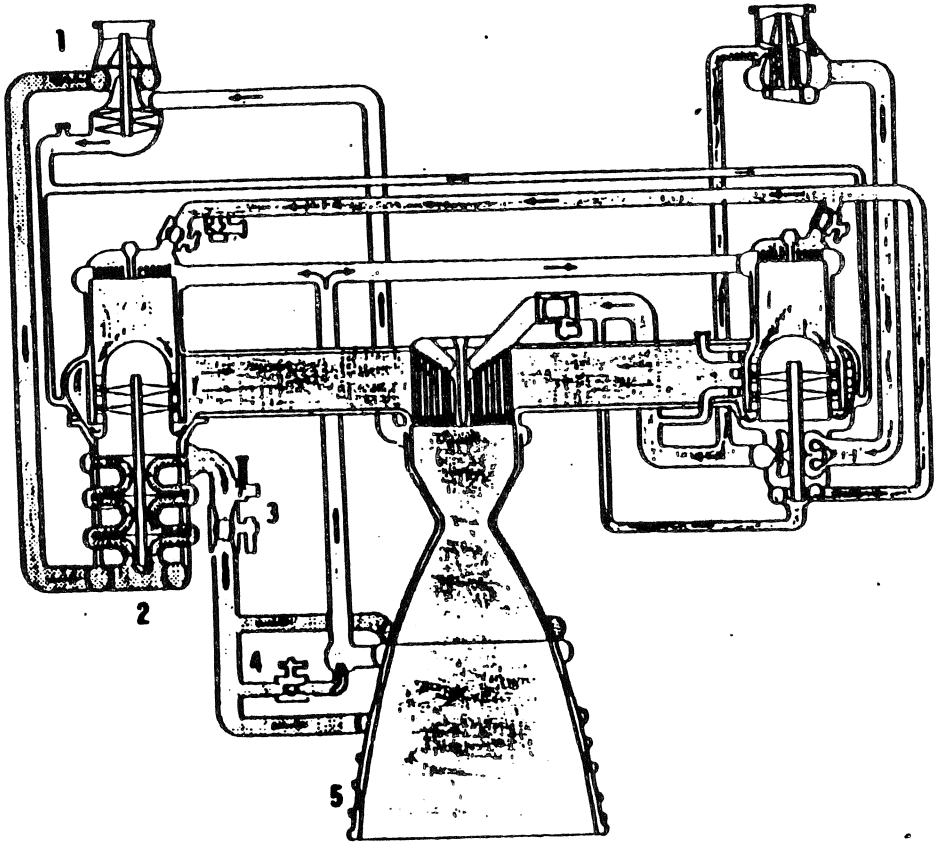


Figure 1-11.- Space Shuttle Main Engine liquid hydrogen fluid flow.

1 LOW PRESSURE OXIDIZER TURBOPUMP (LPOTP)

2 POGO SUPPRESSOR SYSTEM

3 HIGH PRESSURE OXIDIZER TURBOPUMP (HPOTP) (FIRST STAGE)

4 LOW PRESSURE PUMP (TURBINE SIDE)

5 MAIN OXIDIZER VALVE

6 MAIN INJECTOR (OXIDIZER MANIFOLD)

7 HIGH PRESSURE OXIDIZER TURBOPUMP (SECOND STAGE)

8 OXIDIZER PREBURNER OXIDIZER VALVE

9 PREBURNER OXIDIZER MANIFOLD (OXIDIZER PREBURNER)

10 FUEL PREBURNER OXIDIZER VALVE

11 PREBURNER OXIDIZER MANIFOLD (FUEL PREBURNER)

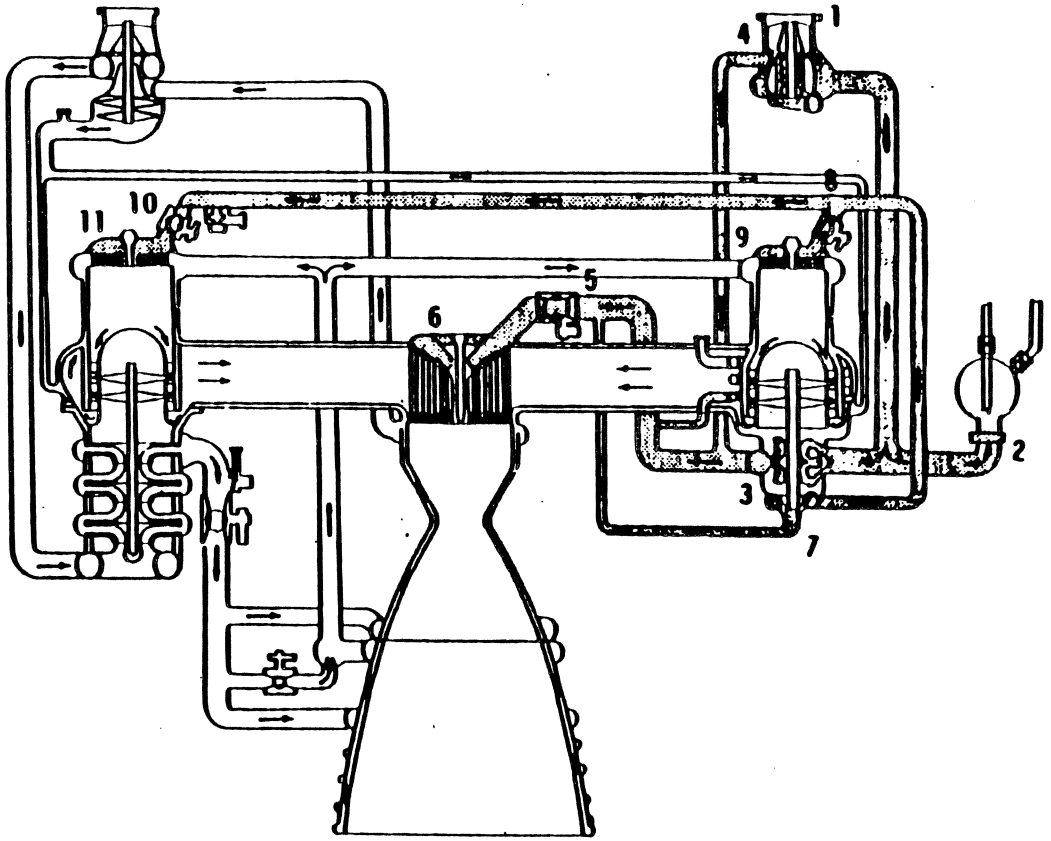


FIGURE 1 - 1.2.3

(7)

Figure 1-12.- Space Shuttle Main Engine liquid oxygen flow path.

GH_2 FLOW

1. THROUGH NOZZEL (REGENERATIVE COOLING)
2. LPFTP TURBINE
3. TO FUEL PREBURNER AND OXID. PREBURNER (FUEL SUPPLY DUCTS)
4. FUEL TANK PRESSURIZATION LINE.

1'. FUEL MIXER ASSEMBLY

2'. FUEL PREBURNER SUPPLY DUCT.

3'. OXIDIZER PREBURNER FUEL SUPPLY DUCT.

GO_2 FLOW

A. HEAT EXCHANGER

B. OXIDIZER TANK PRESSURIZATION

C. POGO ACCUMULATOR DIFFUSER

D. RECIRCULATION ISOLATION VALVE

E. OXIDIZER BLEED LINE

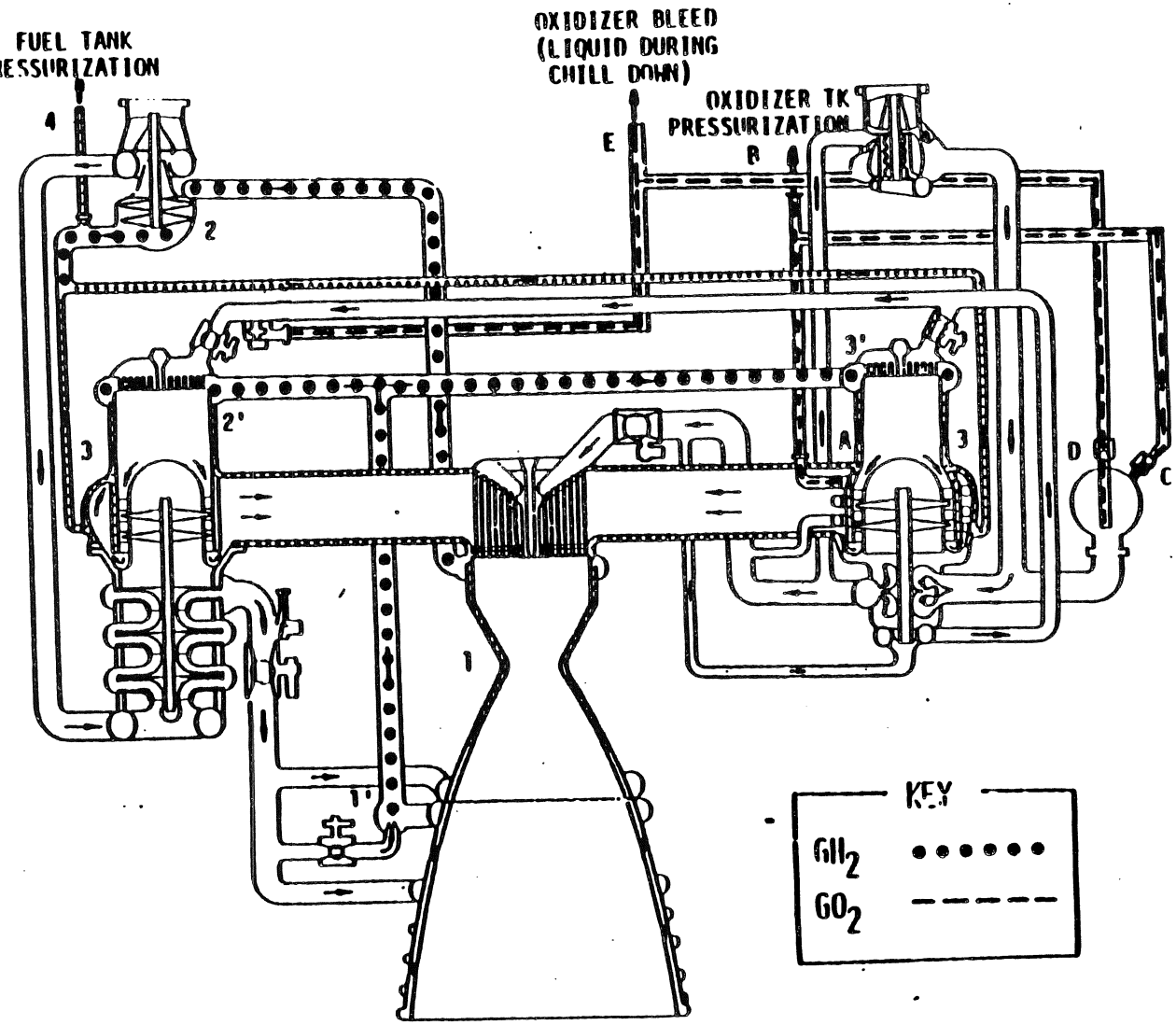


FIGURE 1 - 1.2.4

Space Shuttle Main Engine gaseous propellant flow: Mainstage operation.

PURGE SEQUENCE #1

A. GN_2 STARTS PURGE

PURGE SEQUENCE #2

B. GH_e START PURGE

PURGE SEQUENCE #3

B. GHe STOPS PURGE
(DROPPING PROPELLANTS)

PURGE SEQUENCE #4

B. GH_e STARTS PURGE

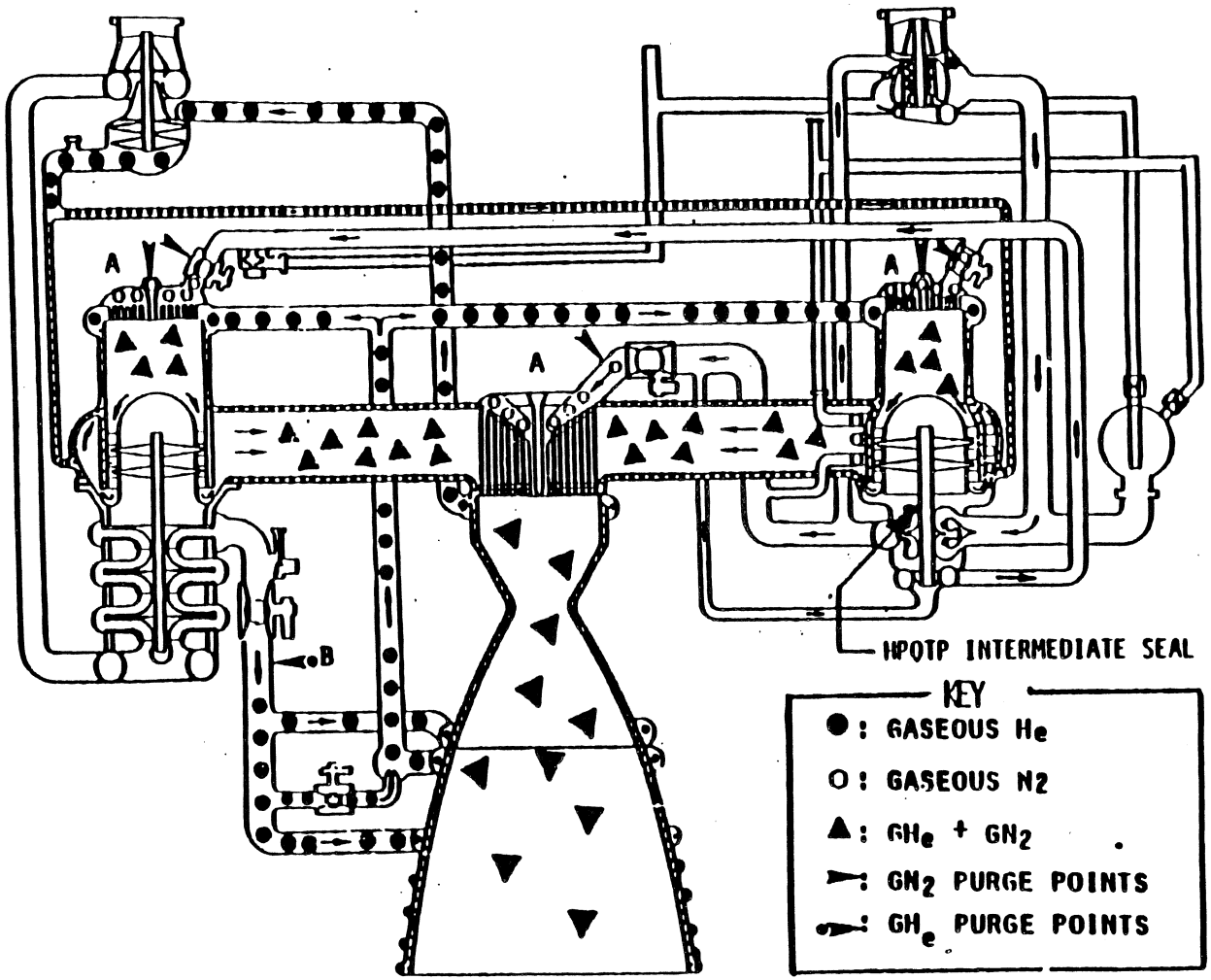


FIGURE 1 - 1.2.5

Space Shuttle Main Engine gaseous purge flow: Prestart.

(9)

TABLE 1.1
TURBO PUMP PERFORMANCE PARAMETERS

	LPOT	LPFT	HPOT		HPFT
			MAIN	BOOST	
Pump Inlet Flowrate (LB/Sec)	887.5	147.9	1067.1	108.7	148.4
Pump Inlet Pressure (PSIA)	100.0	30.0	405.2	4146.1	200.7
Pump Discharge Pressure (PSIA)	439.2	258.5	4283.7	7329.4	6074.4
Pump Efficiency	0.681	.675	0.678	0.807	.757
Turbine Flowrate LB/Sec	179.1	26.75	62.1		153.4
Turbine Inlet Pressure (PSIA)	4109.6	--	969.9		--
Turbine Inlet Temp (Deg R)	192.0	477	1399.2	1883.3	
Turbine Pressure Ratio	--	1.27	1.495		1.476
Turbine Efficiency	0.636	.599	0.812		.783
Turbine Speed (RPM)	5161.8	15302	27885		34563
Turbine Horsepower	1566.4	2957	23950		61678

The HPOT has two separate pumps, driven from a common shaft. The "boost" pump boosts the pressure of a portion of the main pump output and delivers it to the oxidizer valves of the preburners.

The turbine stages of the high pressure turbopumps are driven by the super heated steam of the preburner chambers. The HPFT and the HPOT operate on the same principal, but are of different design because the HPFT must deliver a larger volume of fuel than the HPOT does oxidizer. For the SSME, the ideal burn combination (mixture ratio) of hydrogen with oxygen is six parts of oxygen to one part of hydrogen, but this is by weight. Since LOX is more dense, or heavier, than LH2, the volume of LH2 used is about 2.5 times that of LOX. The smaller Dewar flask at the top of the external tank carries 1,331,555 pounds of LOX. The much larger Dewar flask at the bottom of the external tank carries 223,775 pounds of LH2.

One begins to appreciate the engineering challenges for the development and fabrication of these high pressure turbo-pumps when one recognizes that the relatively short rotating shaft is super cold at the pump end and very hot at the turbine end. Furthermore, the hot gas at the turbine end, must not blend with cryogenic propellants at the pumps ends. THis latter conditions not so critical for the HPFT, but can be catastrophic for the HPOT.

Any material that is hot enough, will burn in an oxygen rich environment, even high alloy steels. Perhaps the worst thing that can happen to this engine is to have "warm to hot" metals exposed to pure oxygen. It is hard to conceive that metal will actually burn or "sputter" and still not be hot enough to melt.

High speed rotating machinery requires superior strength materials. Design concepts, and machining processes, to dynamically balance rotating parts, to fabricate bearings and seals, and to handle the extreme temperature differentials of the HPFT and HPOT, are obviously state of the art.

1.3.1.2 Low Pressure Oxidizer Turbo Pump

The Low Pressure Oxidizer Turbo Pump (LPOTP) is an axial flow pump directly driven by a six stage axial flow turbine that is powered by liquid oxygen. During engine start and mainstage, the LPOTP maintains sufficient pressure to the high pressure oxidizer turbo pump (HPOTP) to permit the HPOTP to operate at high speeds. Turbine drive fluid is tapped fromthe HPOTP discharge and, after powering the turbine, is injected into the pump fluid through a port between the turbine discharge and pump discharge volutes. The combined flows are then routed to the HPOTP inlet. Since the pumped fluid and turbine drive fluid are both liquid oxygen and the LPOTP is located upstream of the oxidizer valves, the requirement for dynamic seals, purges, and drains has been eliminated.

The rotor is supported by two liquid oxygen cooled ball bearings. The turbine end bearing coolant flow path is from the last stage of the turbine, through the bearing, hollow rotor, radial holes in the rotor, and to the inducer discharge. Coolant for the inducer-end bearing is from the turbine inlet, through the rotor labryinth seal, through the bearing, and to the inducer discharge.

A redundant-element, magnetic type speed transducer for measuring shaft speed is installed on the turbine end of the turbopump housing.

1.3.1.3 Low Pressure Fuel Turbo Pump

The low pressure furl turbopump (LPFTP) is an axial flow pump directly driven by a two stage turbine that uses gaseous hydrogen (GH_2) as the power medium. During engine start and mainstage operation, the LPFTP maintains sufficient pressure to the high pressure fuel turbopump (HPFTP) to permit the HPFTP to operate at high speeds. The turbine is powered by GH_2 from the main combustion chamber (MCC) coolant outlet manifold.

The inducer and shaft are supported by three liquid hydrogen cooled (LH_2) ball bearings. The bearing coolant is the leakage across the inducer discharge labryinth seal. The coolant flows through the pump end bearings and turbine bearing and is returned to the pump inlet through passages in the shaft, bearing bearing spacer, and inducer.

Before engine start, leakage from the pump into the turbine is prevented by a spring-loaded-closed, propellant-pressure actuated-open, lift-off seal. During engine start the seal nose is separated from its mate ring when increasing fuel pressure overcomes the spring force. A positive separation between the seal nose and mate ring is maintained until engine shutdown when fuel pressure decreases below spring force. During operation, leakage from the turbine into the pump is minimized by the pump and turbine seals.

A redundant-element, magnetic-type speed transducer is installed in the pump volute to monitor shaft speed.

1.3.1.4 High Pressure Oxidizer Turbo Pump

The High Pressure Oxidizer Turbo Pump (HPOTP) consists of two single stage centrifugal pumps on a common shaft that are directly driven by a two stage hot gas turbine. The main pump received liquid oxygen from the low pressure oxidizer turbo pump (LPOTP) and supplies it at an increased pressure to the LPOTP turbine, the heat exchanger, the preburner pump, and the thrust chamber injector. The preburner pump further increases the pressure to the level required by the oxidizer preburner (OPB) and fuel preburner (FPB). The turbine is powered by hot gas (hydrogen rich steam) supplied by the OPB. Mixing of oxidizer and hot gas is prevented by seals, a purge, and drains. Two duplex sets of liquid oxygen cooled ball bearings support the rotating parts. The HPOTP is flange attached to the hot gas manifold (HGM) and is canted at a 10 degree angle out from the engine centerline.

The HPOTP main pump has a single inlet with a 50-50 flow split into a double entry, common outlet impeller. Liquid oxygen enters the main pump through the main pump housing where the flow split is made. Inlet vanes direct the flow to the inducer/impeller inlet guide vanes, which in turn direct the flow to the inducer/impeller inlets. There are four inducer blades and four full and four partial impeller blades oneach side of the combined inducer/impeller. After passing through the impeller, the flow is redirected into the discharge volute by diffuser vanes.

Turbo pump shaft bearings are cooled by liquid oxygen from the preburner pump. Coolant flow for the pump-end bearings is through the preburner pump impeller hub labryinth seal, through the bearings, and to the main pump inducer/impeller inlet.

The turbine end bearings coolant flow is through the preburner impeller bolt, through the hollow shaft, through the bearings, and to the main pump inducer/impeller inlet. Pump shaft axial thrust is balanced in that the double entry main inducer/impeller is inherently balanced and the thrusts of the preburner pump and turbine are equal but opposite. Residual shaft thrust is controlled by self compensating, non-rubbing, balance piston which utilizes orifices located at the tip and inner diameter of the main shrouds to control the leakage and, consequently, the pressure acting on the respective shrouds. Mixing of oxidizer and turbine gas is prevented by a dynamic shaft seal package that is between the main pump and the turbine.

The seal package consists of a labryinth type primary oxidizer seal, a purged controlled gap intermediate seal, and two controlled gap turbine hot gas seals. Drain cavities with overboard drain lines are located between the primary oxidizer seal and the intermediate seal, between the intermediate seal and secondary turbine seal, and between the secondary and primary turbine seals. To further ensure against the mixing of oxidizer and turbine gas, a helium purge is applied between the elements of the intermediate seal during engine operation.

The preburner pump has single entry impeller that discharges oxidizer through diffuser vanes into the discharge volute. The preburner pump housing is flange mounted to the main pump housing. Impeller seals interface with levels cut in the outside diameter of the impellller shroud and hub to minimize leakage back to the pump inlet and to control the flow for cooling the pump end bearings.

1.3.1.5 High Pressure Oxidizer Turbo Pump Turbine

The high pressure oxidizer turbo pump turbine is powered by hot gas (hydrogen rich steam) generated by the oxidizer preburner (OPB). Hot gas enters the turbine and flows across the shielded support struts, through the first and second stage nozzles and blades, and is discharged into the hot gas manifold (HGM). The turbine rotors are mated through a curvic coupling and are held together with a circle of bolts. The second stage rotor is integral with the pump shaft. Turbine blade to housing leakage is minimized by lands on the outer perimeter of the blade shrouds that run against seals in the turbine housing.

All components of the turbine are cooled by gaseous hydrogen flowing over or through them. Coolant is supplied from the OPB coolant jacket. After cooling the turbine components, the coolant is exhausted into the hot gas flow stream.

Turbine to OPB sealing accomplished by a pair of concentric bellows that load dual seals in the turbine inlet flange to the OPB. The diameter of the turbine rotors with blades is approximately 11 inches.

1.3.1.6 High Pressure Fuel Turbo Pump

The High Pressure Fuel Turbo Pump (HPFTP) is a three stage centrifugal pump that is directly driven by a two stage hot gas turbine. The pump receives fuel from the Low Pressure Fuel Turbo Pump (LPFTP) and supplies it at increased pressure, through the main fuel valve (MFV), to the thrust chamber assembly coolant circuits. The turbine is powered by hot gas (hydrogen rich steam) generated by the FPB.

Fuel flows in series through the three impellers from pump inlet to outlet, with flow being redirected between the impellers by interstage diffusers.

Coolant flow across the pump end bearings is provided by the first stage impeller backplate wear ring flow. The coolant is returned to the inlet of the first stage impeller. Coolant flow the turbine end bearings is supplied from the pump balance piston cavity through the shaft static lift off seal.

Axial rotor thrust is controlled by a self compensating, double acting balance piston that operates between high and low pressure orifices to maintain thrust at zero during normal operation. A thrust bearing, located at the pump inlet end of the rotating assembly, absorbs rotor thrust during start, cutoff, and throttling transient operations.

Before engine start, leakage from the pump into the turbine is prevented by spring-loaded-closed/propellant-pressure-actuated open, lift-off-seal. During engine start the seal nose is separated from its mate ring when increasing fuel pressure overcomes the spring force. A positive separation between the seal nose and mate ring is maintained until engine shutdown when actuating pressure decreases below spring force. Propellent flow through the seal and ring is used to cool the turbine end bearings and the turbine components.

The HPFTP is flange attached to the hot gas manifold (HGM) and is canted out from the engine centerline at a 10 degree angle.

1.3.1.7 High Pressure Fuel Turbo Pump Turbine

The high pressure fuel turbo pump turbine is powered by hot gas (hydrogen rich steam) generated by the fuel preburner (FPB). Hot gas enters the turbine and flows across the shielded support struts, through the first and second stage nozzles and blades, and is discharged into the hot gas manifold (HGM).

The turbine disks are mated through a curve coupling and are held together with a circle of bolts. The two stage turbine transmits torque to the pump by a splined coupling between the second stage wheel and the pump third stage impeller.

Bearing and turbine coolant is supplied through the shaft static lift off seal when the seal is lifted at engine start. The turbine coolant flows over or through the hot gas components and is then exhausted into the hot gas flow stream.

3.2 Valves

There are five servo controlled/hydraulically actuated proportional valve assemblies that control propellent flow on the SSME:

- o Main Fuel Valve MFV
- o Main Oxidizer Valve MOV
- o Coolant Control Valve CCV
- o Oxygen Preburner Oxidizer Valve OPOV
- o Fuel Preburner Oxidizer Valve FPOV

The MFV, MOV and CCV play only a minor role in the control of the propellent flow. The OPOV and FPOV play major roles because they control the speeds of the HPOT and HPFT respectively.

Simply stated, SSME power levels, are proportional to the quantities of propellents burned in the Main Combustion Chamber (MCC). The quantities of LH2 and LOX delivered to the MCC are a function of the HPFT and HPOT speed.

The speed of the HPFT is controlled by the intensity of the fire within the preburner chamber of the HPFT. The FPOV controls the intensity of this combustion by increasing or decreasing the amount of oxidizer used with the available fuel. More oxidizer means a hotter fire and higher pressure gases to increase the HPFT speed.

In similar fashion, the speed of the HPOT is controlled by the intensity of the combustion within the HPOT Preburner (PB) chamber. The OPOV adds or withholds oxidizer to control that combustion.

Through its control of HPOT speed, the OPOV controls the flow of LOX to the Main Combustion Chamber (MCC). In this fashion, the OPOV controls engine thrust levels.

By controlling the HPFT speed and hence the amount of LH2 that enters the preburners and the MCC, through fixed orifices, the FPOV controls mixture ratio.

The SSME engine control is basically oxidizer control. The controlled LOX flow to the three combustion chambers, comes down the center post of concentric injector elements.

The LH2 bleeds through openings in the outer shell of these concentric elements. Proper mixture ratio, in the three combustion chambers, is maintained by HPFT speed which, in turn, pushes the desired quantities of LH2 through these fixed orifices.

Each valve assembly is a complex arrangement of solenoids, hydraulic and pneumatic porting, and shuttle valves. A major part of each assembly are the dual servo actuators (channel A and channel B). These servos are controlled by the SSME Controller. Channel A is primary control for the hydraulic positioning of the valve. If channel A fails, solenoids and shuttle valves can be positioned to permit the channel B servo to control the hydraulic positioning of the valve.

System redundancy management dictates that, if any a channel A servo loop fails, all of channel B servo loops shall be activated. If later, one of the B servos fails and the engine is in stable MAINSTAGE burn, the SSMEC "hydraulically locks" the position of all five valves and simply monitors engine performance for any emergency shutdown condition. The engine continues at that power level and is no longer throttleable. In this condition, the SSMEC cannot shutdown the engine (close the valves) hydraulically, and must rely on a back up system to shut down.

Backing up the electronic/hydraulic control of the servovalves is yet another contingency system, the PNEUMATIC CONTROL ASSEMBLY (PCA). The PCA uses pressurized Helium to actuate all valves closed whenever the SSMEC does not, or is unable to, keep the EMERGENCY SHUTDOWN or the FAIL SAFE solenoids energized. Like a continual guardian, the PCA stands ready to shutdown the engine if electronic control does not hold the PCA in abeyance.

1.3.2.1 Proportional Valves Description

1.3.2.1.1 Main Fuel Valve

The Main Fuel Valve (MFV) is a hydraulically actuated, ball type valve with a 2.5 inch propellant flow passage. The MFV is flange mounted between the high pressure fuel duct and coolant inlet distribution manifold of the thrust chamber nozzle. The valve permits or stops the flow to the thrust chamber coolant circuits, the Low Pressure Fuel Turbo Pump (LPFTP) turbine, hot gas manifold (HGM) coolant circuit, and the oxidizer preburner (OPB), Fuel Preburner (FPB), and the three augmented spark igniters (ASIs). Valve position is controlled by commands from the engine controller.

The valve consists of two major moving components: The integral ball/shaft/cams and the ball seal retracting mechanism. the ball outlet seal is a machined plastic, bellows loaded closed seal.

The ball seal is placed at the outlet of the valve (as opposed to the inlet) to expose the valve housing to liquid hydrogen during engine conditioning (chill down). Redundant shaft seals, with an overboard drain cavity between them, prevent leakage along the shaft (actuator end) during engine operation. Inlet and outlet throttling sleeves align the flow to minimize turbulence and the resultant pressure loss. Ball seal wear is minimized by cams and a cam follower assembly that displaces the seal away from contact with the ball after the initial few degrees of ball travel when being opened. Figure 1-3 shows control fluid flow.

1.3.2.1.2 Main Oxidizer Valve

The Main Oxidizer Valve (MOV) is a ball type valve with a 2.5 inch propellent flow passage, flange mounted between the main chamber oxidizer dome and the high pressure oxidizer duct. The valve controls oxidizer flow to the main chamber LO_2 dome and main chamber Augmented Spark Igniter (ASI) and is operated by a hydraulic servoactuator mounted to the valve housing. The servoactuator receives its control signals from the controller.

The valve consists of two major moving components: the integral ball/shaft/cams and the ball seal retracting mechanism. The ball inlet seal is machined plastic, bellows-loaded-closed seal. Redundant shaft seals, with an overboard drain cavity between them, prevent leakage along the shaft (actuator end) during engine operation. Inlet and outlet throttling sleeves align the flow to minimize turbulence and the resultant pressure loss. Ball seal wear is minimized by cams and a cam follower assembly that displaces the seal away from contact with the ball after the initial few degrees of ball travel when being opened. Figure 1-3 shows control flow.

1.3.2.1.3 Chamber Coolant Valve

The Chamber Coolant Valve (CCV) is a hydraulically actuated, gate type valve that serves as a throttling control to maintain proper fuel flow through the main combustion chamber and nozzle coolant circuits. The valve is installed the chamber coolant valve duct which is an integral component of the nozzle forward manifold assembly and provides the housing for the valve.

The gate has 1.6 inch flow passage. The CCV does not have a gate seal as it is located downstream of the main fuel valve and is not required to be a positive shutoff valve. Redundant shaft seals, with an overboard drain cavity between them, prevent leakage along the shaft (actuator end) during engine operation.

The valve gate is positioned by commands from the engine controller. Its position is scheduled linearly with thrust reference.

1.3.2.1.4 Oxidizer Preburner Oxidizer Valve

The Oxidizer Preburner Valve (OPOV) is a hydraulically actuated, ball type valve with 1.1. by 0.374 inch propellent flow slot. The OPOV is flange mounted between oxidizer supply line to the oxidizer preburner (OPB) and the OPB oxidizer inlet. The valve permits or stops the flow of oxidizer to the OPB and the OPB augmented spark igniter (ASI). Valve position is controlled by commands from the engine controller; during mainstage operation the valve is modulated to control engine thrust between minimum power level (MPL) and full power level (FPL).

MAIN FUEL AND MAIN OXIDIZER VALVE SERVO ACTUATOR

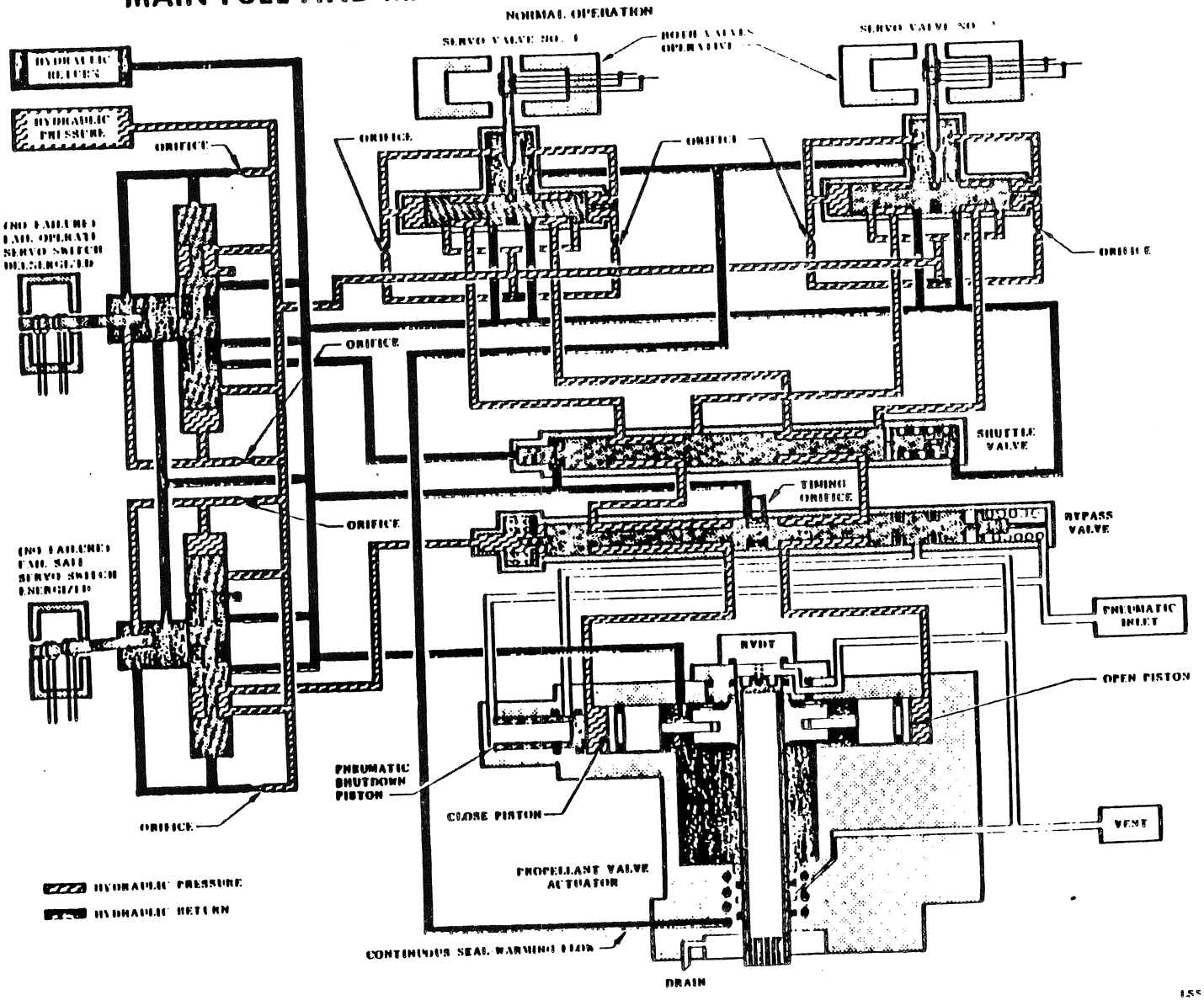


FIGURE 1 - 3

(20)

The valve consists of two major moving components: the integral ball/shaft/cams and the ball seal retracting mechanism. The ball inlet seal is a machined plastic, bellows loaded closed seal. Redundant shaft seals, with an overboard drain cavity between them, prevent leakage along the shaft (actuator end) during engine operation. Inlet and outlet throttling sleeves align the flow to minimize turbulence and the resultant pressure loss. Ball seal wear is minimized by cams and a cam follower assembly that displaces the seal away from the contact with the ball after the initial few degrees of ball travel when being opened. A flow "slot", as opposed to a flow "hole", makes valve opening versus ball rotation a linear function.

1.3.2.1.5 Fuel Preburner Oxidizer Valve

The Fuel Preburner Oxidizer Valve (FPOV) is a hydraulically actuated, ball type valve with a 1.1 inch propellant flow passage. The FPOV is flange mounted between the oxidizer supply line to the fuel preburner (FPB) and the FPB oxidizer inlet. The valve permits or stops flow of oxidizer to the FPB and the FPB augmented spark igniter (ASI). Valve position is controlled by commands from the engine controller; during mainstage operation the valve is modulated to maintain the desired engine mixture ratio.

The valve consists of two major moving components: the integral ball/shaft/cams and the ball seal retracting mechanism. The ball inlet seal is machined plastic, bellows loaded closed seal. Redundant shaft seals, with an overboard drain cavity between them, prevent leakage along the shaft (actuator end) during engine operation. Inlet and outlet throttling sleeves align the flow to minimize turbulence and the resultant pressure loss. Ball seal wear is minimized by cams and a cam follower assembly that displaces the seal away from contact with the ball after the initial few degrees of ball travel when being opened.

1.3.2.1.6 Propellent Valve Hydraulic Actuators

Hydraulic power is provided for the operation of five valves in the propellent feed system (oxidizer preburner oxidizer, fuel preburner oxidizer, main oxidizer, main fuel, chamber coolant valves). Servo actuators mounted to the propellent valves convert vehicle supplied hydraulic fluid pressure to rotary motion of the actuator shaft as a functon of electrical input command.

Two servovalves, which are integral with each servo actuator, convert the electrical command signal from the engine controller to hydraulic flow to position the valve actuator. The dual servovalves provide redundancy that permits a single servovalve failure with no change in actuator performance. A fail operate servoswitch is used to automatically select the redundant servovalve upon failure of a single servovalve. A fail safe servoswitch is used to hydraulically lock up the servo actuator upon failure of both servovalves.

A heater is installed on the MFV actuator neck (at the valve interface flange) to maintain the hydraulic fluid temperature at the required level.

A dual, redundant, rotary variable differential transformer (RVDT) is connected to the actuator shaft and returns two electrical signals of actuator position to the controller.

All actuators are capable of utilizing an emergency shutdown system to pneumatically close the propellent valves. Pneumatic sequence valves in the oxidizer and fuel preburner actuators provide for a proper closing sequence of the propellent valves during an emergency shutdown condition. A pneumatic sequence valve in the chamber coolant valve actuator is used to terminate the engine post shutdown purges. Figure 1-4 is a typical hydraulic actuator.

1.3.2.1.7 Normal, fail-safe, fail-operate and pneumatic shutdown Figures 1-5.1 through 1-5.4 shows the control fluid flow the preburner and CCV valves for normal, fail-safe, fail-operate and pneumatic.

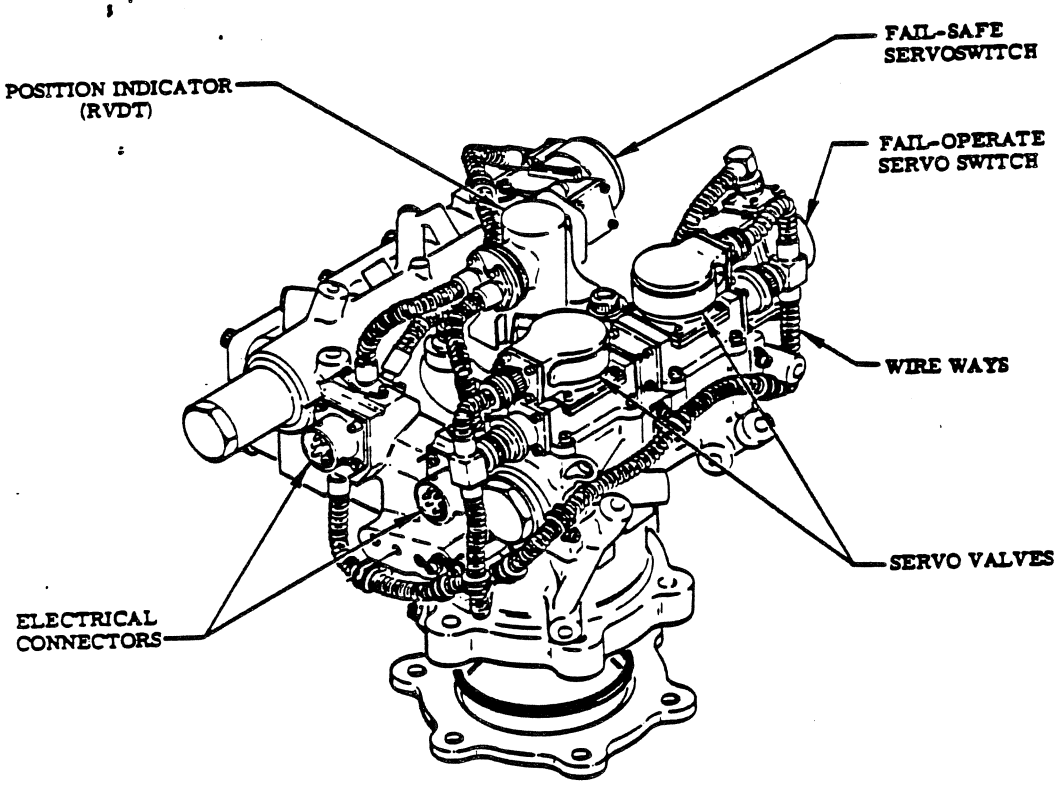
1.3.2.2 Other Valves

In addition to the servo valves there are other valves that also play a part in the engine start, shutdown and safety.

1.3.2.2.1 Propellent Bleed Valves

The Oxidizer Bleed Valve (OBV) and Fuel Bleed Valve (FBV) are spring and bellows loaded closed, pneumatically actuated open, metal to metal seat, poppet valves. The valves are opened by pneumatic pressure from the Pneumatic Control Assembly (PCA) during engine start preparation.

This provides a recirculation flow for propellants through the engine to ensure that propellants in the engine are at the required temperatures for engine start. At engine start, the valves are closed by venting the actuation pressure. The valves are fail-safe in that pressure acting on the unbalanced area poppet, combined with spring bellows forces, can overcome the actuation pressure. The valves have linear variable differential transformers (LVDT) for full open or full closed position indication.



TYPICAL SERVO VALVE HYDRAULIC ACTUATOR

FIGURE 1 - 4
(23)

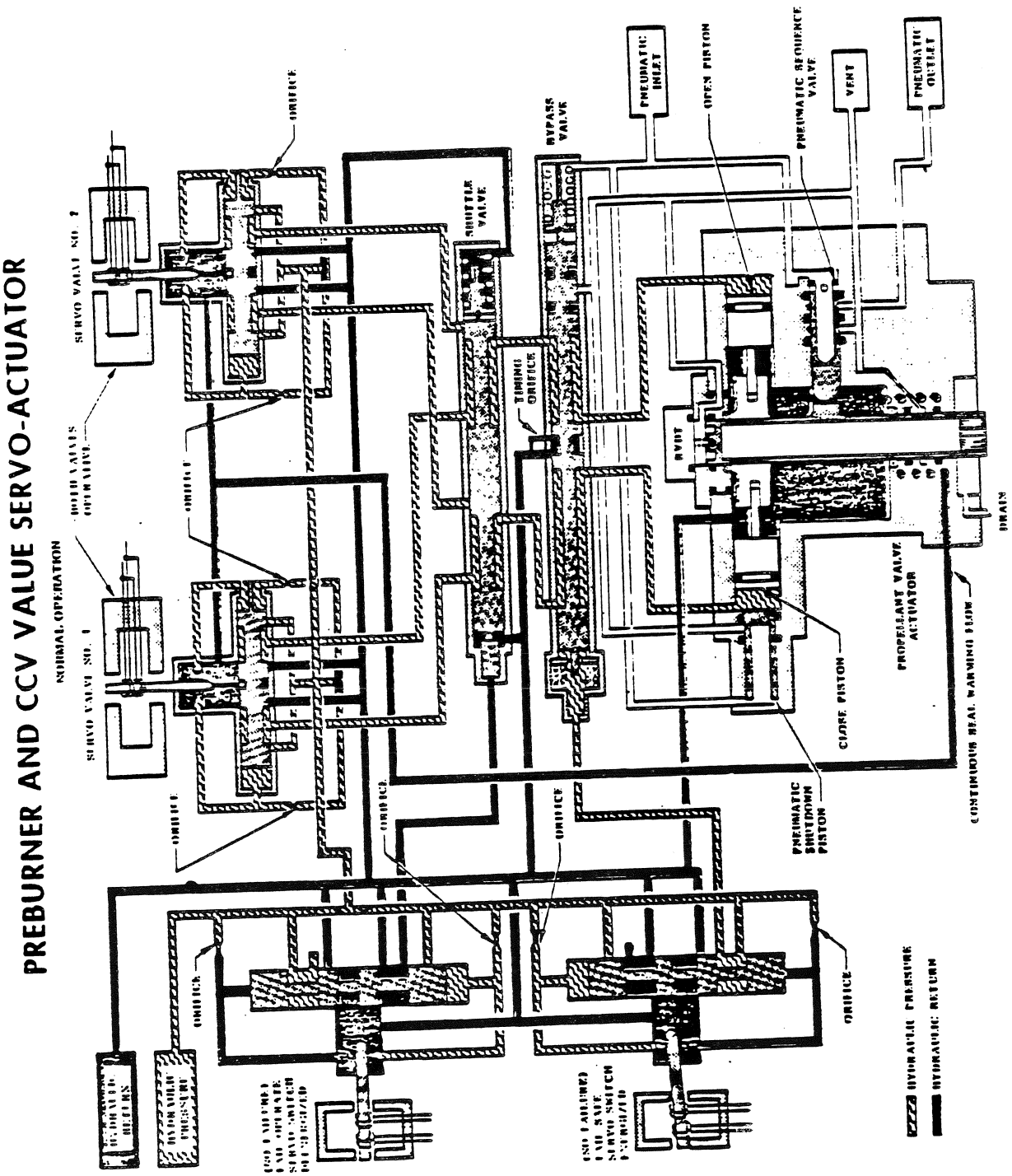

PREBURNER AND CCV VALUE SERVO-ACTUATOR
NORMAL OPERATION
SERVO VALVE NO. 1
SERVO VALVE NO. 2
ORIFICE
SHUTTLE VALVE
BYPASS VALVE
PNEUMATIC INLET
OPEN PISTON
PNEUMATIC SEQUENCE VALVE
VENT
PNEUMATIC OUTLET
TIMING ORIFICE
RVDT
CLOSE PISTON
PROPELLANT VALVE ACTUATOR
PNEUMATIC SHUTDOWN PISTON
DRAIN
HYDRAULIC PRESSURE
HYDRAULIC RETURN

FIGURE 1 - 5.1

PREBURNER AND CCV VALVE SERVO-ACTUATOR

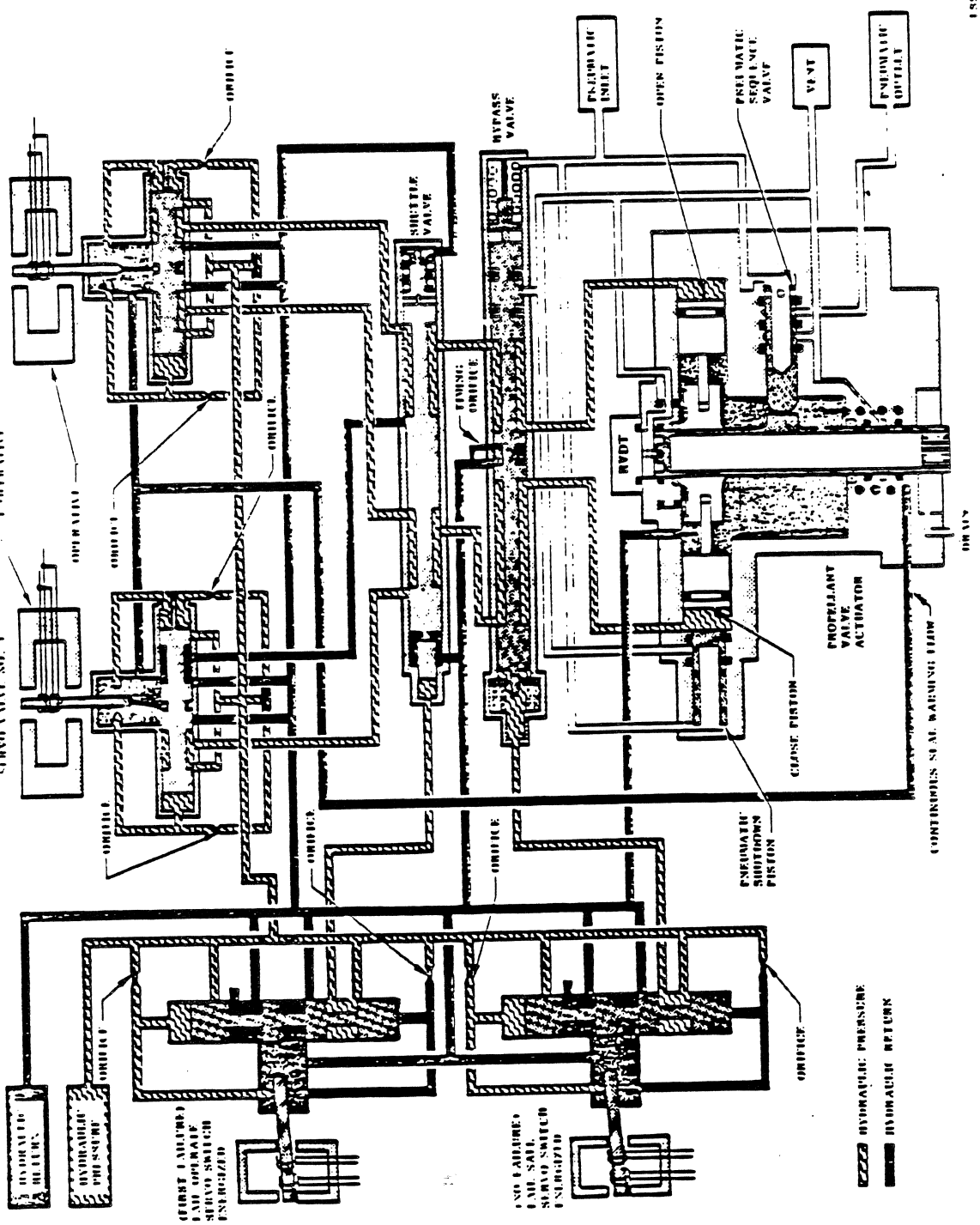


FIGURE 1 - 5.2

PREBURNER AND CCV VALVE SERVO ACTUATOR

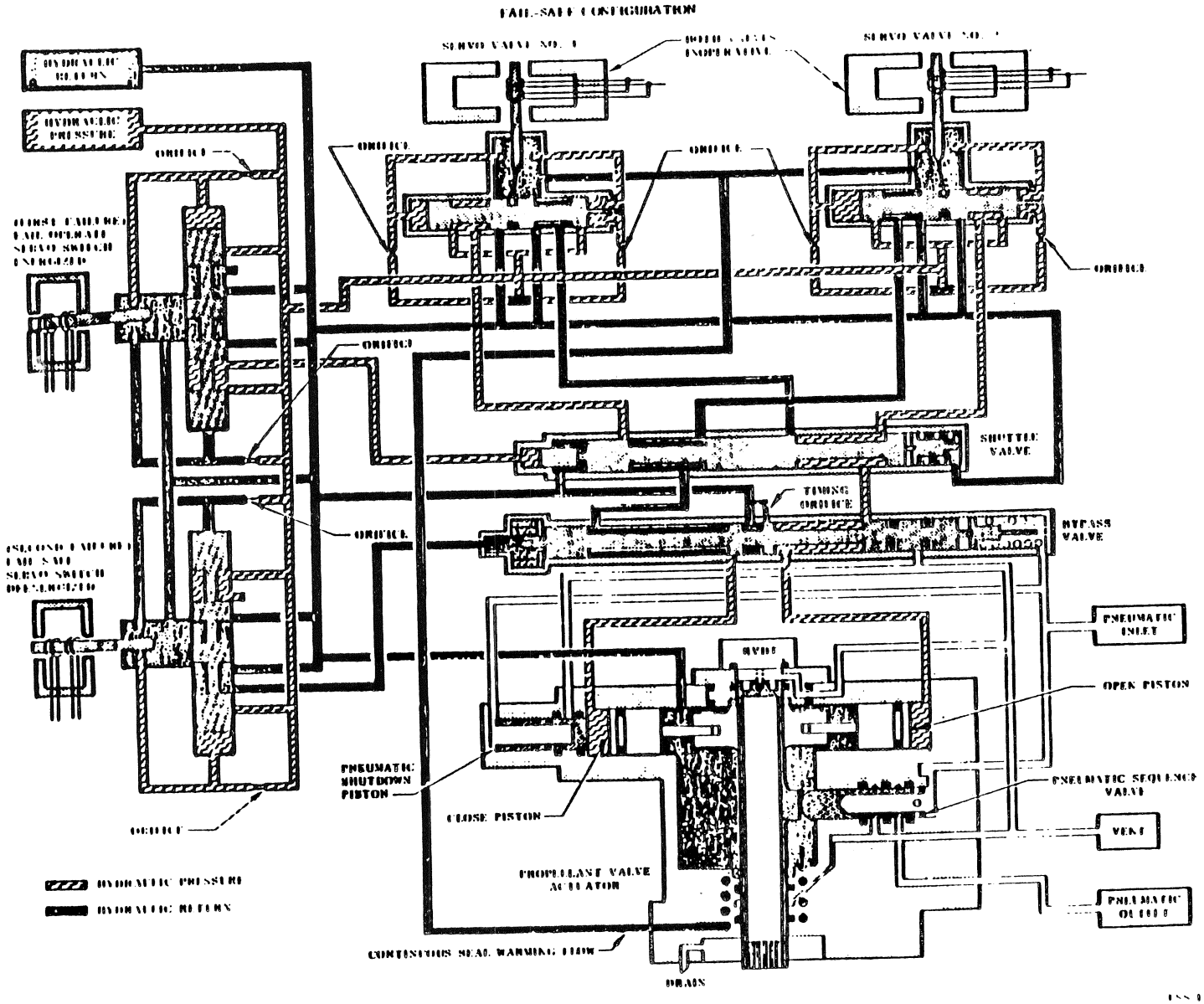


FIGURE 1 - 5.3

(26)

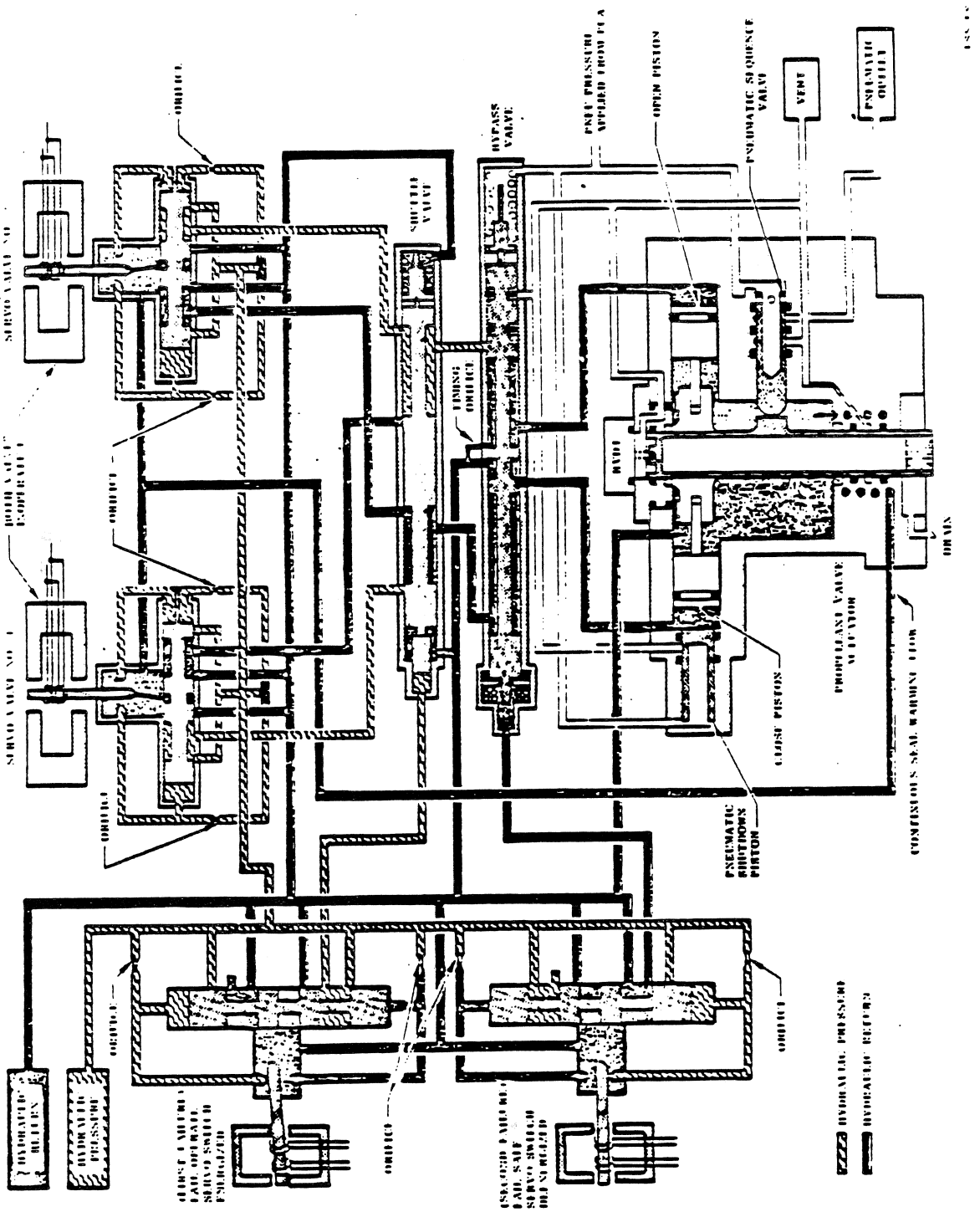

PREBURNER AND CCV VALVE SERVO-ACTUATOR
BYPASS VALVE
VENT
OPEN PISTON
CLOSE PISTON
PNEUMATIC SHUTDOWN PISTON
PROPELLANT VALVE ACTUATOR
ORIFICED
HYDRAULIC PRESSURE
HYDRAULIC RETURN

FIGURE 1 - 5.4

1.3.2.2.2 Anti Flood Valve

The Anti-Flood Valve (AFV) is a spring loaded, normally closed poppet type valve. It prevents the flow of liquid oxygen into the heat exchanger until there is sufficient heat applied to the heat exchanger during engine start to convert the liquid oxygen to gaseous oxygen.

The AFV has provisions for ground checkout without disturbing line connections, and a redundant linear variable differential transformer (LVDT) that serves as the valve dual position indicator.

1.3.2.2.3 Purge Check Valves

The pneumatic control system purge check valves are spring loaded, normally closed, pressure actuated open, poppet valves that isolate propellants from the pneumatic systems.

1.3.2.3 Pneumatic Control Assembly

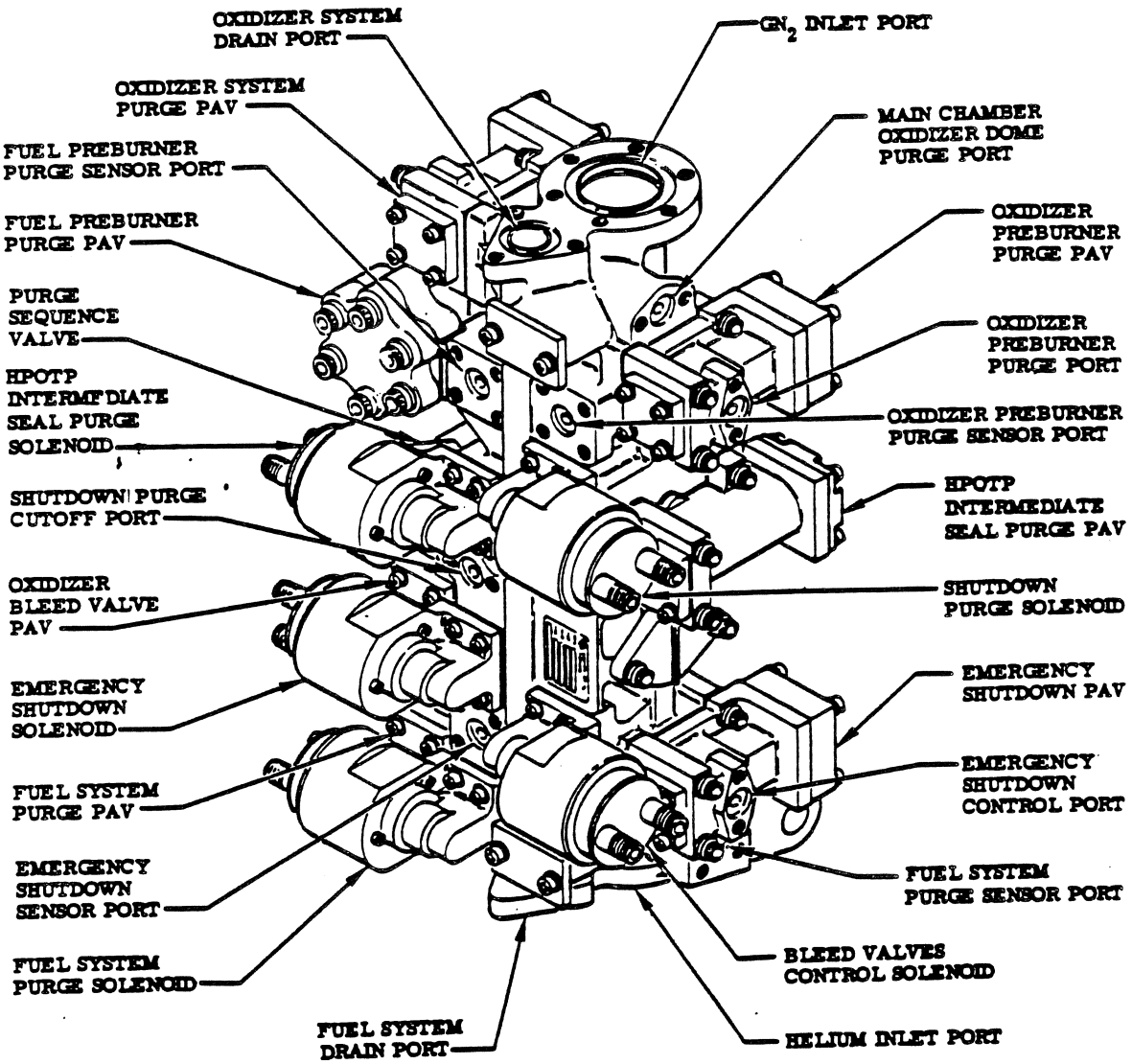
The Pneumatic Control Assembly (PCA) provides control of vehicle supplied helium during pre-start, flight, and shutdown. The helium is used for purges, for bleed valve operation, and for emergency shutdown control of the main propellant valves in the event of electrical power loss to the engine. The PCA also routes ground controlled gaseous nitrogen to the main chamber, HPOTP intermediate seal, and preburner oxidizer dome for pre start purges.

The PCA consists of a ported manifold to which solenoid valves, pressure sensors, and pressure actuated valves (PAV) are attached. The PCA is shown in Figure 1-6. Figures 1-7.1 through 1- 7.12 show the fluid flow and valve positions for various modes.

1.3.3 Ignition System

Like most engines the SSME has an Ignition System. The ignition system is an augmented spark igniter (ASI) type that initiates combustion of main propellents in the main combustion chamber (MCC) and in the fuel preburner and oxidizer preburner (FPB and OPB).

The system consists of six spark igniters, which have the spark exciter electronic circuitry integrally packaged with the spark plug, and three ASI combustion chambers, which are integral with the injector and dome assemblies of the main chamber and preburners. Ignition system propellants supplied to each of the ASI chambers are ignited by dual redundant spark igniters that are controlled and supplied with 28-vdc power by redundant power sources from the engine controller.



PNEUMATIC CONTROL ASSEMBLY

FIGURE 1 - 6
(29)

SSME PNEU SCHEMATIC (1 OF 12)

DEPICTS: NO POWER - NO PRESSURE APPLIED

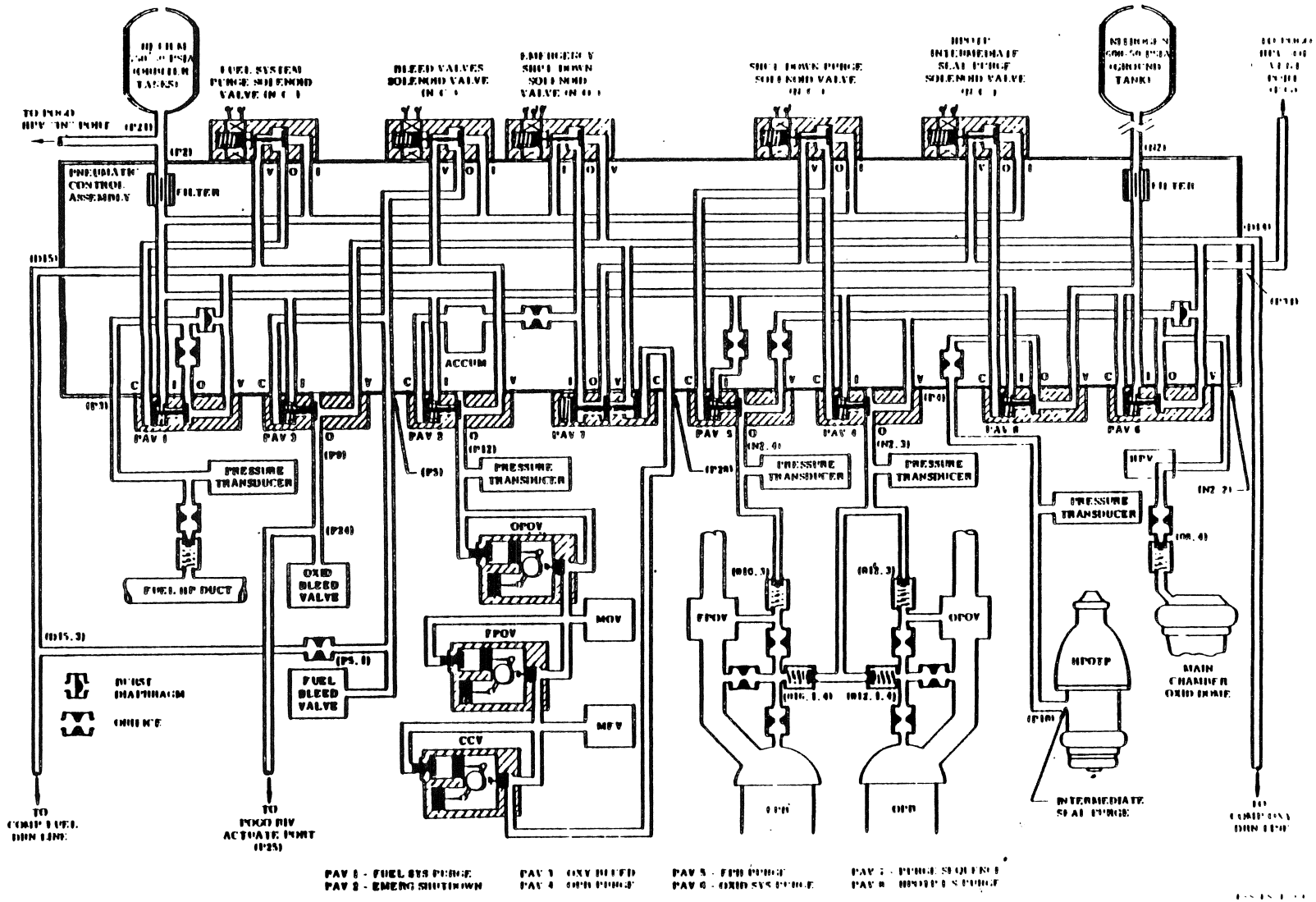


FIGURE 1 - 7.1
(30)

SSME PNEU SCHEMATIC (2 OF 12)

DEPICTS: GROUND CONTROLLED GN^2 PURGE

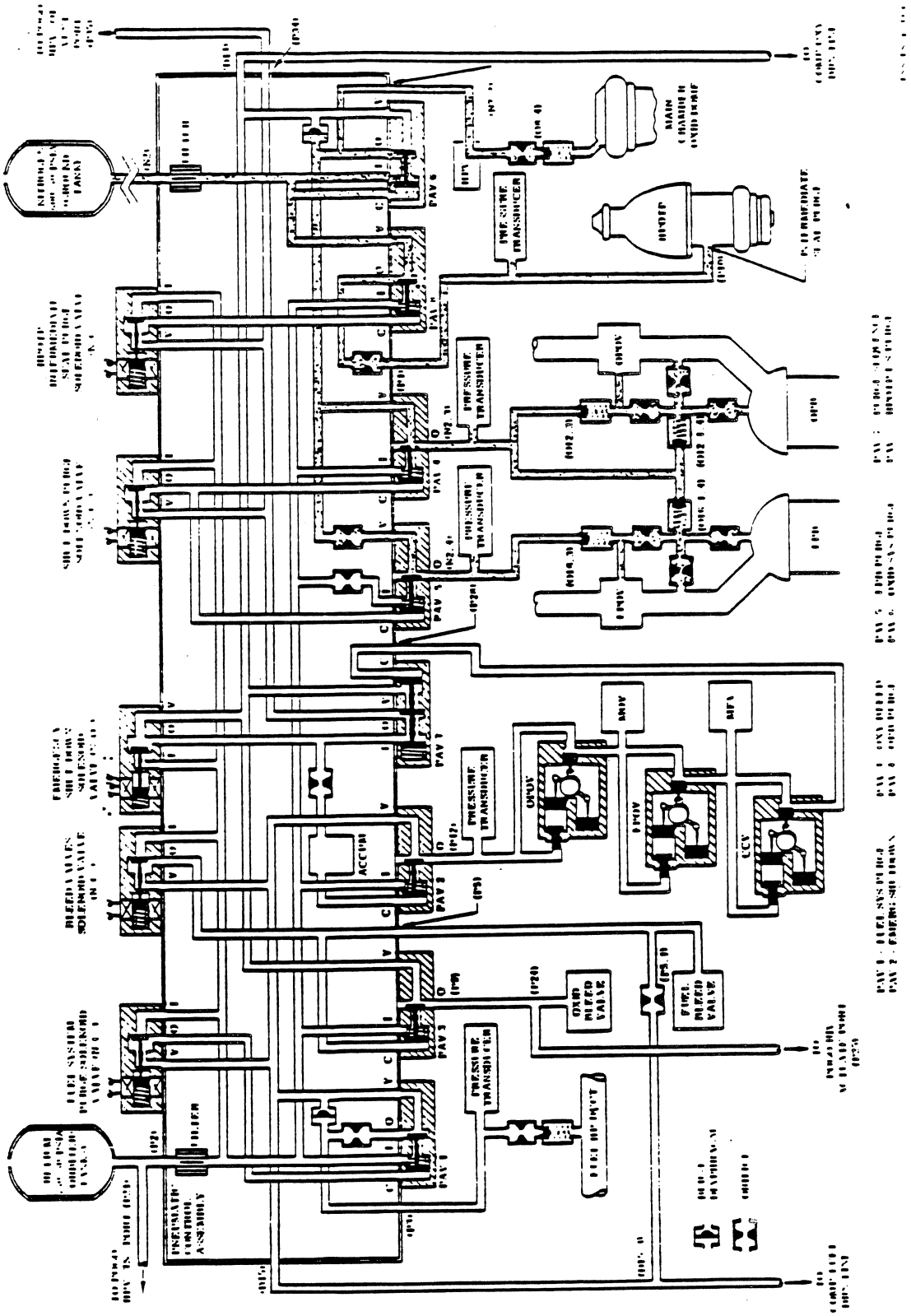


FIGURE 1 - 7.2

SSME PNEU SCHEMATIC (3 OF 12)

DEPICTS: FUEL SYSTEM PURGE

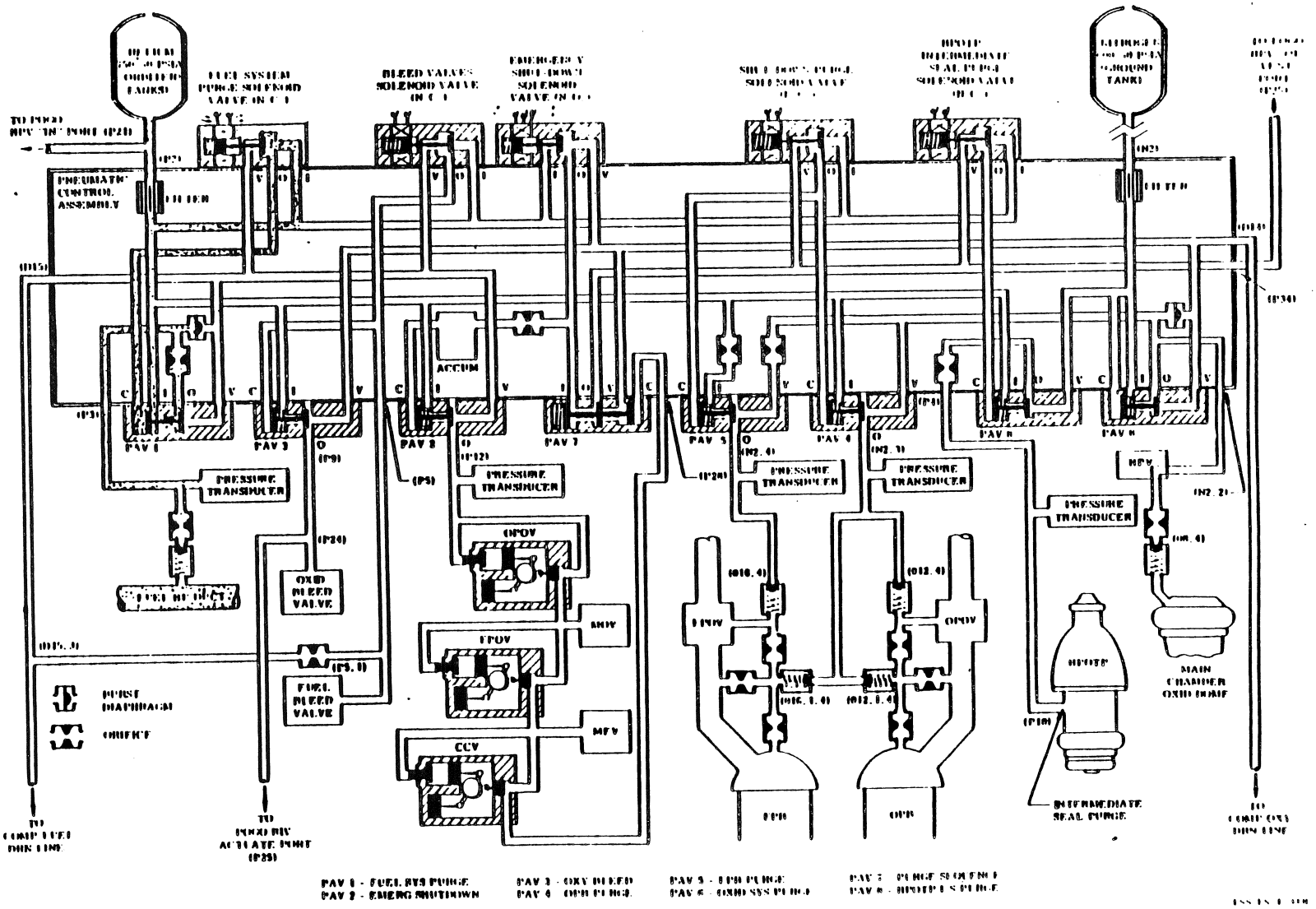


FIGURE 1 - 7.3
(32)

SSME PNEU SCHEMATIC (4 OF 12)

DEPICTS: BLEED VALVES OPEN

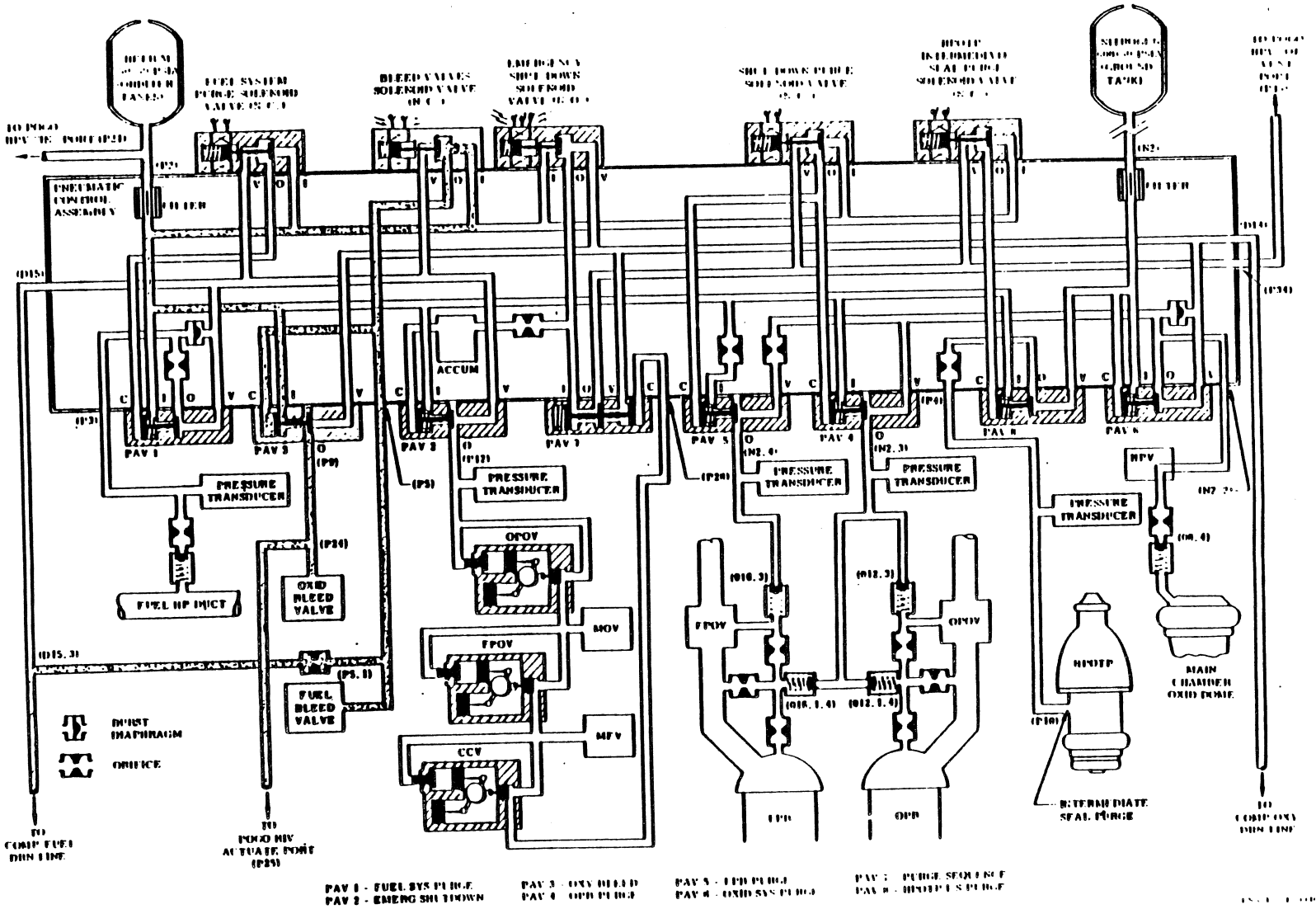


FIGURE 1 - 7.4
(33)

SSME PNEU SCHEMATIC (5 OF 12)

DEPICTS: HPOTP I/S PURGE

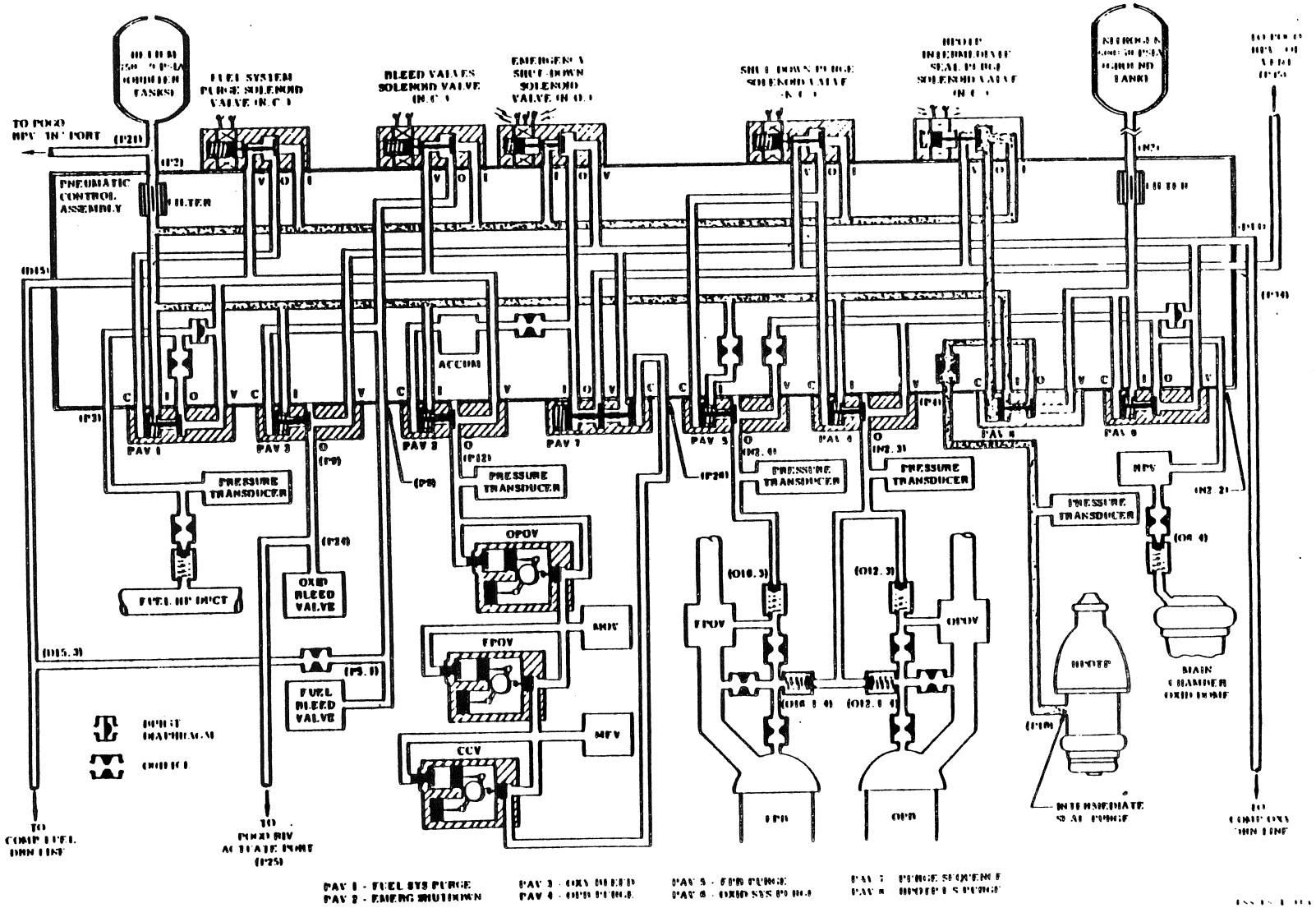


FIGURE 1 - 7.5
(34)

SSME PNEU SCHEMATIC (6 OF 12)

DEPICTS: PREBURNER PURGE (NORMAL SHUTDOWN)

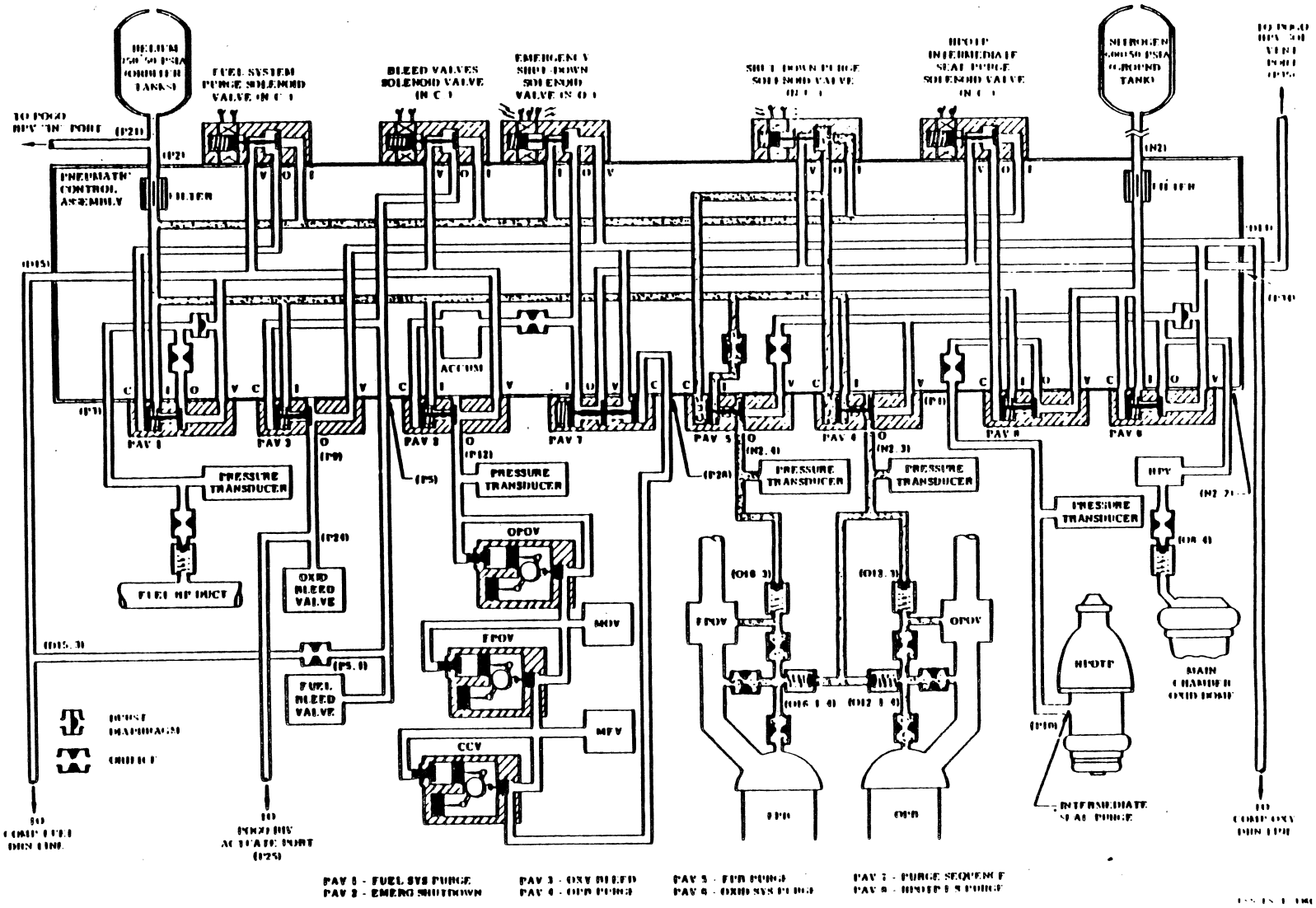


FIGURE 1 - 7.6
(35)

SSME PNEU SCHEMATIC (7 OF 12)

DEPICTS: PURGE SEQUENCE NO. 1 CONFIGURATION

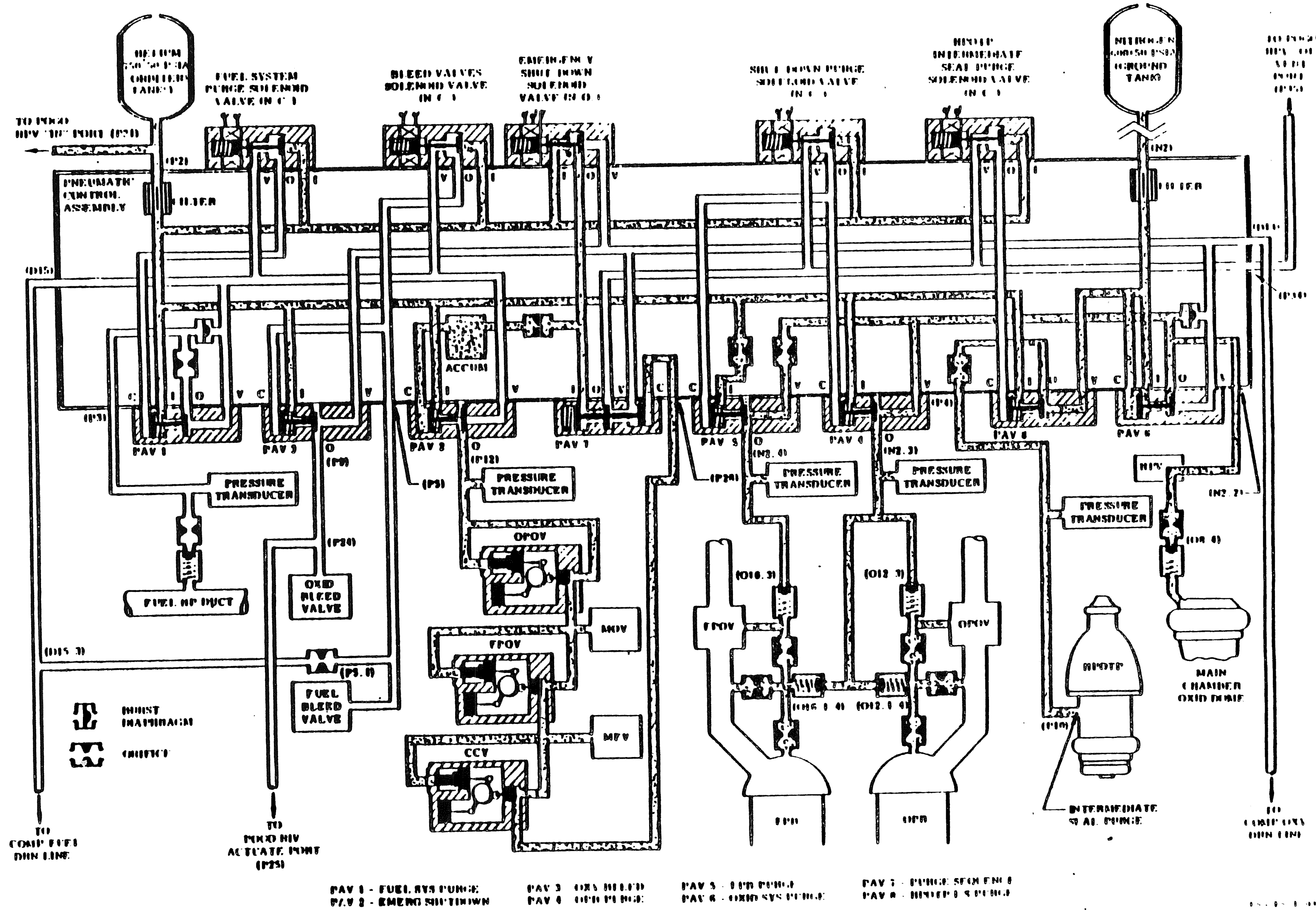


FIGURE 1 - 7.7

(36)

SSME PNEU SCHEMATIC (8 OF 12)

DEPICTS: PURGE SEQUENCE NO. 2 CONFIGURATION

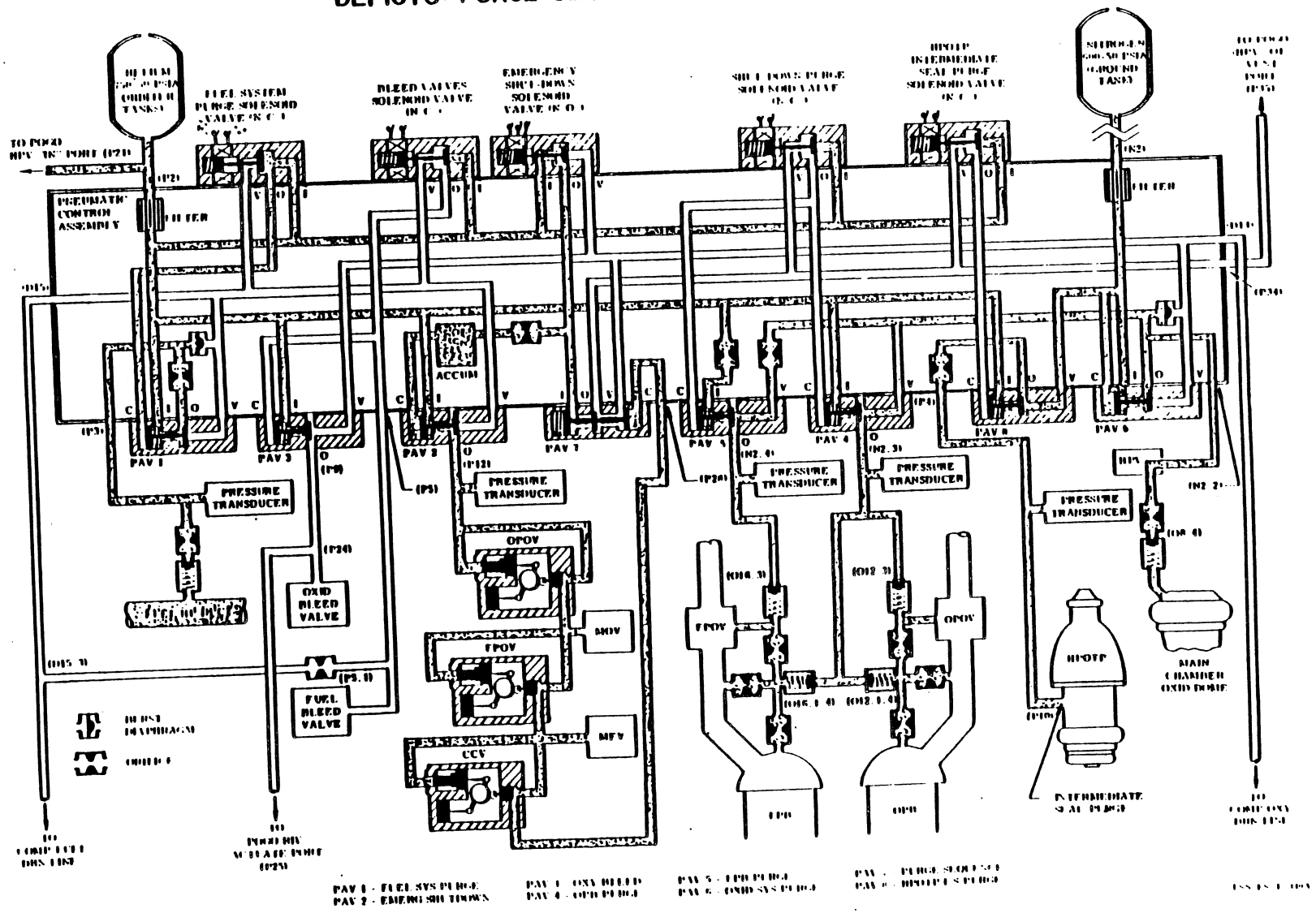


FIGURE 1 - 7.8
(37)

SSME PNEU SCHEMATIC (9OF12)

DEPICTS: PURGE SEQUENCE NO. 3 CONFIGURATION

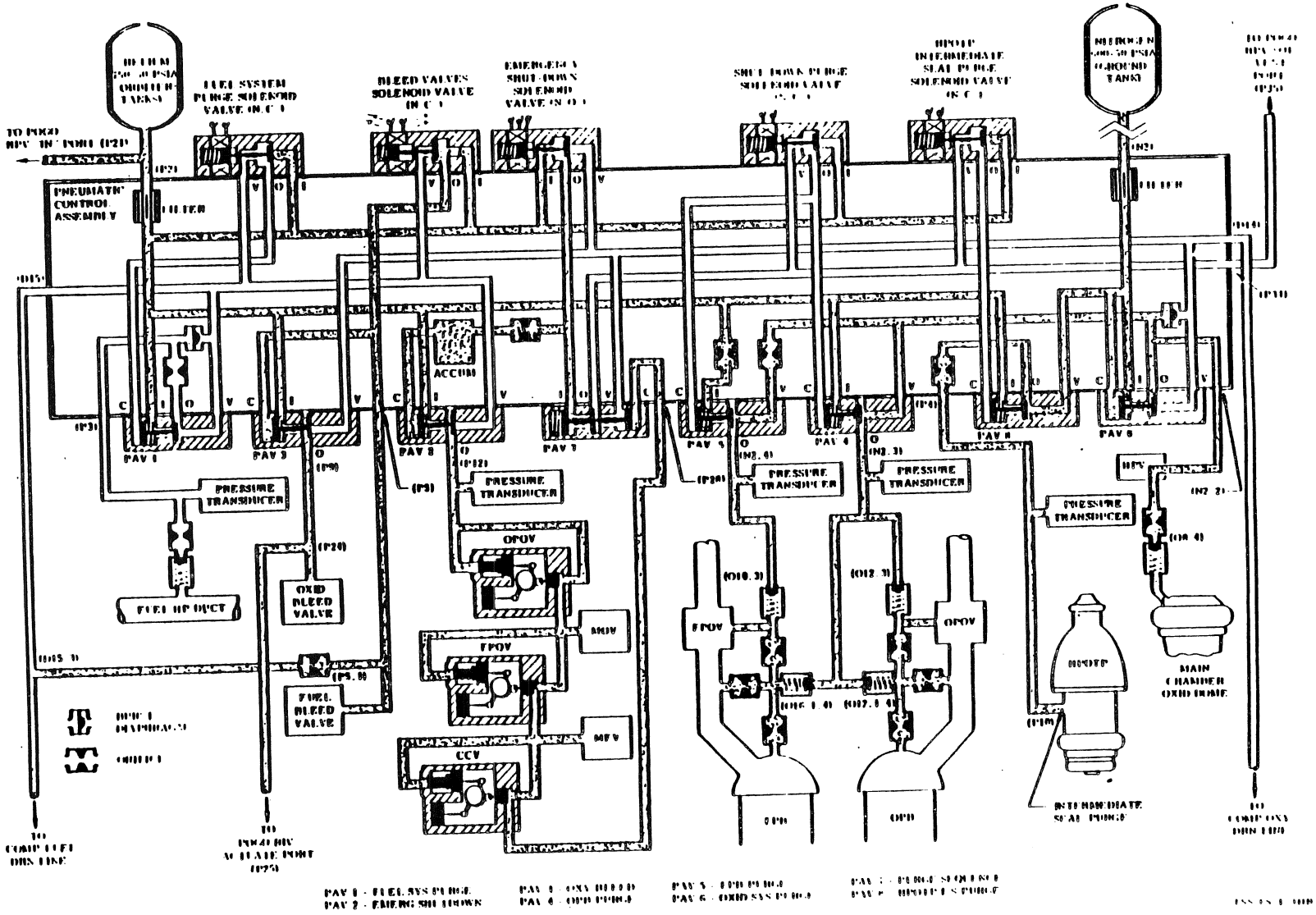


FIGURE 1 - 7.9
(38)

SSME PNEU SCHEMATIC (10 OF 12)

DEPICTS: PURGE SEQUENCE NO. 4 CONFIGURATION

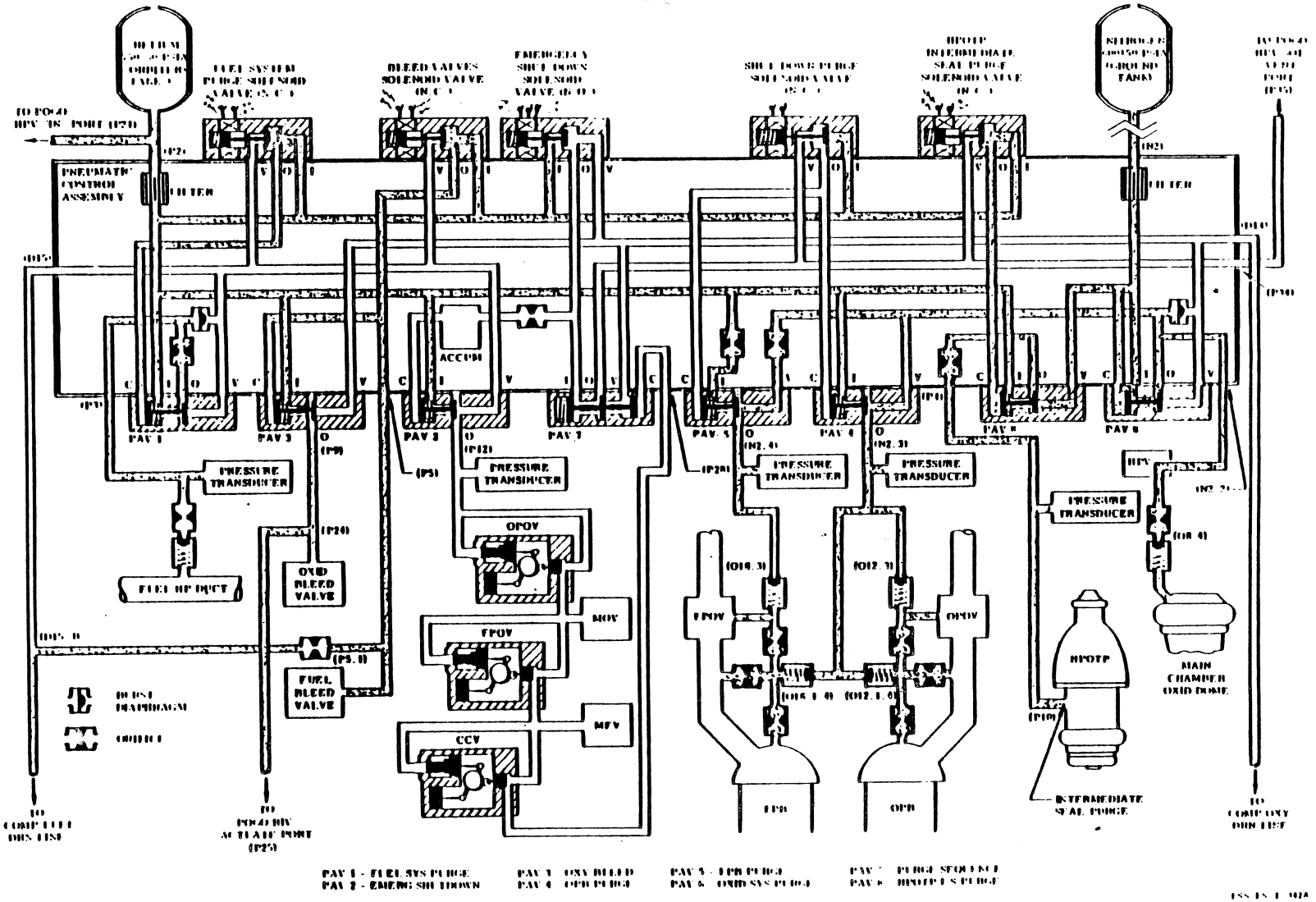


FIGURE 1 - 7.10
(39)

SSME PNEU SCHEMATIC (11 OF 12)

DEPICTS: PNEU SHUTDOWN; PROP VALVES CLOSING, PURGES ON

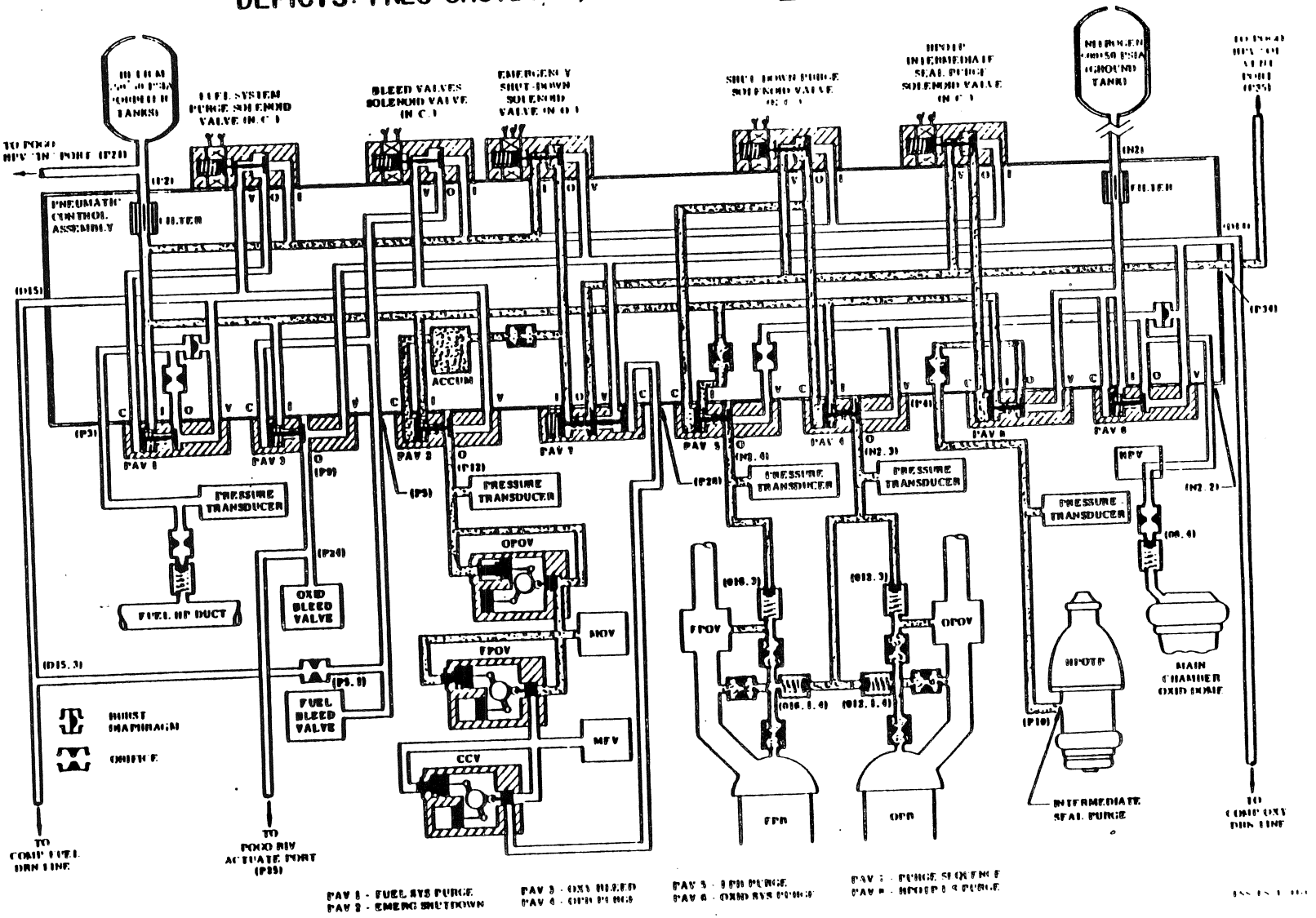


FIGURE 1 - 7.11
(40)

SSME PNEU SCHEMATIC (12 OF 12)

DEPICTS: PNEU SHUTDOWN; PROP VALVES CLOSED, PURGES OFF

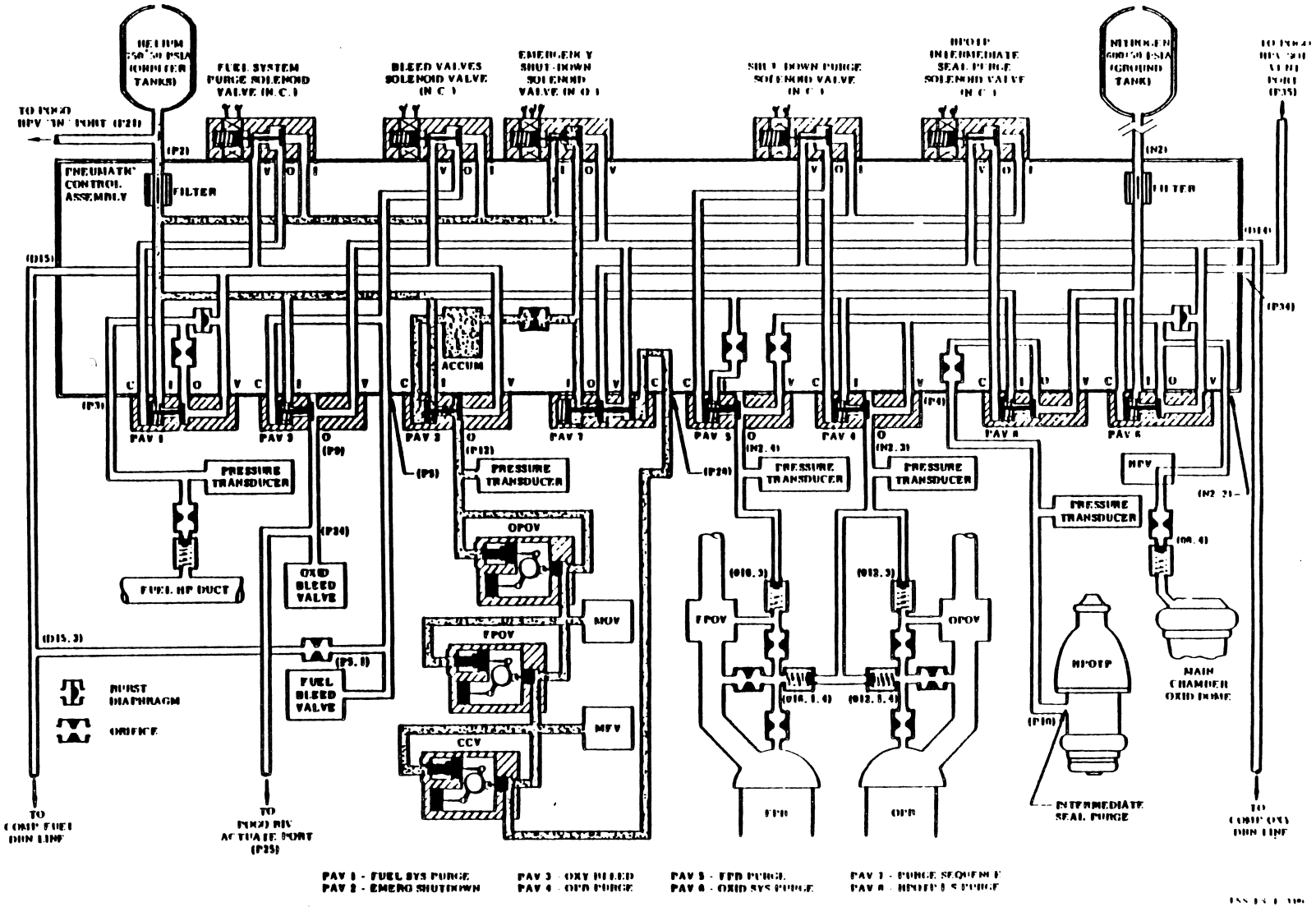


FIGURE 1 - 7.12
(41)

The ASI combustion chamber hot gases discharge into the MCC and preburner combustion chambers to ignite the main propellants. The ignition system produces a continuous supply of hot gas throughout the engine duty cycle, although the electrical energy source is removed within 3.5 seconds after engine start.

Figure 1-8 is a diagram showing the location of the SSME igniters.

1.3.4 Engine Sensors

In addition to the muscle elements (turbines pumps, valves, and igniters) the SSME also contains a large number of sensor elements these sensor elements are used to monitor the engine's condition.

1.4 Space Shuttle Main Engine Controller (SSMEC) General Description.

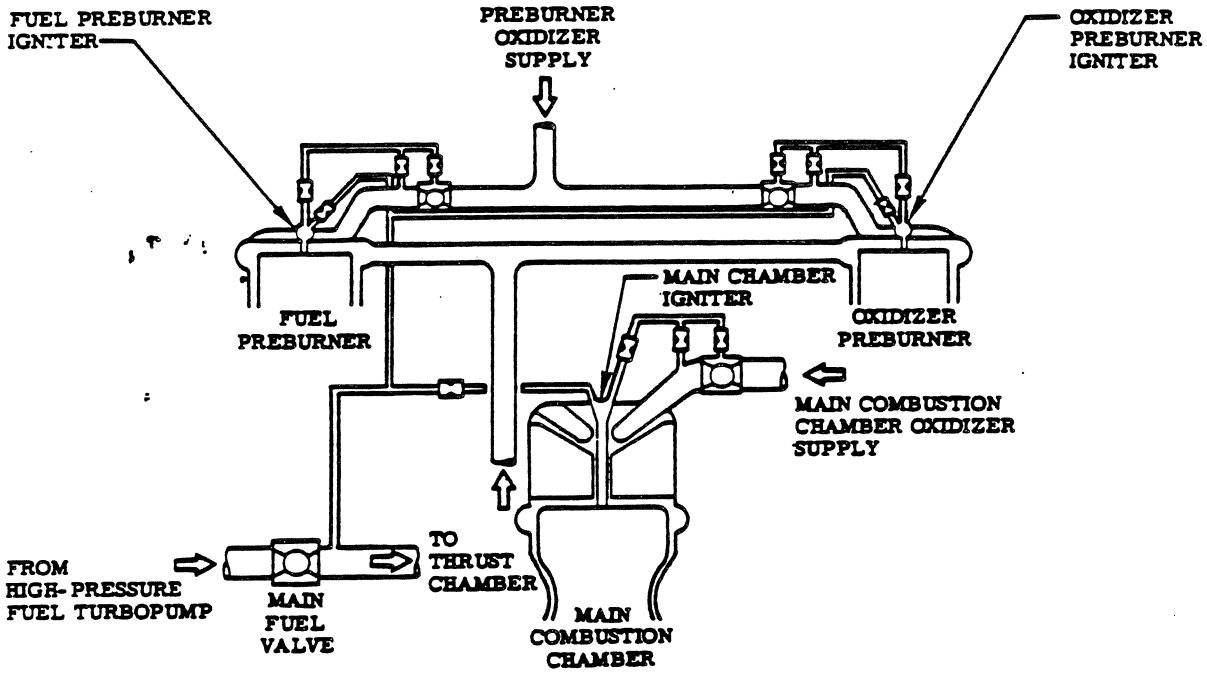
For the sensors to define the SSME's condition and the valves to effectively control the SSME there must be some form of intelligence to read the sensors and issue command to the valves. The SSME controller (SSMEC) provides that intelligence for the main engine.

The SSMEC does virtually the same thing for the SSME that the new computerized ignition system does for the family car. The SSMEC measure engine temperatures, pressures, shaft speed, and fluid flow and adjust the fuel and oxidizer input in the combustion chamber to produce the desired thrust in the most efficient manner.

1.4.1 SSMEC Function

The SSMEC's function is to operate in conjunction with the SSME sensors, the five hydraulically actuated propellent valves and the control software to:

a. Control Engine Start Sequencing
b. Control Engine Thrust
c. Control Engine Shutdown
d. Conduct Run-In Engine Monitoring
e. Receive Vehicle to Engine Commands
f. Transmit Engine Status to the Vehicle
g. Conduct Pre-Launch Engine Check-Out



SSME IGNITER LOCATIONS

FIGURE 1 - 8
(43)

1.4.2 SSMEC Organization

The SSME Controller is organized into five dual redundant functional sections. Figure 1-9 is a block diagram of the controller with five sections. The function of each of these sections is:

a. Input Electronics (IE) - Receives data from the engine sensors in the form of analog signals (resistance, voltage levels, or pulse trains) and converts them into digital words. The input electronics then stores these words in the input electronics dual port memory (IEDPM) which is addressable by the digital computer unit.

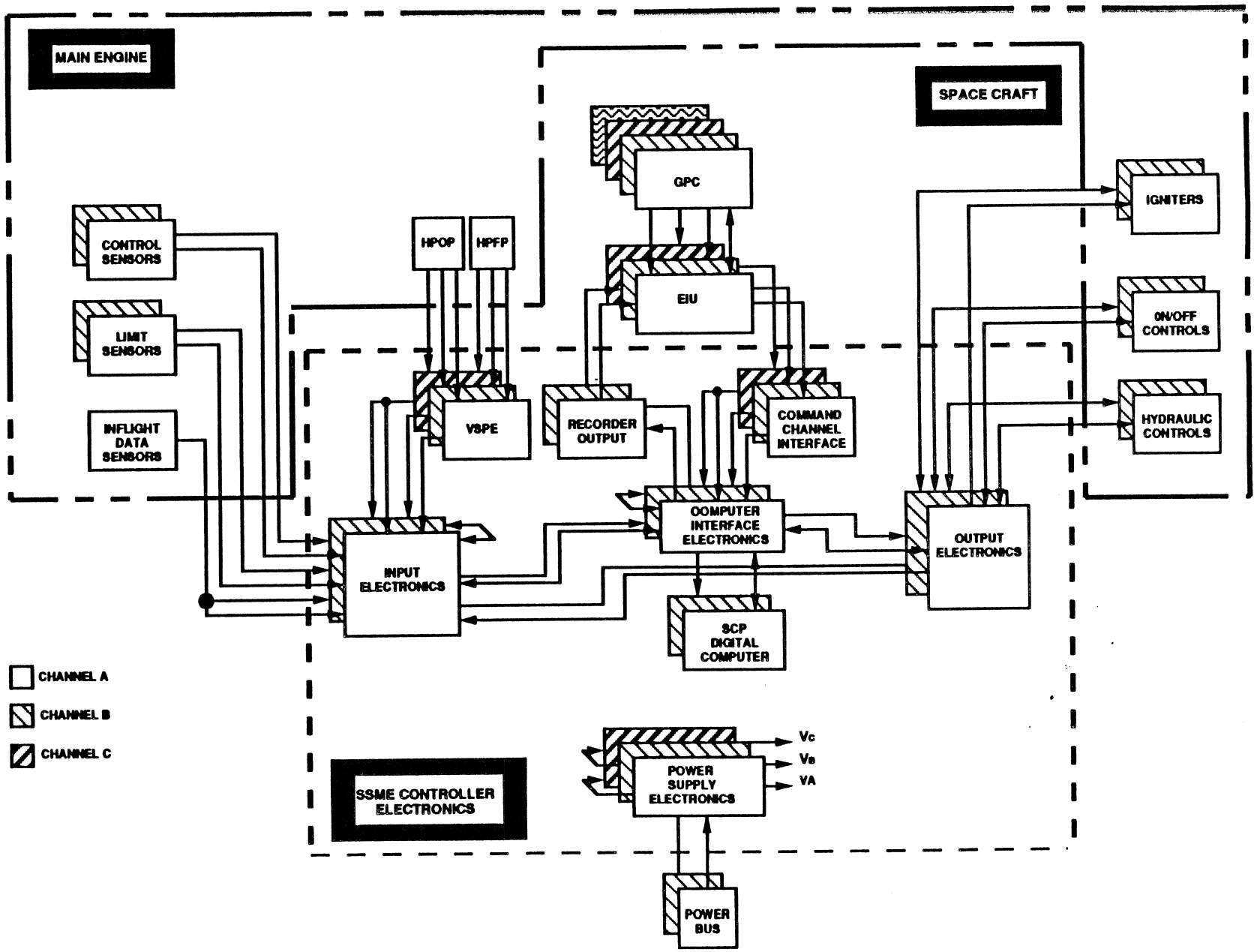
b. Computer Interface Electronics (CIE) - Controls the flow of data between the input electronics, the output electronics and the digital computer unit. The computer interface electronics also controls the flow of data between channels in the controller and the flow of command from the vehicle and data to the vehicle.

c. Digital Computer Unit - Performs the engine control computations based on vehicle command and sensor data from the input electronics and issues control signals to the output electronics. The computer also stores engine. data until requested by the vehicle, conducts test of the engine control system components, the input electronics, the computer interface and the output electronics every major cycle (20 milli seconds).

The digital computer unit s a self-checking pair (SCP)computer unit. This self-check pair unit contains two identical processors and memories operating in lock-synch with each other. Every input of output bus transfer of these two computers is bit by bit compared and the channel is shut down when a mis-compare is noted.

d. Output Electronics - Converts computer digital control signals to voltages and/or currents suitable for operating the engine igniters, actuators and On/Off controls.

e. Power Supply Electronics - Converts the vehicle supplied 3 phase 115VAC 400Hz power in to the procession D.C. and A.C. voltages required to run the controller and activate the engine sensors, igniters, actuators and On/Off controls. The power sequencing logic which assures an orderly turn-on and turn-off of the system is also considered a part of the power supply electronics.



(45)

SSME CONTROLLER ORGANIZATION

FIGURE 1- 9

1.5 Flight Software

The control of the order of sequence of events that the SSMEC goes through to check out, start, run and shutdown a main engine is accomplished by the Flight software program.

The Flight software for the SSMEC Blk II is being generated by Rocketdyne with support by Honeywell. The flow diagram of a typical main engine start, run, and shutdown sequence is shown in Figures 1-10.1 through 1-10.15.

2.0 Requirements

2.1 Programmatic Requirements

The Controller system design must be fail-operate/fail-safe.

Fail-operate means after the first failure the Controller must continue to maintain the required controller and engine performance.

Fail-safe means after a second failure the Controller must continue to control the engine to a safe condition which can include:

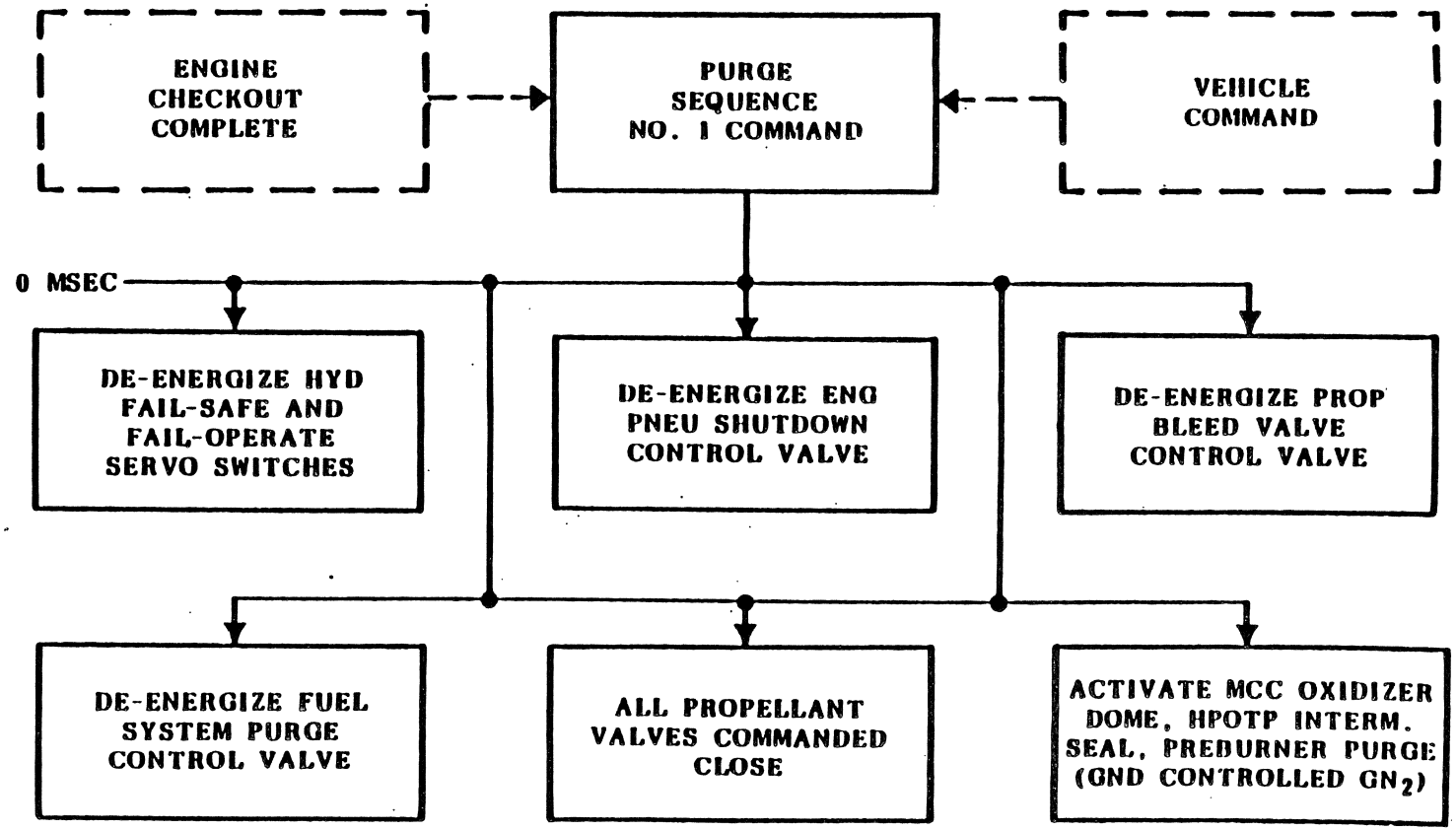
- Continued engine operation
- Hydraulic shutdown of the engine
- Pneumatic shutdown of the engine

These requirements drove the system architecture and detail design. Failure modes effects analysis have been and continue to be conducted on the design. The analysis are aimed at finding single point failures, hazards, and violation of requirements in the design where:

- A Single Point Failure is defined as single controller failure that could cause engine shutdown after solid rocket booster ignition (SRB) and prior to normal engine shutdown. The failure may be detectable by BITE, self-test, or ground checkout but is not limited to those failures detectable by this testing. In defining Single Point Failures, it is valid to combine the failure with one ground checkout, self-test, or BITE testing (one or more undetected failures can be combined). It is not valid to combine the failure with another previously undetected failure that becomes detectable due to a power transient. Ground checkout and self-test tests are defined in the Honeywell Hardware/Software Interface specification DSYG8991A1.

START PREPARATION - PURGE SEQUENCE NO.1

(NOMINAL DURATION: 4 MINUTES)



LSS-ES-T-93C

FIGURE 1 - 10.1
(46)

START PREPARATION - PURGE SEQUENCE NO.2

(NOMINAL DURATION: 3 MINUTES)

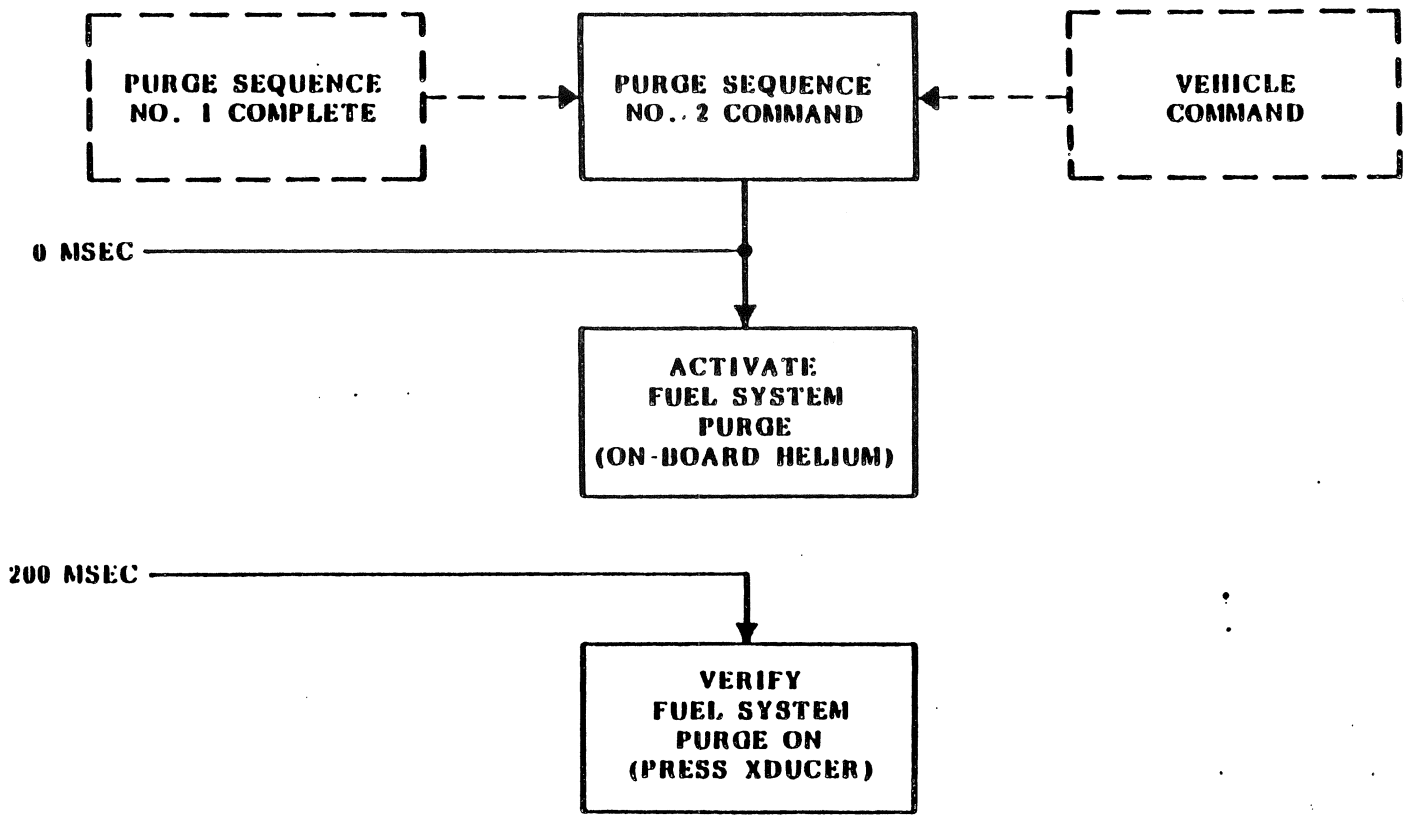


FIGURE 1 - 10.2

(47)

START PREPARATION - PURGE SEQUENCE NO.3

(NOMINAL DURATION: 57 MINUTES)

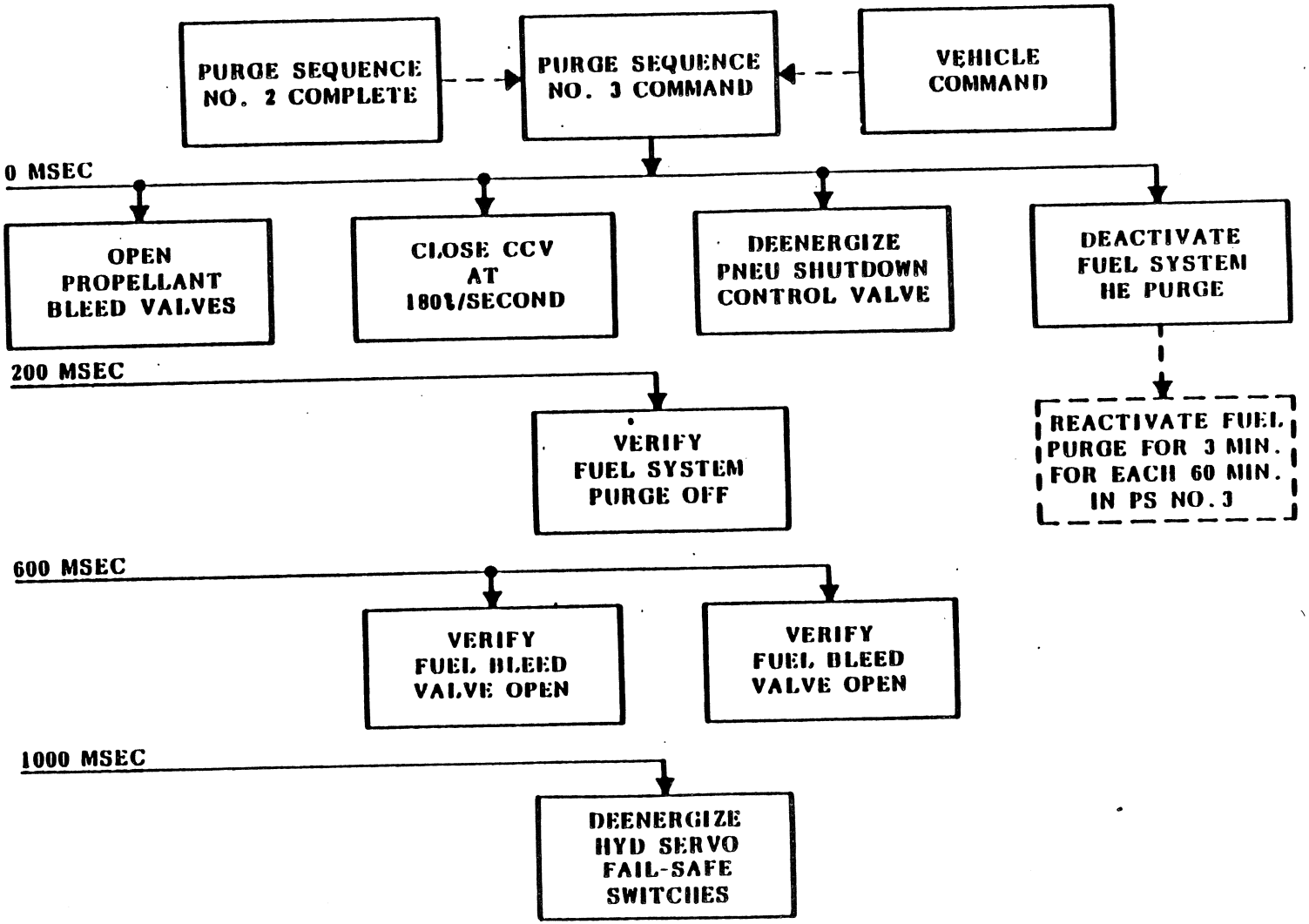


FIGURE 1 - 10.3 (48)

START PREPARATION - PURGE SEQUENCE NO.4

(NOMINAL DURATION: 3 MINUTES)

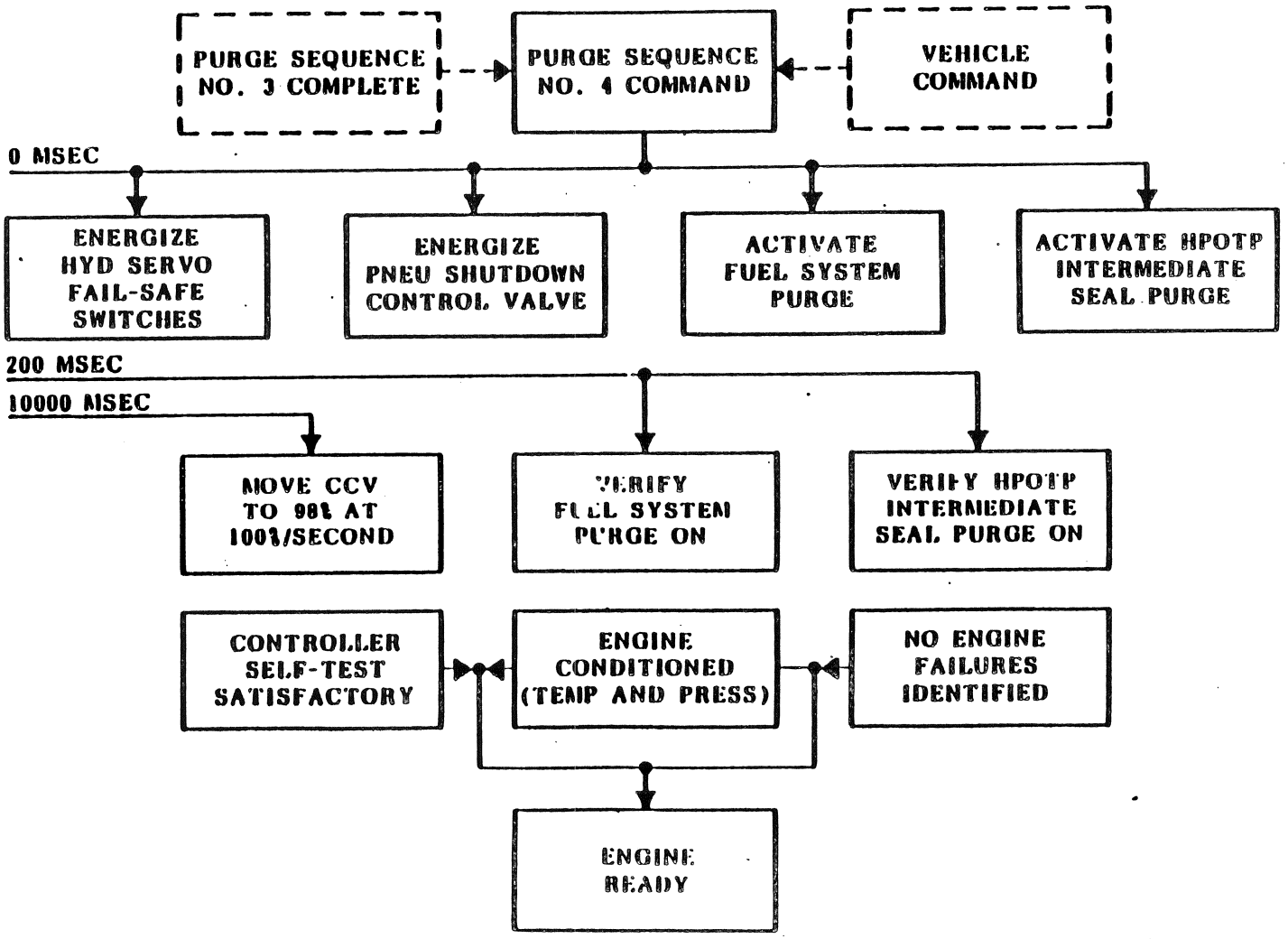


FIGURE 1 - 10.4

SSME START PHASE MODES

- START PHASE: OPERATIONS FOR ENGINE STARTING AND FIRING ARE IN PROGRESS, BEGINNING WITH SCHEDULED (OPEN-LOOP) OPERATION OF PROPELLANT VALVES.

  - START INITIATION MODE: INITIAL FUNCTIONS ASSOCIATED WITH START SEQUENCE ARE IN PROGRESS. THESE INCLUDE ALL FUNCTIONS PRIOR TO IGNITION CONFIRMED, AT 2300 MSEC. ALL PURGES OFF AND VERIFIED. BLEED VALVES CLOSED AND VERIFIED. IGNITERS ENERGIZED AND VERIFIED. THRUST CONTROL LOOP IS CLOSED.

  - THRUST BUILDUP MODE: IGNITION HAS BEEN DETECTED BY MONITORING MAIN COMBUSTION CHAMBER PRESSURE AND CLOSED-LOOP THRUST BUILDUP SEQUENCING IS IN PROGRESS. MIXTURE RATIO CONTROL LOOP IS CLOSED. POGO SUPPRESSION ACCUMULATOR IS HELIUM PRE-CHARGED FOR 2 SECONDS. MFV, MOV, AND CCV ARE SCHEDULED I/A/W MCC PRESSURE (THRUST).

FIGURE 1 - 10.5

SSME START SEQUENCE (1 OF 3)

(IGNITION PHASE - NOMINAL DURATION: 2.3 SECONDS)

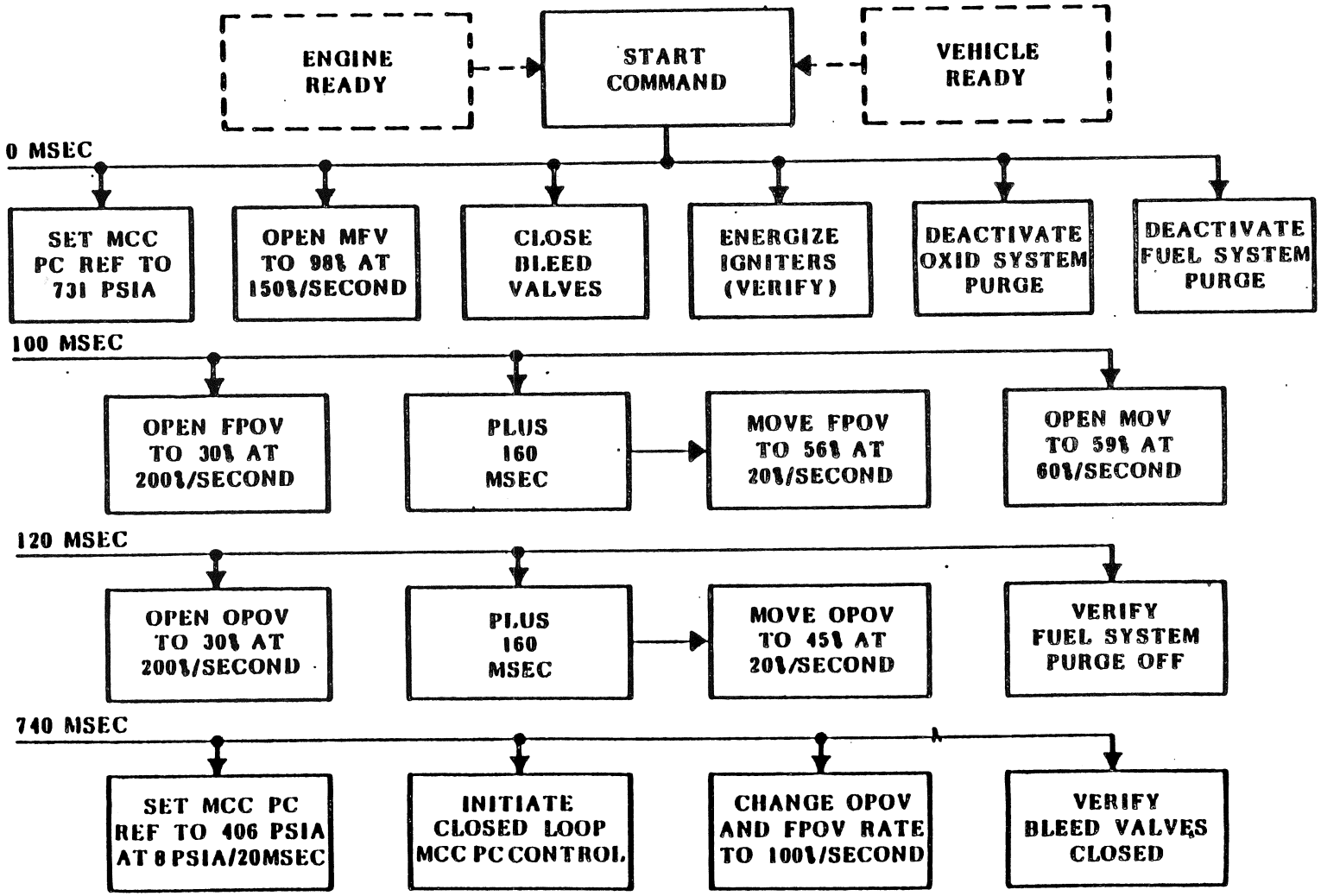


FIGURE 1 - 10.6 (5H) 52

SSME START SEQUENCE (2 OF 3)

(IGNITION PHASE CONTINUED - NOMINAL DURATION: 2.3 SECONDS)

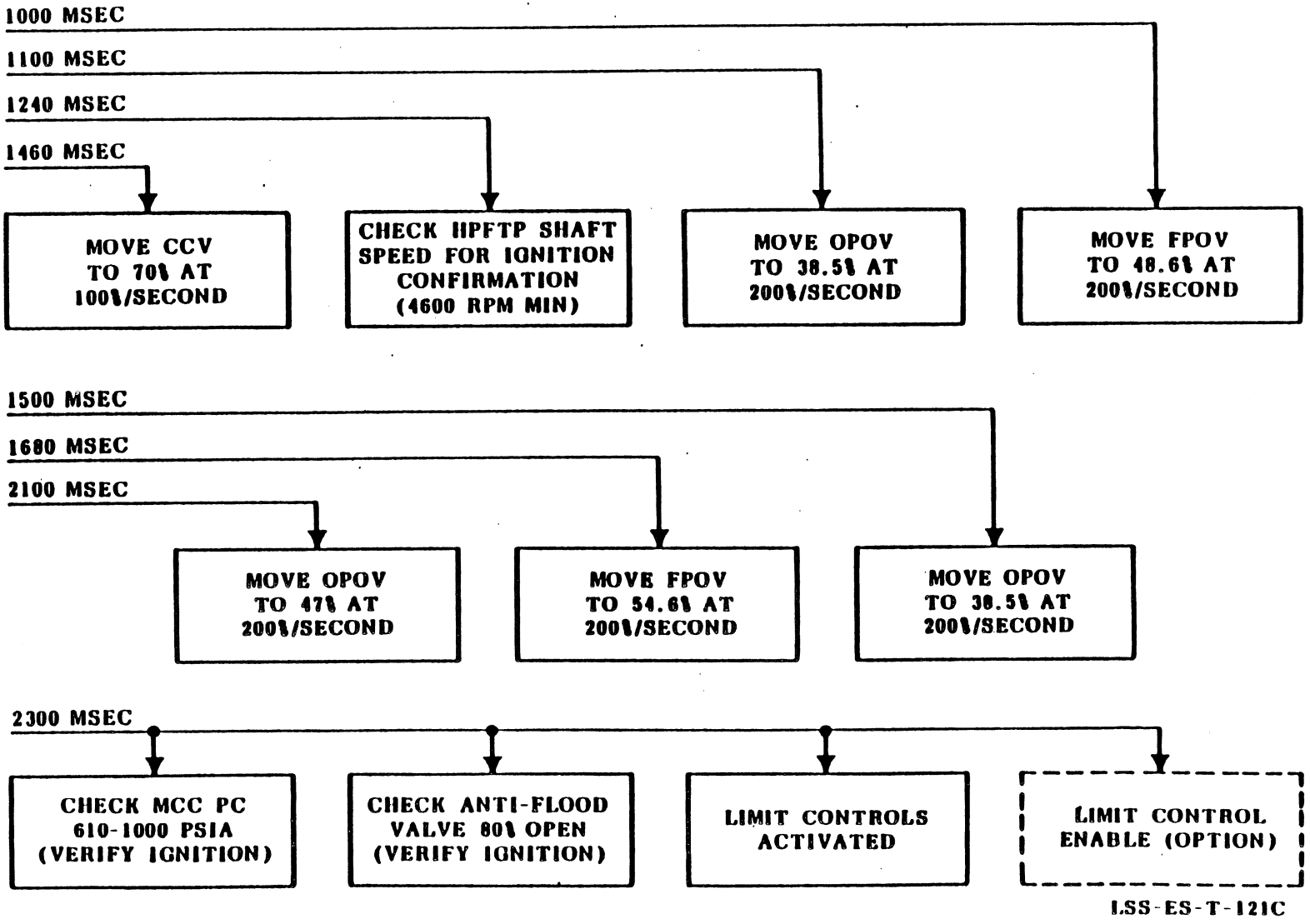
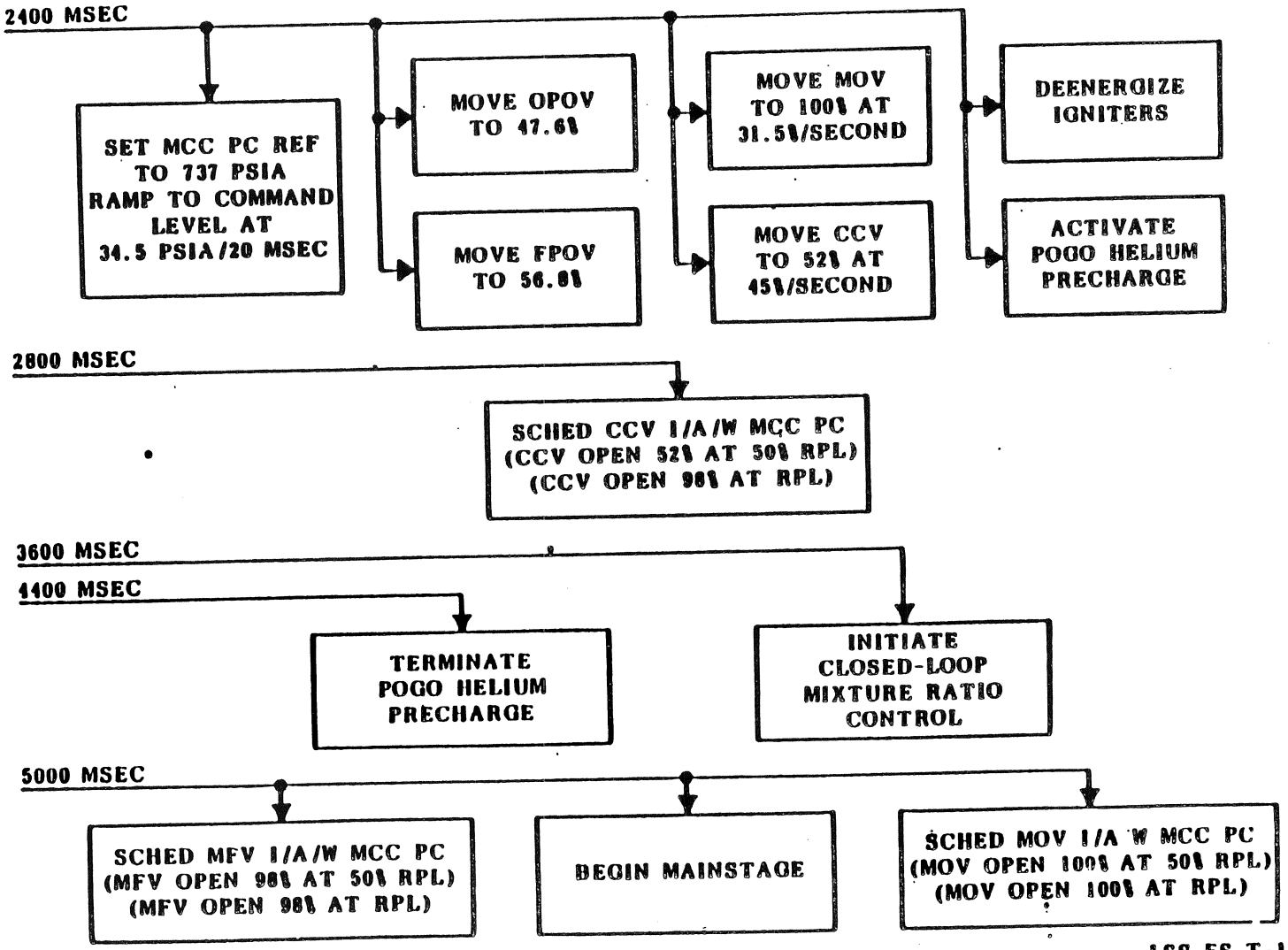


FIGURE 1 - 10.7
(52)

SSME START SEQUENCE (3 OF 3)

(THRUST BUILDUP PHASE - NOMINAL DURATION: 2.6 SECONDS)



LSS-ES-T-122C

FIGURE 1 - 10.8
(53) ص ٤

SSME MAINSTAGE PHASE MODES

- MAINSTAGE PHASE: AUTOMATICALLY ENTERED ON COMPLETION OF START PHASE.

  - NORMAL CONTROL MODE: MIXTURE RATIO CONTROL HAS BEEN INITIATED; THRUST CONTROL IS OPERATING NORMALLY.

  - ELECTRICAL LOCKUP MODE: ENGINE PROPELLANT VALVES ARE ELECTRICALLY HELD IN A FIXED CONFIGURATION AS EXISTED AT INITIATION OF THIS MODE. ALL CONTROL LOOP COMPUTATIONS ARE SUSPENDED.

  - HYDRAULIC LOCKUP MODE: ALL FAILSAFE VALVES ARE DE-ENERGIZED TO HYDRAULICALLY HOLD PROPELLANT VALVES IN A FIXED CONFIGURATION AS EXISTED AT INITIATION OF THIS MODE. ALL CONTROL LOOP COMPUTATIONS ARE SUSPENDED.

FIGURE 1 - 10.9

SSME SHUTDOWN PHASE MODES

- SHUTDOWN PHASE: OPERATIONS TO REDUCE ENGINE MCC PRESSURE AND DRIVE ALL VALVES TO EFFECT ENGINE SHUTDOWN

  - THROTTLING TO MPL MODE: SHUTDOWN IS IN PROGRESS AT A PROGRAMMED SHUTDOWN THRUST REFERENCE LEVEL ABOVE MPL. HELIUM POST-CHARGE IS ACTIVATED.

  - VALVE SCHEDULE THROTTLING MODE: SHUTDOWN IS AT A STAGE IN SEQUENCE WHERE PROGRAMMED THRUST REFERENCE HAS DECREASED BELOW MPL. SHUTDOWN PURGE IS ACTIVATED.

  - PROPELLANT VALVES CLOSED MODE: THE SHUTDOWN SEQUENCE IS IN STAGE FOLLOWING CLOSURE OF ALL LIQUID PROPELLANT VALVES.

FIGURE 1 - 10.10

SSME SHUTDOWN SEQUENCE (1 OF 2)

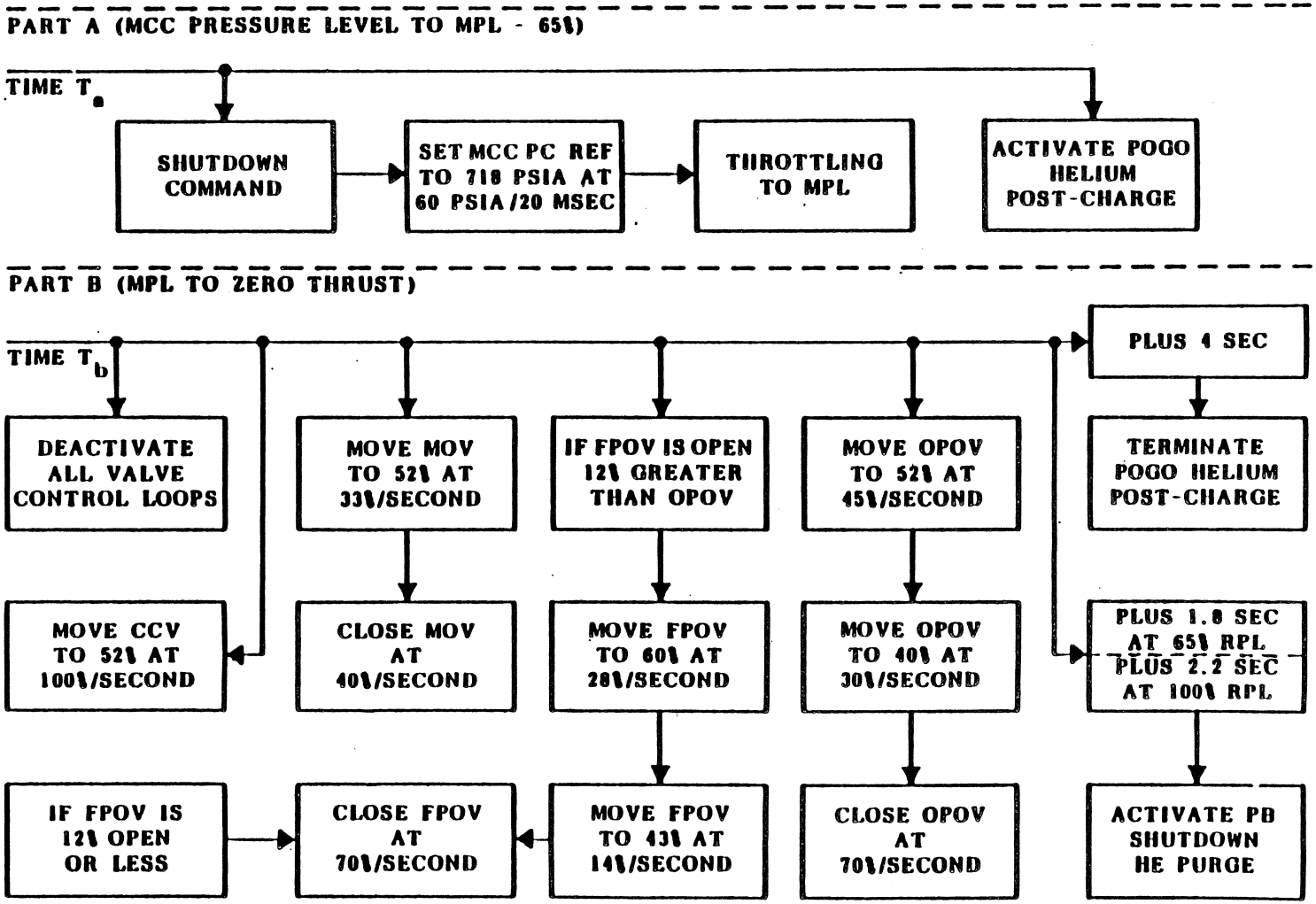


FIGURE 1 - 10.11

SSME SHUTDOWN SEQUENCE (2 OF 2)

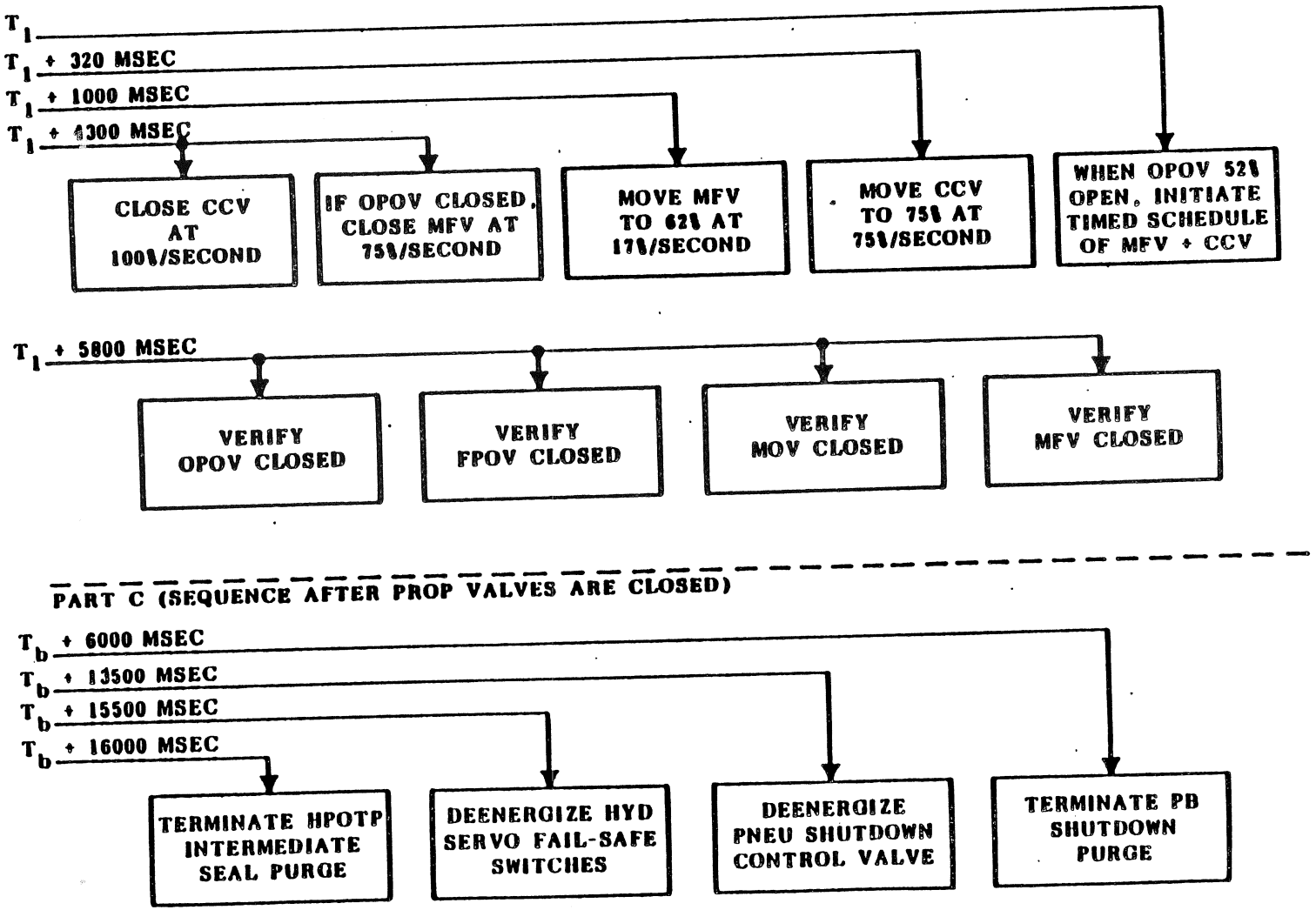


FIGURE 1 - 10.12
(57)

ENGINE SHUTDOWN VALVE SEQUENCE (TYP)

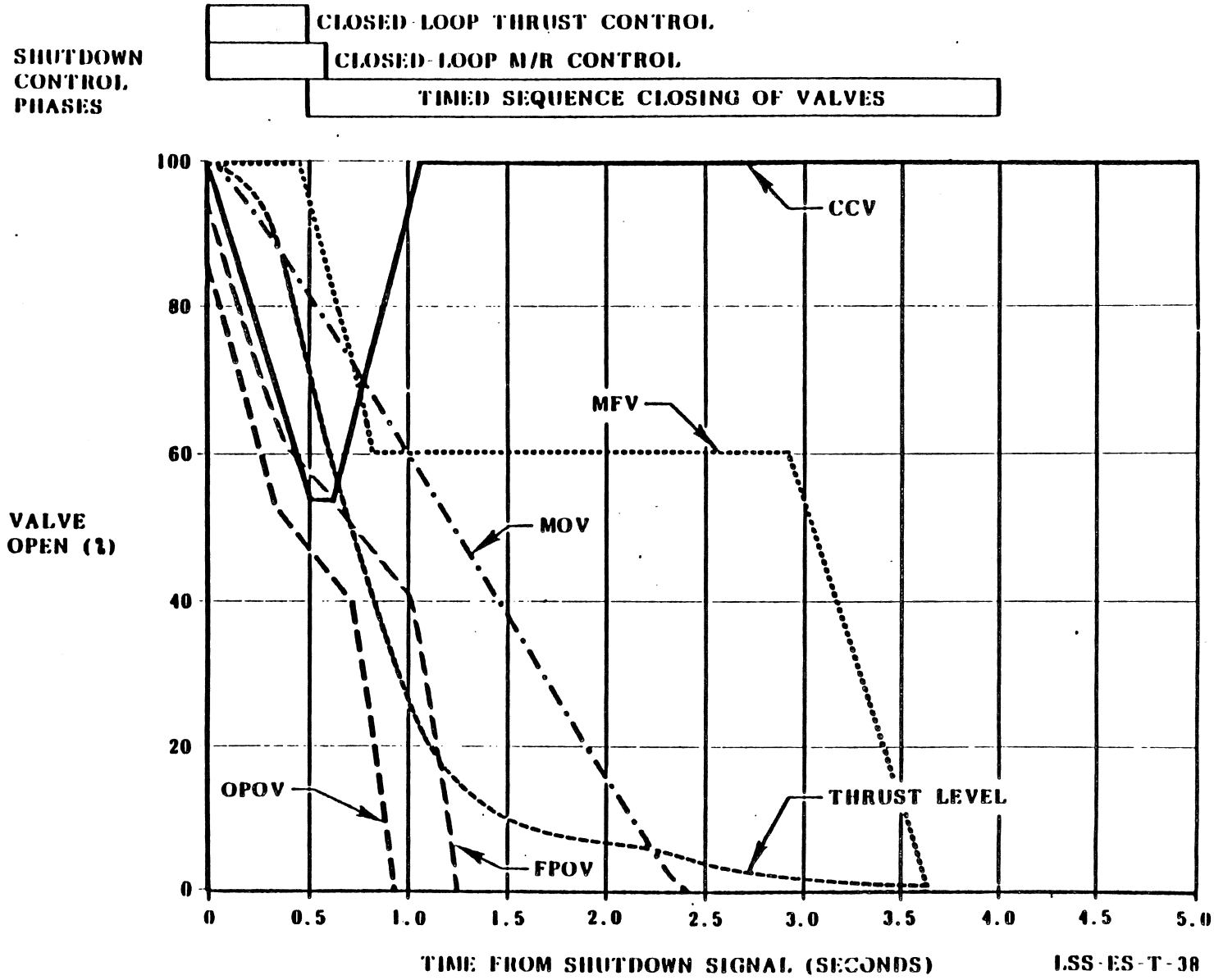


FIGURE 1 - 10.13
(58)

SSME POST-SHUTDOWN PHASE MODES

- POST-SHUTDOWN PHASE: STATE TO WHICH SSME AND MEC GO AT COMPLETION OF ENGINE FIRING.
  - STANDBY MODE: A WAITING MODE OF CONTROLLER OPERATIONS WITH FUNCTIONS IDENTICAL TO THOSE OF STANDBY DURING CHECKOUT. THIS IS NORMAL MODE OF POST-SHUTDOWN ENTERED AFTER COMPLETION OF SHUTDOWN PHASE.
  - TERMINATE SEQUENCE MODE: TERMINATION OF A PURGE SEQUENCE BY A COMMAND FROM VEHICLE IS IN PROGRESS. ALL PROPELLANT VALVES ARE BEING CLOSED, AND ALL SOLENOID AND FAIL-SAFE SERVO SWITCHES ARE BEING DEENERGIZED.
  - ~~OXIDIZER DUMP MODE: OXIDIZER DUMP SEQUENCE BEING PERFORMED.~~
  - FUEL DUMP MODE: FUEL PURGE AND DUMP SEQUENCE ARE IN OPERATION.

FIGURE 1 - 10.14

- A Hazard is defined as a first or second controller failure that could result in erroneous engine control leading to major equipment damage and/or danger to personnel. In defining Hazards, it is valid to combine the failures with a normally recoverable power transient and/or other failures not identifiable by ground checkout, self-test, or BITE testing (one or more undetected failures can be combined). Ground check out and self-test test are defined in the Honeywell Hardware/Software Interface specification DSYG8991A1.

- A Violation of Requirements is defined as a failure that causes a violation of the Fail-Operate requirement for which the controller shall be capable of full operation with the vehicle/engine after the controller has experienced one failure. The Violation of Requirements definition is applicable during start, mainstage (prior to solid rocket booster ignition only), shutdown, and post shutdown phases, but does not create a hazard. The failure may occur after ground checkout and prior to start. In defining Violations of Requirements, it is valid to combine the failure with one recoverable power transient and/or other failures not identifiable by ground checkout, self-test, or BITE testing (one or more undetected failures can be combined). It is not valid to combine the failure with another previously undetected failure that becomes detectable due to a power transient. Ground checkout and self-test tests are defined in the Honeywell Hardware/Software Interface specification DSYG8991A1.

2.2 Rocketdyne Specification

The Baseline Hardware Requirements for the Space Shuttle Main Engine Controller are contained in:

- RC1493 - Procurement Specification; Controller, Space Shuttle Main Engine.

- RC1494 - Interface Control Document, Controller/Engine and GSE.

2.3 Honeywell Requirements

The programmatic and Rocketdyne requirements were combined by Honeywell to produce a set of design and test requirements for the build and test of the SSMEC Blk II. These requirements/specifications are:

o DSHG8977A1	Part I - Hardware Specification
o DSHG8977A1	Part II - Acceptance Test Requirements
o DS34053435	Part I - Power Supply Specification
o DSYG8991A1	Hardware/Software Interface Specification
o DSCP34053987	Computer Acceptance Test Program PT -1 Specification.

2.3.1 Block Diagrams

To further aide in the design of the Controller block diagrams of them major section were generated. These diagrams can be obtained from the print room by ordering:

o	34048832	Controller Assembly Block Diagram
o	34048830	Digital Computer Unit Block Diagram
o	34048828	Computer Interface Electronics Block Diagram.
o	34048829	Output Electronics Block Diagram
o	34048827	Input Electronics Block Diagram
o	34048831	Power Supply Assembly Block Diagram

3.0 Space Shuttle Main Engine Controller Design

3.1 Architecture

The basic architecture of the SSME Controller is shown in Figure 3-1. The Architecture shown is that of a dual redundant system with cross strapping of the converted input signals and of the commands to the output. In this arrangement to avoid conflicting commands to the output, due to the channels not being in sync, only one computer interface is allowed to control the output at any one time. The hardware is designed in a hierarchy with channel "A" in control until it fails. When "A" fails "B" automatically takes over control. When "B" fails the engine is committed to hydraulic lock-up or pneumatic shutdown of the engine.

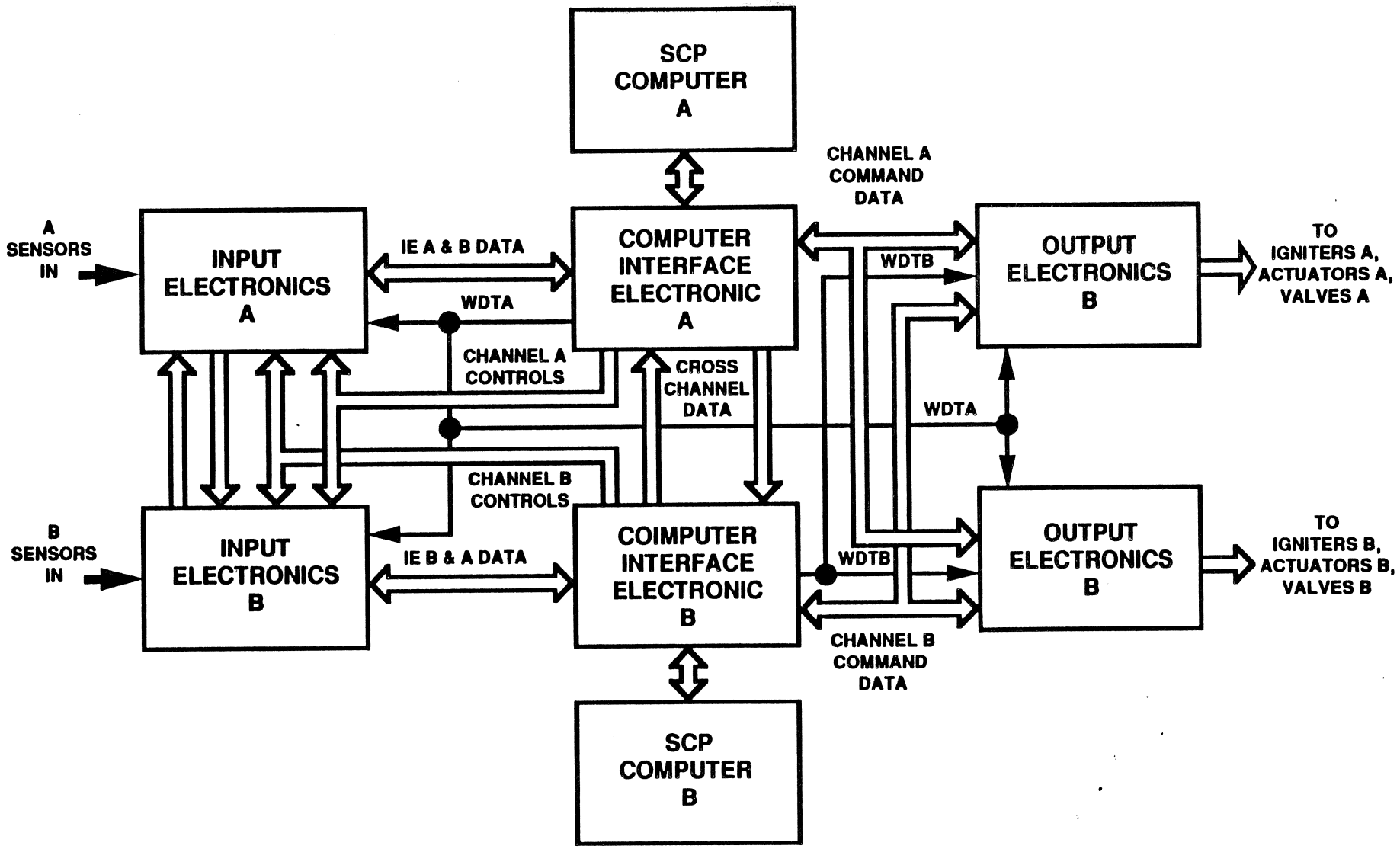
In order to implement this architecture each channel must be able to self test its electronics and software in a manner that will prevent undetected failures. When a failure is detected within a channel that channel must notify the other channel and allow its own Watch Dog Timers to time out. The detection of failures and failure/redundancy management occupy a very large percentage of both the hardware and the software in the SSMEC.

3.2 Interface

The SSME Controller has two interfaces, one with the main engine itself and the other with the vehicle.

3.2.1 Engine Interface

The Controller interfaces with the main engine both physically and electrically.



SSMEC BLOCK II CROSS STRAPING

FIGURE 3- 1

3.2.1.1 Physical Interface

The engines physical interface is through vibration isolators to the Controller's three point mounting system Figure 3-2 shows the mounting points.

3.2.1.2 Electrical Interface

The electrical interface with the engine takes place with the engine sensors, valves and effectors. The quantity of these interfaces are:

SENSOR TYPE	TOTAL QTY	SPARE
Presssure	36	4
Temperature	27	4
Shaft Speed	6	2
Flow Rate	4	-
Accelerometer	6	-
Position	27	12
Spark Feed Back	6	-

Affector Types	Total Qty	Spare
Solenoids	26	14
Servoswitches	18	3
Spark Igniters	6	-

Valve Types	Total Qty	Spare
Servovalves	12	2

3.2.2 Vehicle Interface

The Controller interface with the vehicle is strictly electrical. There are, however, 3 types of electrical interface involved, analog telemetry, digital data, and power.

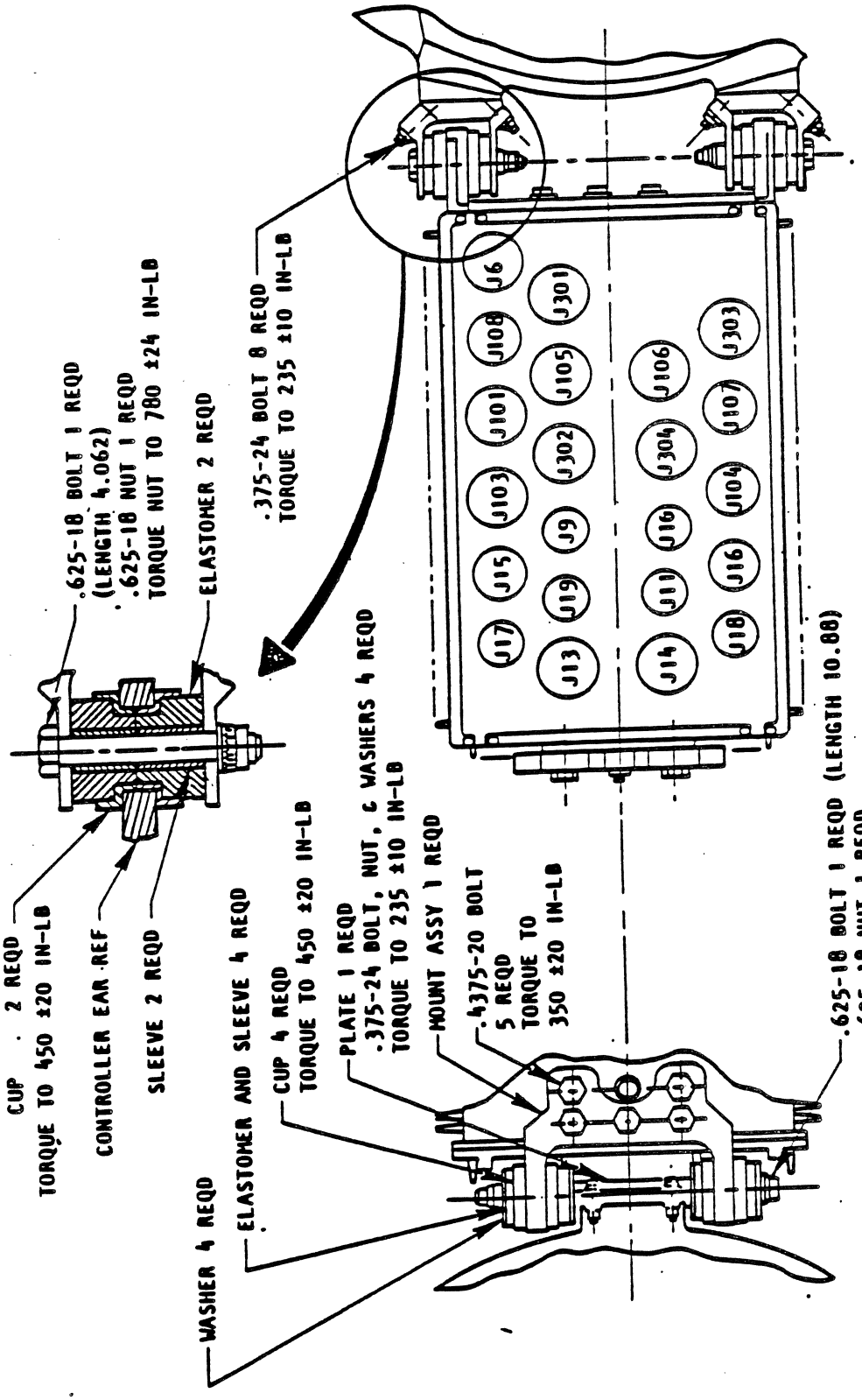
3.2.2.1 Analog Telemetry

The analog interface consists of the output of:

- Controller internal temperature (100 ohms thermistor)
- The amplified and filtered outputs of the six vibration sensors (accelerometers).

3.2.2.2 Digital Data

The Digital Data Interface consists of the Vehicle/Controller Electrical Interface (VEEI) which consists of the Status/Recorder Channel Interface, and the Command/Data Interface.



CONTROLLER SOFTMOUNT CONFIGURATION

FIGURE 3 -2

3.2.2.2.1 Command/Data Interface

The Command/Data Interface is the means by which the Controller receives commands from the vehicle. These commands are received over three independent input channels. Each channel receives the same 31 data bits plus a synch bit which has been transmitted in Manchester B1-Phase code (see Figure 3-3) by the Vehicle Electrical Interface Units (EIU's). The 31 bits are made up of 16 bits of data plus 15 bits of Bose, Chaudhuri, and Hocquenghem (BCH) encoding. For the 16 bits of data to be judged as data or command the Manchester code must contain 31 bits, can not be all zeros and the BCH code must be valid for the 16 data bits.

Once the 16 bits of data are judged to be valid the three channels of data are voted on by Software and two of three must agree for the data to be used by the Controller.

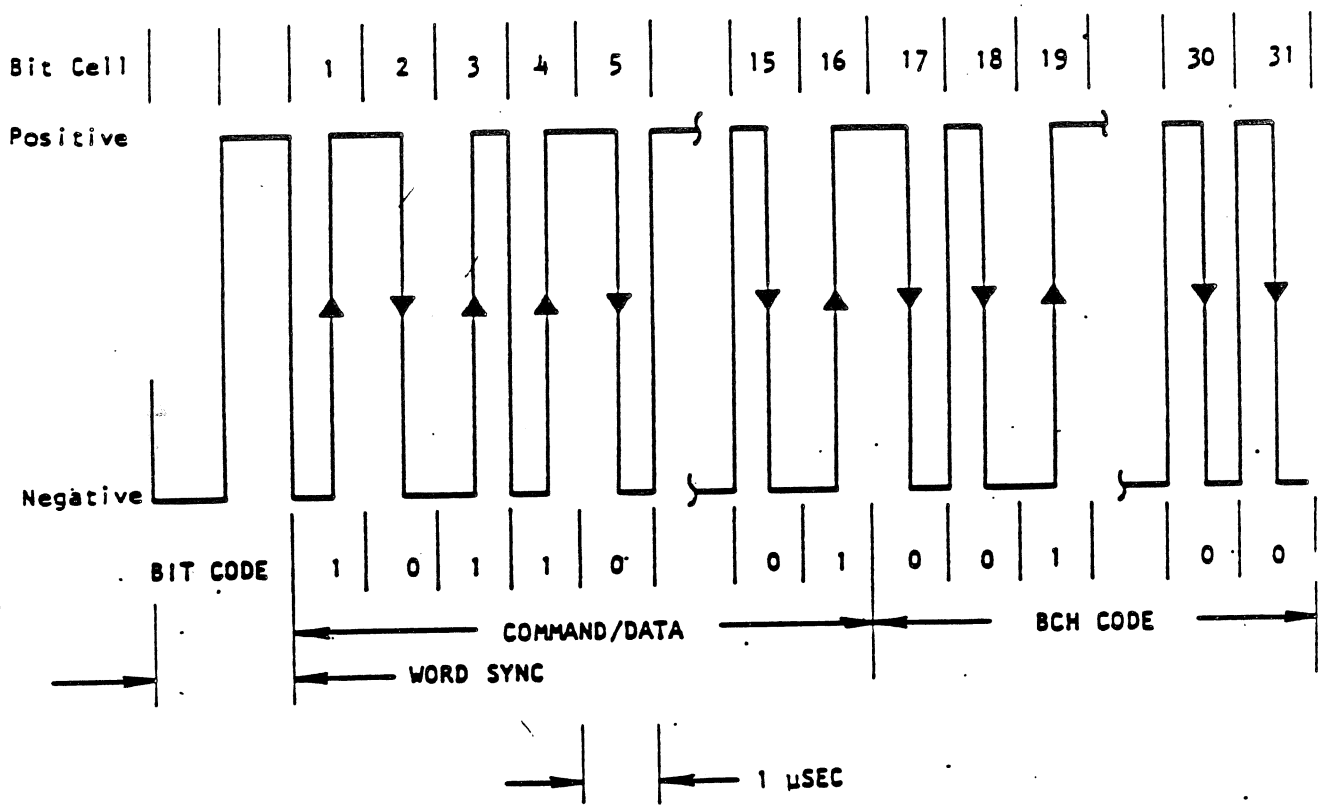
In the special case of the reset channel command the three channels are Software voted and also Hardware voted before the command can be executed. The reset command is used to restart processing after a channel has been halted.

The three controller command channels interface with the quad redundant general purpose computers in the vehicle as shown in Figure 3-4.

3.2.2.2.2 Status Recorder

The Status Recorder has dual channel serial outputs. Each status/recorder channel can send 16 bit plus parity serial words in Manchester code from the Controller to the Vehicle. Each channel can send data from either channel "A" or channel "B" of the Controller. Which channel the data comes from is determined by the channel in control. With both "A" and "B" operating, channel "A" will normally be in control. Channel A can turn the recorder channel control over to "B" without giving up any other controls by issuing a specific command and it can resume control with another command channel "B" can only get control when "A" has relinquished control. Both Controller channels "A" and "B" have independent 128 word dual port memories dedicated to holding the recorder data words. These memories are updated by the Controller's computers once every major cycle. The status/recorder sends its data out in 128 word blocks.

Figure 3-5 defines the status/recorder data bit pattern. Figure 3-6 shows how the two channels of telemetry data from each of the three main engines is sent to the four general purpose computer in the vehicle.



NOTE: (1) Manchester bi-phase level "one" represented by a positive transition in center of the Bit Cell, "zero" is represented by a negative transition in the center of Bit Cell.

(2) Bit Cell 1 is the most significant bit and is the first bit received by the controller.

(3) The Vehicle Command signal transition with respect to the Vehicle Command Return signal shall be from negative to positive for a Manchester bi-phase level "one" and from positive to negative for a Manchester bi-phase level "zero" during a bit cell period.

COMMAND/MEMORY DATA WORD

FIGURE 3 -3

GPC / SSME COMMAND DATA FLOW

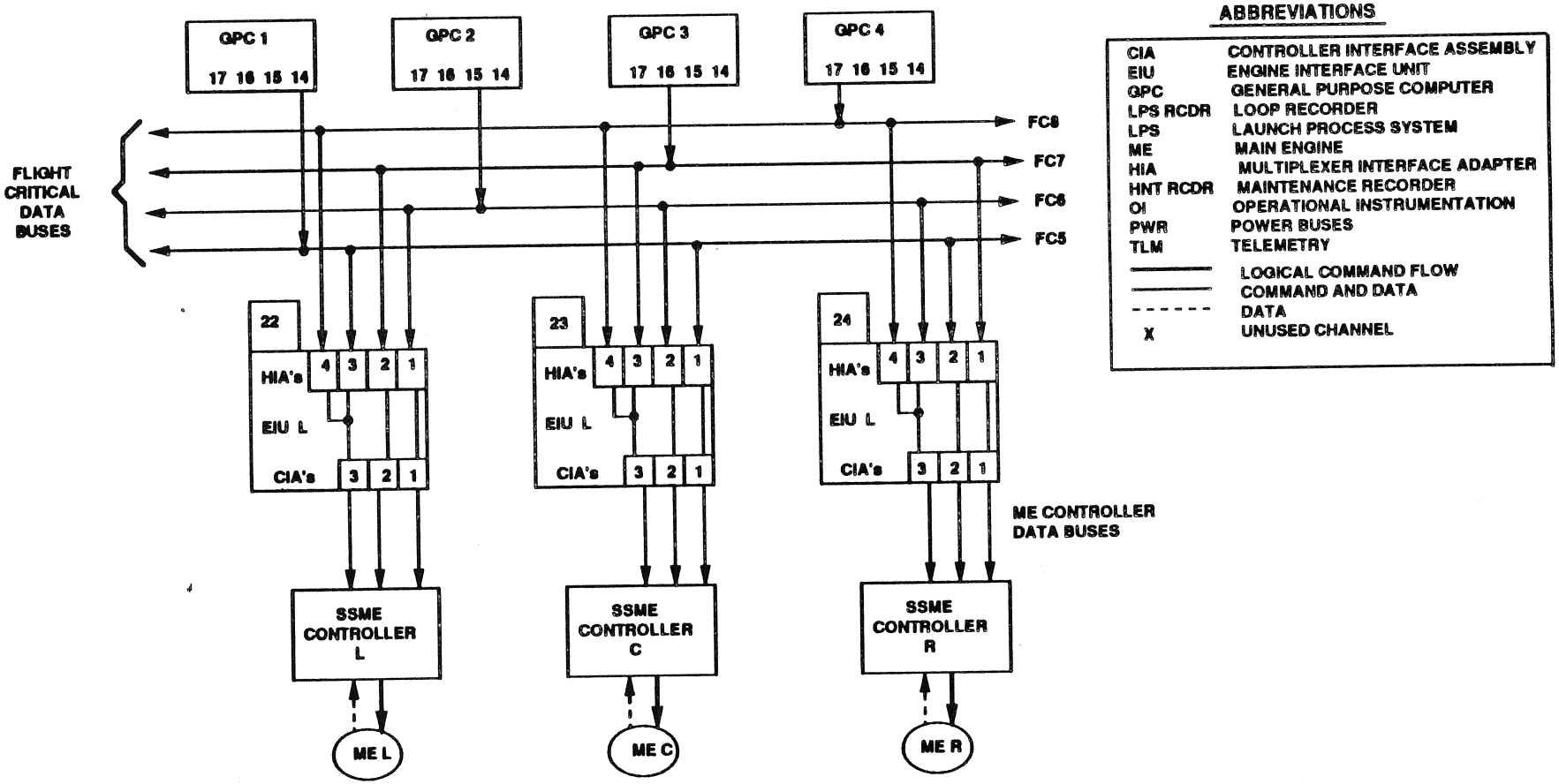
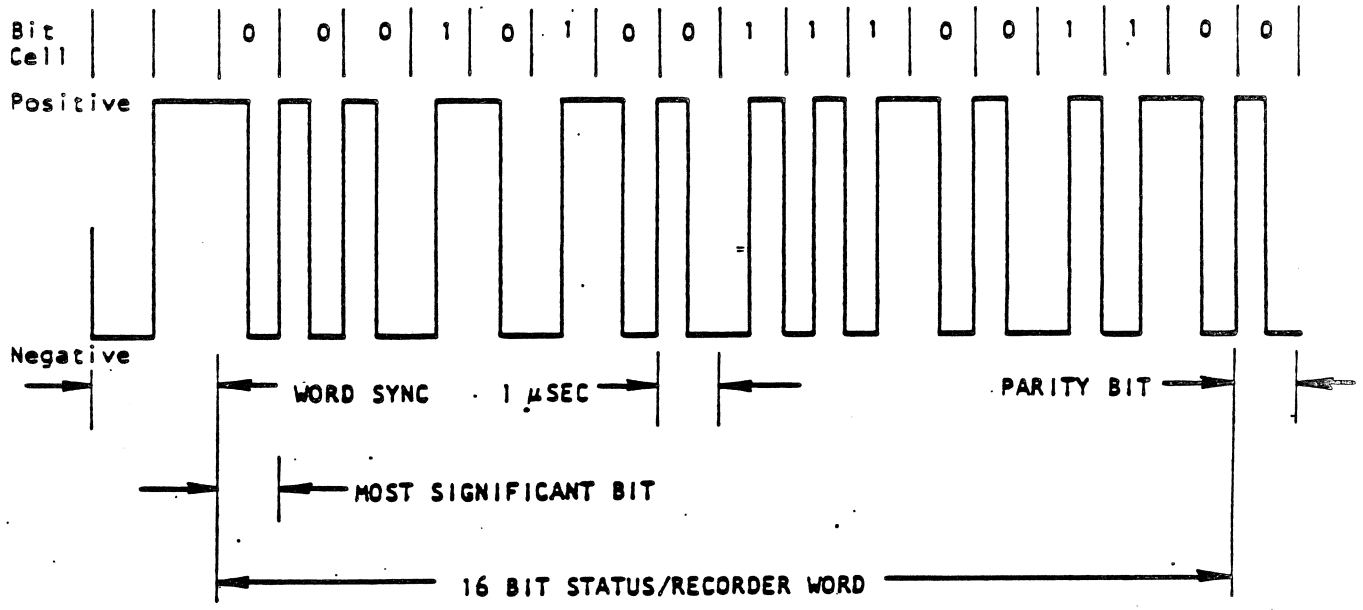


FIGURE 3 - 4



NOTE: (1) Manchester bi-phase level "one" represented by a 10, "zero" is represented by a 01.

(2) Most significant bit is the first bit transmitted by the engine.

(3) The Status/Recorder Data signal transition with respect to the Status/Recorder Data Return signal shall be from negative to positive for a Manchester bi-phase level "one" and from positive to negative for a Manchester bi-phase level "zero" during a bit cell period.

STATUS/RECORDER WORD

FIGURE 3-5

GPC / SSME TELEMETRY DATA FLOW

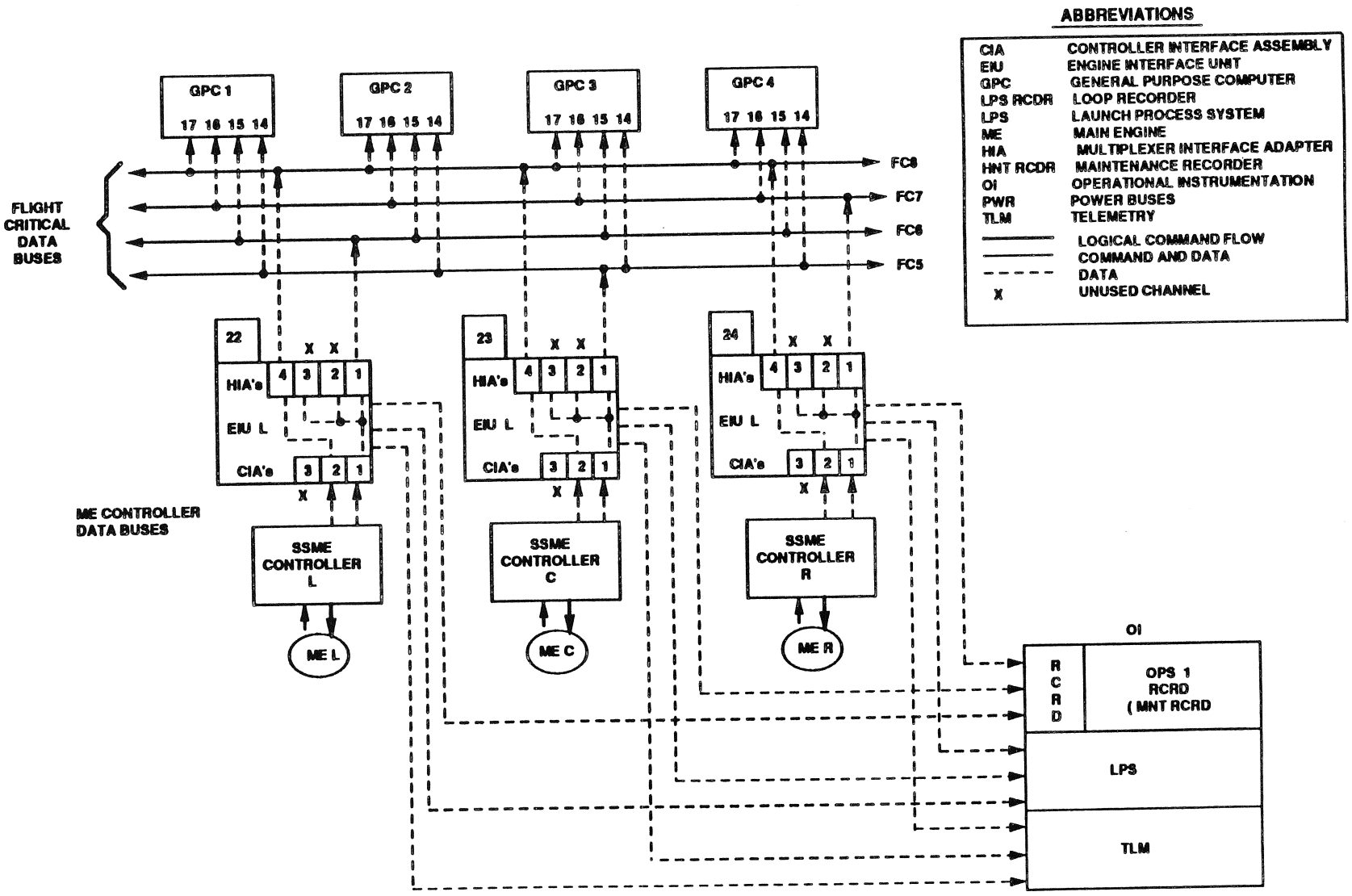


FIGURE 3 - 6

3.2.2.3 Power

The Vehicle sends the Controller dual redundant A.C. and dual redundant D.C. power.

3.2.2.3.1 A.C. Power

The Vehicle supplies each Controller with two independent 115VAC phase 400Hz power sources. The Controller converts these A.C. sources to the D.C. voltages required by the controller electronics and the voltages required to drive the engine valves and effectors. At least one A.C. source must be applied to the Controller to control the engine. The controller typically requires a little more than 200 watts per channel and has a worst case load of 350 watts per channel. A typical A.C. power hook-up is shown in Figure 3-7.

3.2.2.3.2 D.C. Power

In addition to the A.C. power the vehicle also supplies two independent 28 volt D.C. power sources to the Controllers. The 28VDC is only used to produce a back-up +5VDC source for the MC6800 processors, the RAM main memory and the failure dta recorder RAM memory. The Controller can not control an engine with only 28VDC supplied. The +28VDC is used to keep vital parts of the of the system alive during 115VAC power drop-outs. The 28V must be on and remain in specification during A.C. power transients for the Controller to execute a power recovery from an A.C. transient. If the 28V is not on or fails during an A.C. transient the Controller will not recover from the transient. The Controller will draw from 25 to to 37 watts from the 28VDC when the A.C. is off. The Controller will draw from 3 to 5 watts from the 28VDC when the A.C. is on.

3.2.2.3.3 Other Power

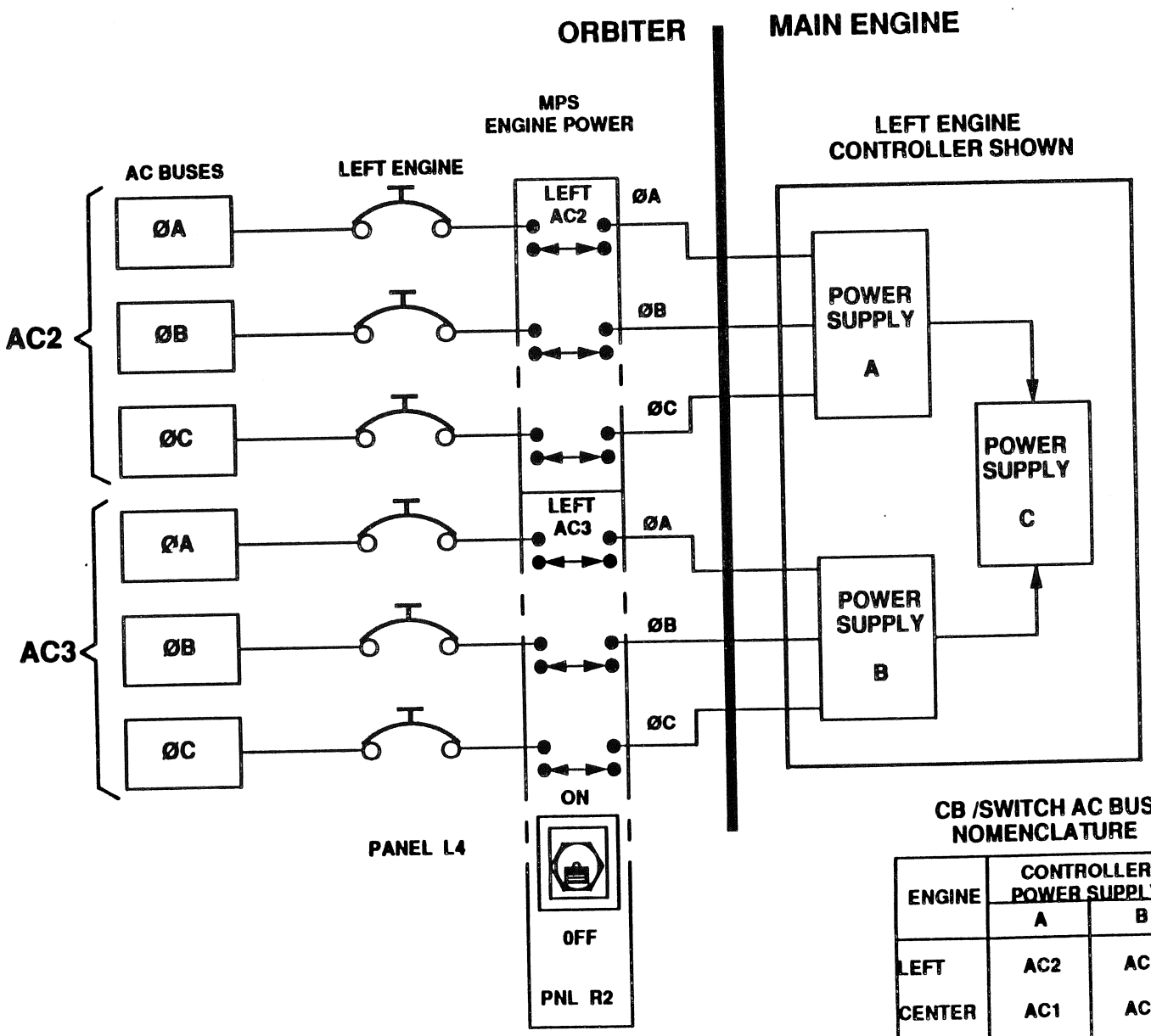
Provisions have been made in the Controller to connect an external battery to the Controller in order to hold-up the main RAM memory during shipment or total power-off conditions.

To maintain the RAM memories data requires no more than 6.4 milli amps at 2.8 to 4.0 VDC per channel.

There are two connection points per channel for the batter and they are:

- J302 - Pins 109-112 for Channel A
- J304 - Pins 109-112 for Channel B
- J3 - Pins A & B for Channel A
- J4 - Pins A & B for Channel B

MAINE ENGINE CONTROLLER POWER



CB /SWITCH AC BUS NOMENCLATURE

ENGINE	CONTROLLER POWER SUPPLY	
	A	B
LEFT	AC2	AC3
CENTER	AC1	AC2
RIGHT	AC3	AC1

FIGURE 3 - 7

(72)

3.3 Digital Computer Unit (DCU)

The Block II Digital Computer Unit is composed of two major functional blocks. These blocks are the self checking pair processor and the replicated memory. Figure 3-8 shows how the five printed wiring boards that make-up the digital computer unit are interconnected. The major point of this diagram is that each half of the Self Checking Pair Processor (SCP-P) has its own independent 64K words of memory with which to operate.

The digital computer unit can address over 8 million words of memory directly. Although the SSME Controller has only 64 thousand words of memory. With the large unused memory address field available the SSMEC DCU is designed with Memory Addressed Input Output. This means that each input/output function is handled just like a memory word and that special I/O handling functions are not needed. Figure 3-9 is a map of how the memory words are allocated. The DCU's functions are:

- Processes data received from engine sensors
- Processes commands received from the vehicle
- Performs engine control computations
- Performs engine monitoring computations
- Performs engine checkout computations
- Issues commands to engine control devices

3.3.1 Self Checking Pair Processor (SCP-P)

The Self Checking Pair Processor Printed Wiring Assembly (PWA) is shown in block diagram form in Figure 3-10. The diagram shows the major functional areas of the self checking pair processor assembly.

3.3.1.1 MC68000 Processors

Two MC68000 Micro Processors are the heart of the self checking pair processor. Each MC68000 is a 16 bit micro processor that operates at an 8 megahertz rate and has a 23 bit address field.

3.3.1.2 Clock Oscillator

The processor clock oscillator is a 16 megahertz crystal control oscillator that is divided by 2 to produce an 8 megahertz square wave clock. This 8 megahertz clock drives both halves of the self checking pair to keep them in synch. The processor clock also drives the real time clock generator in the Computer Interface Electronics.

BLOCK DIAGRAM OF THE 5 BOARD DIGITAL COMPUTER UNIT

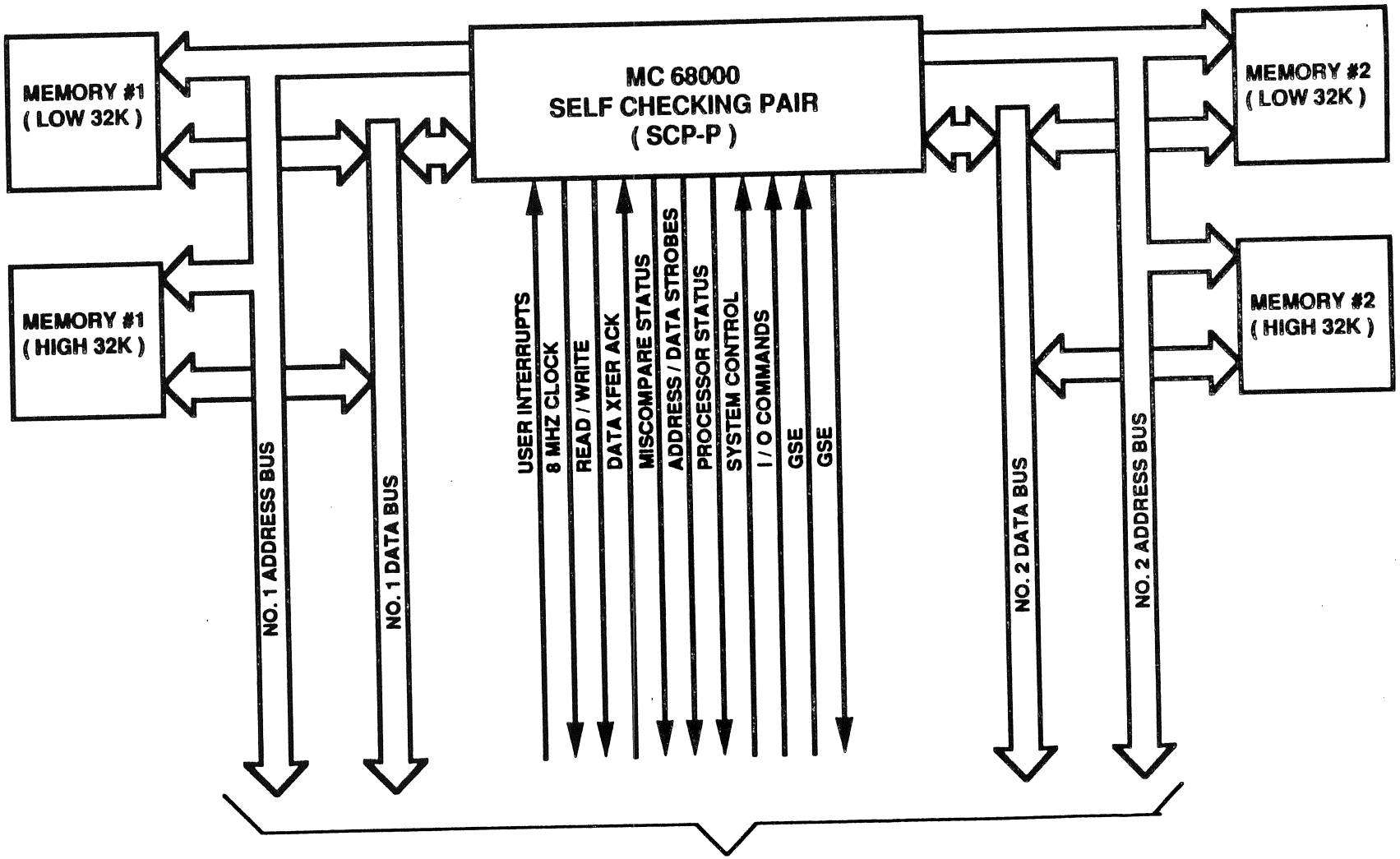


FIGURE 3-8

DCU ADDRESS SPACE

WORDS	EVEN BYTE		ODD BYTE	BYTES
32,768	FFFFFE	SRAM	FFFFFF	65,536
	FF0000		FF0001	
	FEFFFE		FEFFFF	
4,093,952		UNUSED		8,187,904
	821000		821001	
2,048	820FFE 820000	I.O.	820FFF 820001	4,096
63,488	81FFFE	UNUSED	81FFFF	126,976
	801000		801001	
2,048	800FFE 800000	PROM	800FFF 800001	4,096
	7FFFFE		7FFFFF	
4,161,536		UNUSED		8,323,072
	010000		010001	
32,768	00FFFE	SRAM (VECTORS	00FFFF	65,536
	000000		000001	

FIGURE 3-9

SIMPLIFIED SCP-P DIAGRAM

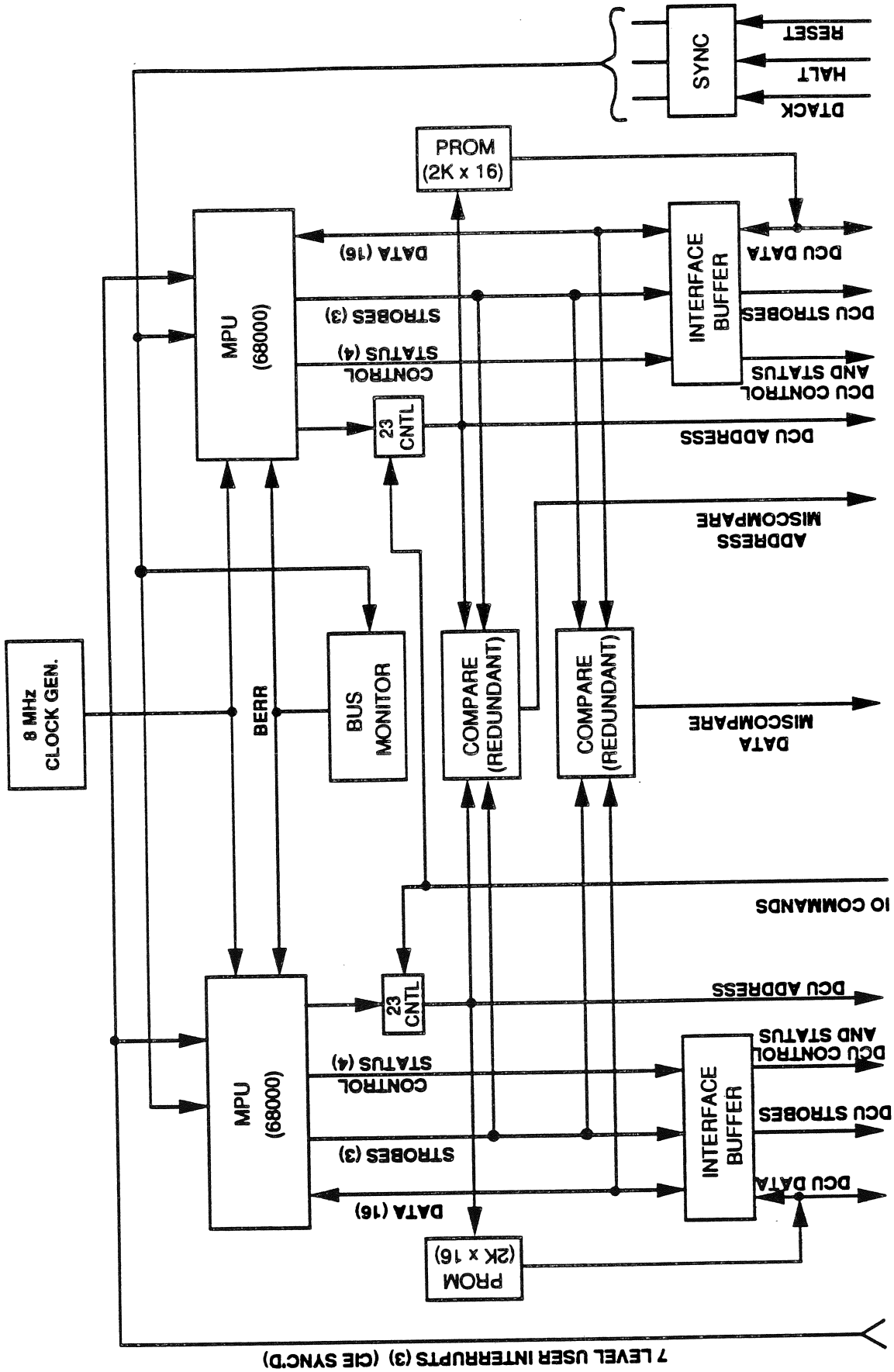


FIGURE 3 - 10

3.3.1.3 Sync Circuit

The Processor Sync Circuit takes the asynchronous DTack, Halt and Reset signals and synchronizes them with the processor clock before they are applied to both halves of the self checking pair processor. This control synchronization is necessary to keep the two MC68000 micro processors running in lock step.

3.3.1.4 Comparators

The self checking pair processor has dual redundant comparators connected to both processors data buses and address buses. These comparators do a bit by compare of the data entering and leaving the processor and a bit by bit compare of every address bit sent by the processor. If either of the comparators senses a mis-compare an interrupt will be sent to both processors via the interrupt logic and both Watch Dog Timers for that channel will be forced to a timed out state. The self checking pair interrupt may be blocked with an interrupt block but the Watch Dog Timer time out can not be stopped.

3.3.1.5 PROMS (2K x 16)

The self checking pair processor has an independent 2K word by 16 bit PROM selected by the processors address bus and driving the buffered processor data bus.

These PROMs contain the controller initialization software and the memory loader software. The data from these PROMs is compared by the dual redundant data comparator as it is read into the processor. No error checking code is required because of this comparison.

3.3.1.6 Interface Buffers

The 16 bits of data to an from the processors in each half of the self checking pairs are buffered from the SCP data bus by bi-directional buffers. These buffers reduce the noise on the MC68000 data lines by shortening the lines to only those contained on the Printed Wiring Assembly. The buffers also allow the data drive more loads. The strobe and controls buffers on the other hand are uni-directional buffers used to increase drive capability.

3.3.1.7 23 Control

The 23 Control Logic Controls Bit 23 of the MC68000's address outputs. This logic forces address Bit 23 to a one during power on/power recovery or upon command by the MC68000. The Bit 23 control is used to jam the memory address to upper memory and in general force the computer into PROM memory. Once jammed on 23 control logic can only be released by a MC68000 command.

3.3.1.8 Address Lines

Except for address Bit 23 all of the other address Bits (22) are driven off of the PWA directly by the MC68000 drivers. Bit 23 is driven by the "23 Control" logic.

3.3.1.9 Bus Monitor

The Bus Monitor monitors the address strobe lines for both processors. The logic is established such that if the address strobe remain true for greater than 16 clock time a bus error (BERR) is generated. This prevents the failure to receive a DTACK signal from going undetected for up to a major cycle (20 milli seconds).

3.3.1.10 Interrupt

The self checking pair processor receives 3 coded interrupt lines at each MC68000 from the interrupt logic Printed Wiring Assembly. These 3 lines are synchronized with the SCP clock and encoded into 7 levels of interrupts by the interrupt logic board.

3.3.1.11 Detail Design

The detail design of the self checking pair processor is on drawing 34070354. The details of the MC68000's operation are in the Motorola MC68000 documentation.

3.3.1.12 Summary

The self checking pair processor has the following major features:

- o Synchronous self-checking processor operation
  - Dual 68000 microprocessors
  - Dual memories
  - Redundant Bit-by-Bit Comparison of Processor #1 and Processor #2 address and data bits.
- o Forced "RESET" addressing
- o Microprocessor clock $\geq$ 8 MHz
- o Fixed program memory (2K words x 16 bits No Wait states)
- o Internal interrupts as specified for the 68000 microprocessor.
- o Prioritized external interrupts
  - RESET (highest)
  - 7 levels of user interrupts
- o Bus monitor (BERR)
- o GSE control to assist troubleshooting

3.3.2 Main Memory

The Block II SSMEC Digital Computer has replicated 64K words by 16 Bit main memories. One 64K word memory is dedicated to each half of the self checking pair processor. All data in an out of the two memories is Bit for Bit compared. This comparison eliminates the need for any form of error checking code.

The basic requirements for the RAM memory are:

- o Dual 65,636 x Bit Static Random Access Memory
- o No 68000 wait states for read or write access
- o Word or Byte access
- o Data retention
  - Memory save power (Bat = 6.4 mA)
  - Power transition protection

Figure 3-11 is the block diagram of a 32K word x 16 Bit PWA. The SSMEC has four of these boards per channel.

3.3.2.1 Memory Chips

Each memory board is populated with 32 2K words by 8 Bit chips. These chips are partitioned into two 16K word by 16 Bit memory segments and each segment is further partitioned into an upper data byte and a lower data byte.

Which memory chips are read or written into by any given instruction is defined by address lines the read/write signal, the data strobes and the address strobes.

3.3.2.2 Address Lines

Each memory board receives 23 address Bit lines in addition to the upper data strobe and the lower data strobe (= Bit & Bit O). Address Bits 16-23 are decoded into 256 34K words by 16 Bit board select signals. Each memory board compares address Bits 16-23 against a code hardwired in by the Main Interconnect System (MIS). When address Bits 16-23 match the hardwire code the memory board is enabled. Only octal addresses 00 and FF are hardwired into the SSMEC MIB. Address Bits 12-15 are decoded into 2K words group or chip select signals. The decode of address Bit 15 selects either high order 16K words (1) or the low order 16K words (0) on the selected board. Address Bits 12-14 select one of eight 2K word by 8 Bit chip pairs in either upper or lower memory. Address Bits 1-11 are decoded by the memory chips into one of two thousand and forty eight words by 16 Bits.

SIMPLIFIED MAIN MEMORY DIAGRAM

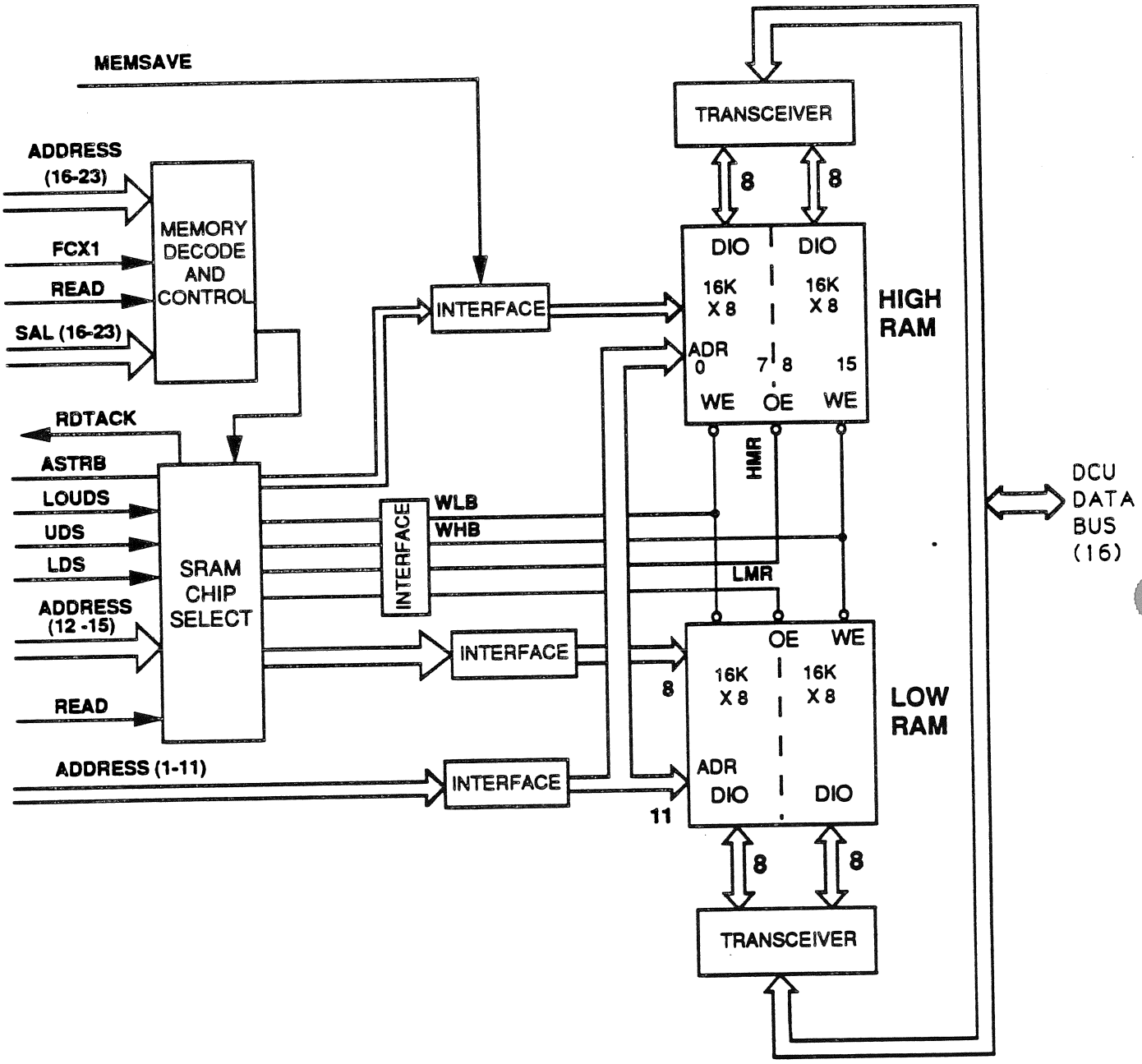


FIGURE 3-11

The Upper Data Strobe (UDS) and lower data strobe define whether data will be written into the upper Byte, lower Byte or both Bytes on a memory write sequence. All 16 Bits are written into when both the upper data strobe and lower data strobe are both asserted. The memory only allows word wide reads (16 Bits). The processor ignores the unwanted Bytes on a read operation.

3.3.2.3 DTACK

Each memory board sends a DTACK (RDACK) signal back to the processor when the addressed board receives an address strobe.

3.3.2.4 Interface Circuits

The memory interface circuits are 54S734 IC's that have a high output impedence when their Vcc is removed. These circuits help protect the memory when the memory is on back up or battery power.

3.3.2.5 Transceivers

The memory transceivers are bi-directional amplifiers that buffer the memory chips from the data bus and increase the drive to the data bus.

3.3.2.6 MEMSAVE

MEMSAVE is a signal generated by the Power Supply logic that de-selects all memory chips to protect their contents during power turn on and turn off.

3.3.3 Computer Interface Electronics (CIE)

Each channel in the controller has its own computer interface electronics group. These computer interface electronics group are made up of 6 Printed Wiring Assemblies (PWA) types. The function of these six PWA types is to provide the interface circuits the decoding and the timing for interfacing the SCP computers with:

- The Input Electronics
- The Output Electronics
- The Cross Channel CIE
- The Vehicle/Controller Electrical Interface (VEEI)
- The Vehicle Recorder Channel
- The Watch Dog Timers
- The Ground Support Electronics (GSE)

In order for the CIE to handle this task a system of four major data buses per channel was established. These buses were:

- o 1DATXX - Processor/Memory #1 Data Bus
- o 2DATXX - Processor/Memory #2 Data Bus
- o COMDBXX - Common Data Bus
- o XCMXXX - Cross Channel Data Bus

The 1DATXXdata bus is dedicated to the #1 processor and memory.

The 2DATXX data bus is dedicated to the # 1 processor and memory

The common data bus (COMDBXX) is designed to organize the in channel self-test data from the input electronics, output electronics, CIE, and cross channel data for transfer to the processor/memory data buses 1DATXX and 2DATXX.

The common data bus is organized into 16 Bit words. 17 words are for reading in channel data and 13 words are cross channel data. Of the cross channel words, four are for reading the failure data recorder and the rest are test words.

The cross channel data bus is designed to organize inchannel self-test data from the input electronics, output electronics, CIE, and failure data recorder for transfer to the cross channels common data bus. Table 3 - 1 defines the input data word format to the common data bus.

Figure 3-12 is a block diagram of the common data buses and cross channel data buses in both channels of the Block II Controller. Common data bus A is buffered on to processor/memory data buses #1A and #2A by two separate tri-state (3-S) buffers. Common data bus B is buffered on to processor/memory data buses #1B and #2B by another pair of tri-state buffers.

TABLE 3 -1

I/O INPUT DATA WORD FORMAT

INPUT WORD	BIT	LOGIC STATE	SELF TEST OUTPUT/FUNCTION
1	15 - 00	Note 2	Command Mux Test Word AAAA
2	15 - 00	Note 3	Commad Channel A
3	15 - 00	Note 3	Commad Channel B
4	15	Note 1	CH A /CH B ndicator 1
	14	Note 1	CH A /CH B ndicator 2
	13	1	SCPμP1 Data Error
	12	1	SCPμP2 Data Error
	11	1	SCPμP1 Address Error
	10	1	SCPμP2 Address Error
	09	0	POI Set
	08	0	PFI Pending
	07	0	PRI Pending
	06	0	SCPI Pending
	05	0	WDTI 1 Pending
	04	0	WDTI.2 Pending
	03	0	TRI Pending
	02	0	RCFI 1 Pending
	01	0	RCFI 2 Pending
	00	0	ADPFI Pending
5	15 - 00	Note 3	Command Channel C
6	15	0	WDT-1 Timed Out
	14 - 02	-	RTC Output (Bit 14 MSB)
	01	0	WDT-2 Timed Out
	00	1	Alternate Channel Power Bus Down
7	15	0	SEII-1 OPOV-A FAILED
	14	0	SEII-2 FPOV-A FAILED
	13	0	SEII-3 MOV-A FAILED
	12	0	SEII-4 MFV-A FAILED
	11	0	SEII-5 CCV-A FAILED
	10	0	SEII-6 SPARE-A FAILED
	09	0	SEII-7 OPOV-B FAILED
	08	0	SEII-8 FPOV-B FAILED
	07	0	SEII-9 MOV-B FAILED
	06	0	SEII-10 MFV-B FAILED
	05	0	SEII-11 CCV-B FAILED
	04	0	SEII-12 SPARE-B FAILED

TABLE 3 -1

I/O INPUT DATA WORD FORMAT

INPUT WORD	BIT	LOGIC STATE	SELF TEST OUTPUT/FUNCTION
7	03	1	Program Control SW4 Set
	02	1	Program Control SW3 Set
	01	1	Program Control SW2 Set
	00	1	Program Control SW1 Set
8	15-00	Note 2	Command MUX Test Word 5555
9	15-00	Note 2	Ch. A MUX Test Word AAAA
10	15-00	Note 2	Ch. B MUX Test Word 5555
11	15	Note 9	IE-A Coversion Complete
	14-08	Note 5	IE-A Range Counter
	07-01	Note 5	IE-Address Counter
	00	Note 10	IE-A Channel Indicator
12	15	Note 9	IE-B Conversion Complete
	14-08	Note 5	IE-B Range Counter
	07-01	Note 5	IE-B Address Counter
	00	Note 10	IE-B Channel Indicator
13	15	1	VRCA-VDT1A Complete
	14-08	Note3	VRCA-VDT1A Address Register
	07	1	VRCB-VDT2A Complete
	06-00	Note3	VRCB-VDT2A Address Register
14	15	1	VRCA-VDT1B Complete
	14-08	Note3	VRCA-VDT1B Address Register
	07	1	VRCB-VDT2B Complete
	06-00	Note3	VRCB-VDT2B Address Register
15	15	0	Bleed Valve A coil energized
	14	0	Fuel System Purge A Coil energized
	13	0	POGO Precharge Control A Coil energized
	12	0	Preburner S/D Purge A Coil energized
	11	0	Emergency S/D A Coil energized
	10	0	HPOP INT. Seal A Coil energized
	09	0	Sensor Checkout 1A (Note 7)
	08	0	Sensor Checkout 2A (Note 7)
	o7	0	Power OFF Time Exceeded B
	06	0	Ch.A Pull-in Hold In Pull-in
	05	0	PRC Overflow Test On-A

TABLE 3 -1

I/O INPUT DATA WORD FORMAT

INPUT WORD	BIT	LOGIC STATE	SELF TEST OUTPUT/FUNCTION
15	04	0	Fuel Preburner Igniter A ON
	03	0	Oxidizer preburner Igniter A ON
	02	0	Main Combustion Chamber Igniter A ON
	01	0	Spare (Note 8)
	00	0	Safety Switch A On
16	15	0	Bleed Valve B coil energized
	14	0	Fuel System Purge B Coil energized
	13	0	POGO Precharge Control B Coil energized
	12	0	Preburner S/D Purge B Coil energized
	11	0	Emergency S/D B Coil energized
	10	0	HPOP INT. Seal Seal B coil energized
	09	0	Sensor Checkout 1B (Note 7)
	08	0	Sensor Checkout 2B (Note 7)
	o7	0	Power OFF Time Exceeded A
	06	0	Ch.B Pull-in Hold In Pull-in
	05	0	PRC Overflow Test On-B
	04	0	Fuel Preburner Igniter B ON
	03	0	Oxidizer preburner Igniter B ON
	02	0	Main Combustion Chamber Igniter B ON
	01	0	Spare (Note 8)
	00	0	Safety Switch B On
17	15	0	Spare Bits
	14	0	Spare Bits
	13	0	Spare Bits
	12	0	Spare Bits
	11	0	Spare Bits
	10	0	Spare Bits
	09	0	Wired Spare #2
	08	0	2KHz A On
	07	0	Halt Exit Enable A Disable
	06	0	Spare Pneumatic Solenoid 1A Disabled
	05	0	Wired Spare #3
	04	0	Wired Spare #4
	03	0	Spare (Note 8)
	02	0	Spare (Note 8)
	01	0	FDR A Enabled
	00	0	Wired Spare #7(Note 8)
18	15	0	OPOV F/O Coil Energized
	14	0	FPOV F/O Coil Energized
	13	0	MOV F/O Coil Energized

TABLE 3 -1

I/O INPUT DATA WORD FORMAT

INPUT WORD	BIT	LOGIC STATE	SELF TEST OUTPUT/FUNCTION
18	12	0	MFV F/O Coil Energized
	11	0	CCV F/O Coil Energized
	10	0	SPARE F/O Coil Energized
	09	0	Wired Spare #2
	08	0	2KHz B On
	07	0	Halt Exit Enable B Disable
	06	0	Spare Pneumatic Solenoid 1B Disabled
	05	0	Wired Spare #3
	04	0	Wired Spare #4
	03	0	Spare (Note 8)
	02	0	Spare (Note 8)
	01	0	FDR B Enabled
	00	0	Wired Spare #7(Note 8)
19	15	0	OPOV F/S Coil A Energized
	14	0	FPOV F/S Coil A Energized
	13	0	MOV F/ Coil A Energized
	12	0	MFV F/S Coil A Energized
	11	0	CCV F/S Coil A Energized
	10	0	SPARE F/S Coil A Energized
	09	0	Spare Pneumatic Solenoid 2A Energized
	08	0	Spare Pneumatic Solenoid 3A Energized
	07	0	Spare Pneumatic Solenoid 4A Energized
	06	0	Spare Pneumatic Solenoid 5A Enertgized
	05	0	Spare Pneumatic Solenoid 6A Energized
	04	0	Spare Pneumatic Solenoid 7A Energized
	03	0	Spare (Note 8)
	02	0	Spare (Note 8)
	01	0	Spare (Note 8)
	00	0	Wired Spare #5A(Note 8)
20	15	0	OPOV F/S Coil B Energized
	14	0	FPOV F/S Coil B Energized
	13	0	MOV F/ Coil B Energized
	12	0	MFV F/S Coil B Energized
	11	0	CCV F/S Coil B Energized
	10	0	SPARE F/S Coil B Energized
	09	0	Spare Pneumatic Solenoid 2B Energized
	08	0	Spare Pneumatic Solenoid 3B Energized
	07	0	Spare Pneumatic Solenoid 4B Energized
	06	0	Spare Pneumatic Solenoid 5B Enertgized
	05	0	Spare Pneumatic Solenoid 6B Energized
	04	0	Spare Pneumatic Solenoid 7B Energized

TABLE 3 -1

I/O INPUT DATA WORD FORMAT

INPUT WORD	BIT	LOGIC STATE	SELF TEST OUTPUT/FUNCTION
20	03	0	Spare (Note 8)
	02	0	Spare (Note 8)
	01	0	Spare (Note 8)
	00	0	Wired Spare #5B(Note 8)
21	15-00	NOTE 3	OE A Storage Register
22	15-00	NOTE 3	OE B Storage Register
23	15-00	Note 2	Channel A MUX Test Word 5555
24	15-00	Note 2	Channel B MUX Test Word AAAA
25	15-00	Note 3	16 Bit Status Word A
26	15-00	Note 3	16 Bit Status Word B
27	15-00		All Ones
28	15-00		All Ones
29*	15	1	FDR SCPμP2 FCO
	14	1	FDR SCPμP2 FC1
	13	1	FDR SCPμP2 FC2
	12	Note 4	FDR SCPμP2 R/W
	11	1	FDR SCPμP2 IPL0
	10	1	FDR SCPμP2 IPL1
	09	1	FDR SCPμP2 IPL2
	08	1	FDR SCPμP2 Data Error
	07	1	FDR SCPμP2 Address Error
	06-00	Note 5	FDR SCPμP2 Address 7 MSBs (Bit 06= MSB)
30*	15-00	Note 3	FDR SCPμP2 Address 16 LSBs (Bit 00= LSB)
31*	15-00	Note 3	FDR SCPμP2 Data (Bit 15 = MSB)
32*	15-05	Note 6	FDR Address Register
	04-00	0	Spares (Note8)

TABLE 3 -1

I/O INPUT DATA WORD FORMAT

* Input words 29, 30, 31, and 32 are Cross Channel Words.

Note: 1) Channel A Shall have a bit 15 logic 1 and bit 14 logic 0 via MIB hardwires.
Channel B Shall have a bit 15 logic 0 and bit 14 logic 1 via MIB hardwires. (Logic 1 ≥ 2.5v; Logic 0≤ 0.5v
2) Sixteen bit binary pattern of $ AAAA or $ 5555
3) Sixteen data words composed of 1s and 0s
4) Logic 1=Read; Logic 0=Write
5) Seven bits of binary data.
6) Eleven bits of binary data
7) Logical AND of ON/OFF Registers 1A and 1B bits.
8) "Spare" and "Hard Wire Spare" define internal hardware configurations and both shall be transparent to software.
9) 0=Complete, 1= DPM Request.
10) 0= Channel A ; 1= Channel B.

3.3.3.1 Computer Interfasce PWA No. 1 (CIE-1)

Computer interface PWA No. 1 schematic is given in drawing number 34069277 and the assembly and parts list are 34069279. The functions contained on CIE-1 are:

- o I/O Decode Logic
- o IE Dual Port Memory #1
- o Recorder Dual Port Memory #1
- o Dual Port Memory Control Logic

CIE COMMON & CROSS CHANNEL DATA BUSSES

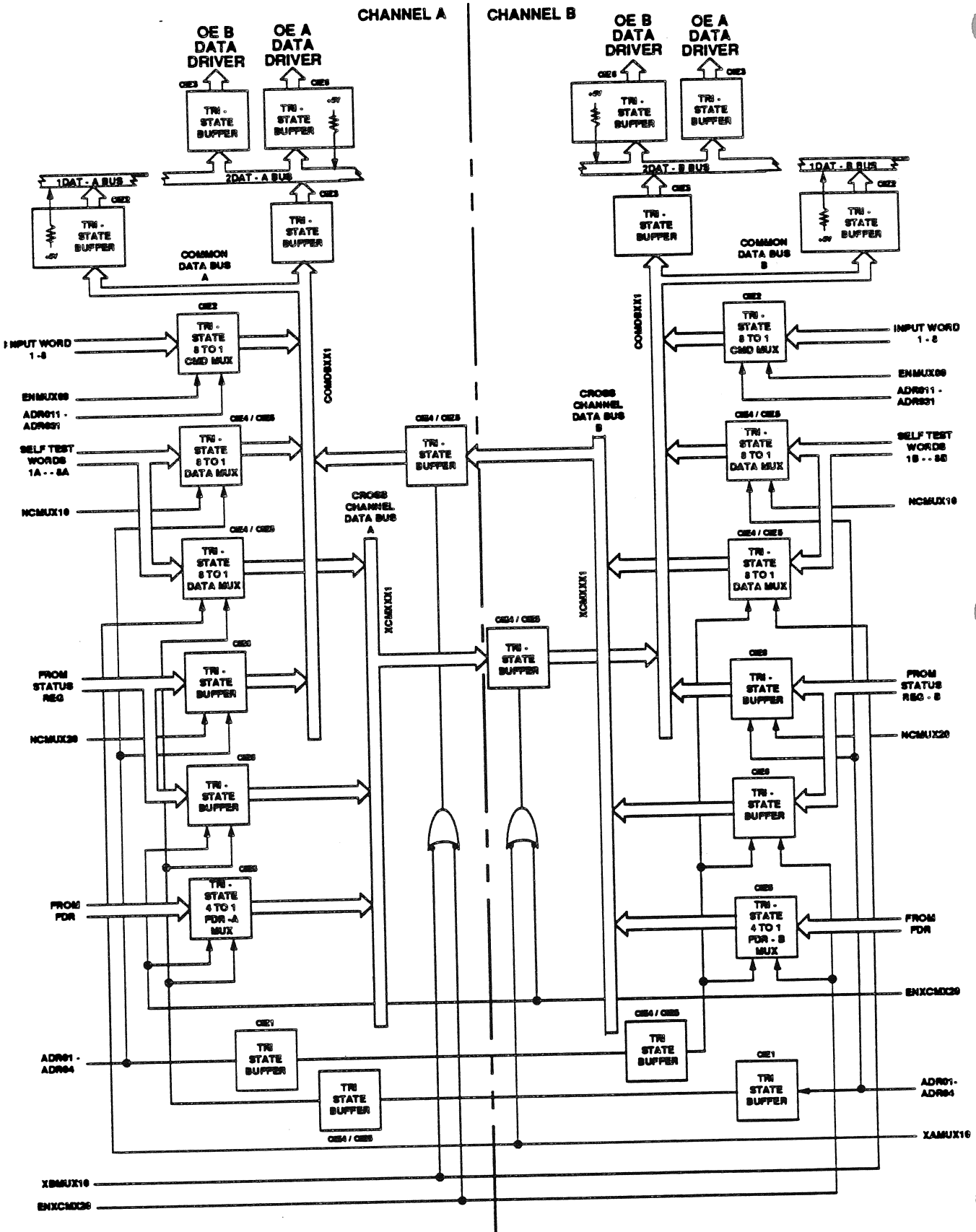


FIGURE 3 - 12

3.3.3.1.1 I/O Decode Logic

The self checking pair interfaces with the input and output electronics as memory addressed I/O. This means that the SCP addresses I/O devices the same way it would memory word locations. When the SCP wants to send data to an I/O device it writes into the address assigned to that device. When the SCP wants to receive data from an I/O device it reads from the address assigned to the device. Only even address words are valid I/O device addresses. The controller I/O address map is:

Address Field From	To	Function
820000	8201FF	IE Dual Port Memory
820600	8206FF	Recorder Channel 1 and 2
820A00	820AFF	Output Commands
820B00	820BFF	Output Commands (not implemented).
820C00	820CFF	Input Commands
820D00	820DFF	Input Commands (not implemented).

NOTE: All addresses are expressed as the 24 Bit address field used in the processor and not the 23 Bit hardware address lines.

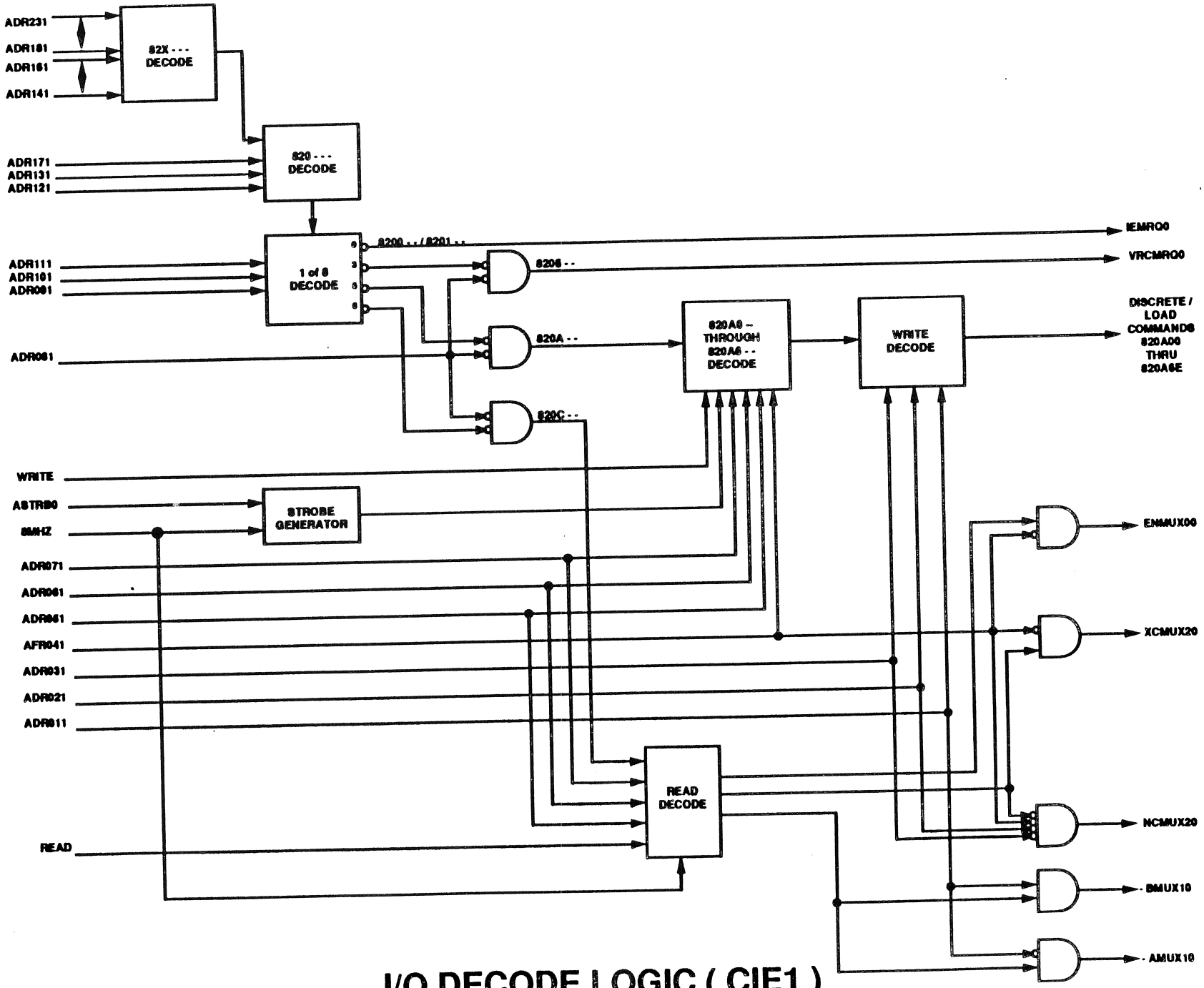
Figure 3-13 is a block diagram of the I/O decode logic on CIE-1and Table 3 -1 defines the decodes. As you can see the decode uses all 23 address lines to decode I/O addresses. As can be seen, all of the addresses between 820000 and 820DFF are not used for I/O addresses. In fact only 420 addresses are decoded or enabled by CIE1.

- o 255 for IE Dual Port Memory
- o 127 for Recorder Channels
- o 29 Output Commands
- o 9 Input Commands

3.3.3.1.2 Input Electronics Dual Port Memory

The requirements per channel for the Block II Input Electronics (IE) dual port memories are:

- o Two - 256 words x 16 bit RAM memories
- o IE Port is write only
- o Contention between IE and DCU resolved in favor of the DCU.
- o Generate DTACK for all reads or write
- o Insert two wait states for all read or writes
- o The common control logic for the IE dual port memories for SCP processors number one and two.



I/O DECODE LOGIC (CIE1)

FIGURE 3 - 13

TABLE 3 -2

I/O INSTRUCTIONS (WRITE COMMANDS)

Output Commands shall be Move from DN to EA instructions.

Function	Load/Discrete	Effective Address
Load IE Address Counter	L	820A00
Load IE Range Counter	L	820A02
Load Channel A Storage Reg.	L	820A04
Load Channel B Storage Reg.	L	820A06
Spare #2	-	820A08
Spare #3	-	820A0A
Spare #4	-	820A0C
Spare #5	-	820A0E
Initiate IE Operation	D	820A10
Transfer Chan. A Storage Reg.	D	820A12
Turn On Chan. OE Power Switch	D	820A14
Turn Off Chan.A OE Power Switch	D	820A16
Spare Cmd. #3	D	820A18
Spare Cmd. #1	D	820A1A
Set +5V UNDER Voltage Test	D	820A1C
Reser +5V Under Voltage Test	D	820A1E
Clear Reset Jam Bit	D	820A20
Transfer Chan. B Storage Reg.	D	820A22
Turn on Chan. B OE Power Switch	D	820A24
Turn Off Chan. B OE.Power switch	D	820A26
Reset WDT1	D	820A28
Terminate IE Sequence	D	820A2A
Initiate Recorder Data	D	820A2C
Set WDT1 Time Out	D	820A2E
Reset WDT2	D	820A30
Switch Recorder to DCU B	D	82OA32
Switch Recorder to DCU A	D	82OA34
Decrement Cross Chan. FDR Address Counter	D	820A36
Inhibit FDR	D	820A38
Reset FDR Inhibit	D	820A3A
Spare Cmd. #2	D	820A3C
Set WDT2 Time Out	D	820A3E
Clear PFI0	D	820A40
Clear PRI0	D	820A42
Clear SCPI0	D	820A44
Clear WDTH1	D	820A46
Clear WDTH2	D	820A48
Clear TRI0	D	820A4A
Clear SEII	D	820A4C
Clear Comparator #1	D	820A4E

TABLE 3 -2

Function	Load/Discrete	Effective Address
Clear Comparator #2	D	820A50
Clear ADPFI	D	820A52
Clear RCFI1	D	820A54
Clear RCFI2	D	820A56
Reset POI	D	820A58
-----	D	820A5A
-----	D	820A5C
-----	D	820A5E
Load Status Reg.	L	820A60
Load Interrupt Mask #1	L	820A62
Load Interrupt Mask #2	L	820A64
Set POI	L	820A66
-----	L	820A68
-----	L	820A6A
-----	L	820A6C
-----	L	820A6E

I/O INSTRUCTION (READ COMMANDS)

INPUT COMMANDS SHALL BE :MOVE FROM EA TO DN

INPUT WORD	INPUT FUNCTION	EFFECTIVE ADDRESS
1	Read Cmd Test Wd. AAAA	820C00
2	Read Command Channel A	820C02
3	Read Command Channel B	820C04
4	Read Processor Signal Wds.	820C06
5	Read Command Channel C	820C08
6	Read RTC	820C0A
7	Read SEII	820C0C
8	Read Command Test Wd 5555	820C0E
9	Read Self Test Word 1A	820C20
10	Read Self Test Word 1B	820C22
11	Read Self Test Word 2A	820C24
12	Read Self Test Word 2B	820C26
13	Read Self Test Word 3A	820C28
14	Read Self Test Word 3B	820C2A

TABLE 3-2

I/O INSTRUCTION (READ COMMANDS)

INPUT COMMANDS SHALL BE :MOVE FROM EA TO DN

INPUT WORD	INPUT FUNCTION	EFFECTIVE ADDRESS
15	Read Self Test Word 4A	820C2C
16	Read Self Test Word 4B	820C2E
17	Read Self Test Word 5A	820C30
18	Read Self Test Word 5B	820C32
19	Read Self Test Word 6A	820C34
20	Read Self Test Word 6B	820C36
21	Read Self Test Word 7A	820C38
22	Read Self Test Word 7B	820C3A
23	Read Self Test Word 8A	820C3C
24	Read Self Test Word 8B	820C3E
25	Read Status Word A	820C40
26	Read Status Word B	820C42
27	Read	820C44
28	Read	820C46
29	Read FDRWd 1	820C48
30	Read FDRWd 2	820C4A
31	Read FDRWd 3	820C4C
32	Read FDRWd 4	820C4E

CIE 1 contains the common control logic for SCP processors and the dual port memory for the number one processor of the SCP. Figure 3-14 is a block diagram of both IE dual port memories. This block diagram shows the break between the processor number one memory on CIE 1 and the processor number two memory on CIE 3.

The IE dual port memory on CIE 1 consists of two 2K words by 8 Bit RAMS, a one of two address select circuit (Mux) and two sets of data buffers. The one of two select logic selects between the input electronics and the processor number one address lines as the source of the desired memory address. Both these address sources are eight Bits wide, therefore they can address only 256 words of the 2K words in the RAMS. The data for this 256 word memory comes from either a 16 Bit wide bi-directional buffered data word from the SCP's number one processor buffered data bus (IDATXX).

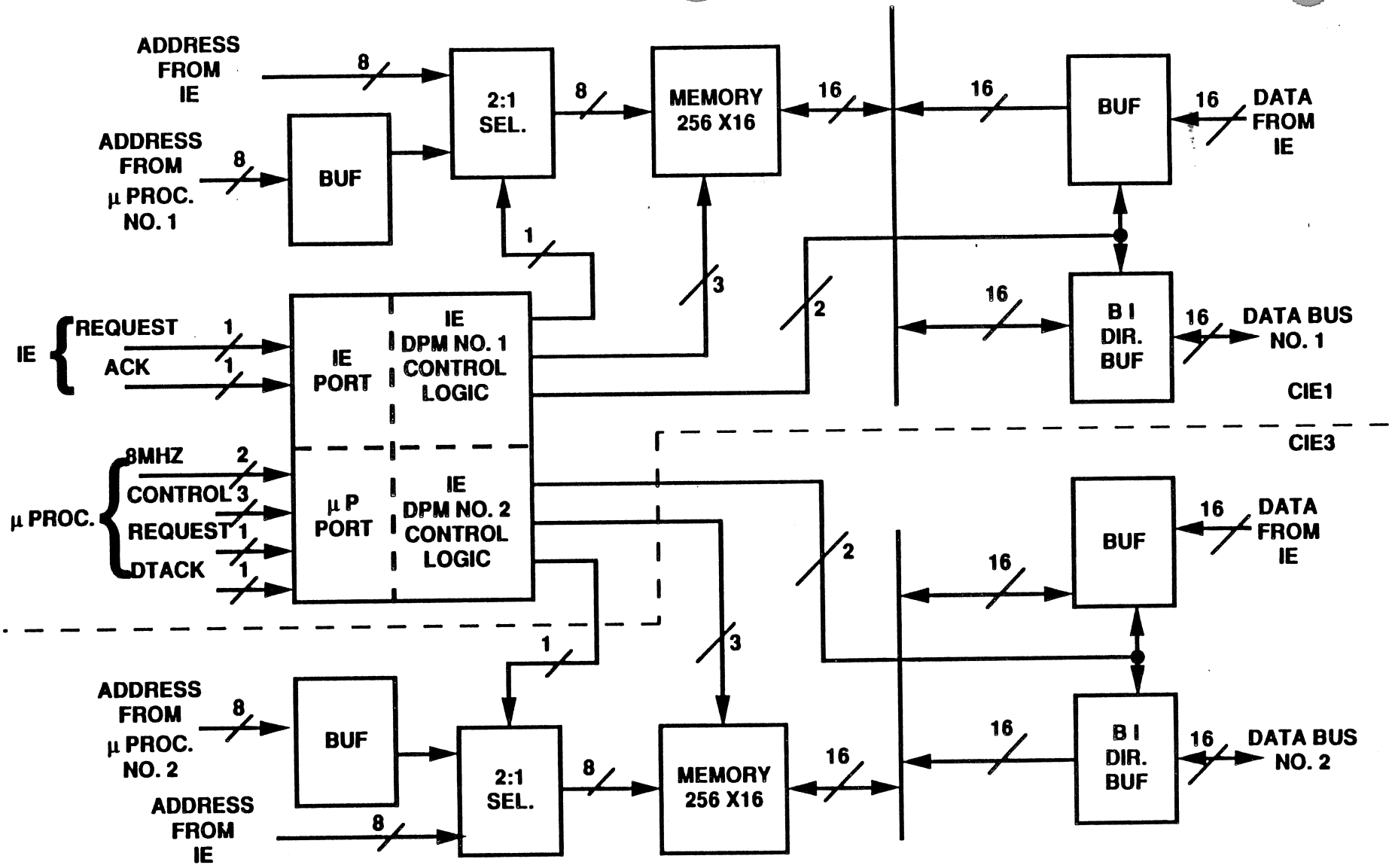
Data words can only be read out of these memories by the bi-directional buffer on to the IDATXX data bus. The IE Dual Port memory's read and write control is contained in the common IE dual port memory control logic of CIE1.

3.3.3.1.2.1 IE Dual Port Memory Control Logic

The IE Dual Port Memory Control Logic's function is to control the writing into the dual port memory and the reading of data from the dual port memory.

The Read operation has only one source of request and that is the SCP processor. When the processor makes a read request the control logic selects the number 1 processor as the source of address and enables the selected word on to the IDATXX data bus, if an IE write is not in process. If an IE write is in process the read request and the DTACK signal will be delayed until the write operation is complete. At the end of the write the read will be executed and the DTACK signal will be sent to the processor.

The Write operation has two sources of data and address. The data may come from the number one processor or the IE. For input electronics controlled writes the address comes from the IE address counter (IE1DMAXX) and the data from the IE data bus (I1MDXX). For proessor controlled writes the data comes from processor number data bus (1DATXX) and the address from the processor number one address bus (1ADRXX). The control logic resolves any conflict between the IE and processor in favor of the processor, except that any IE write in process will always be allowed to finish.



IE DUAL PORT MEMORY BLOCK DIAGRAM

FIGURE 3 -14

3.3.3.1.3 Recorder Dual Port Memory (RDPM)

The requirements for the SSMEC Block II VIE recorder dual port memories are:

- o Two 128 Word x 16 Bit Memories
- o Common Control Logic for both Memories
- o Recorder Port is Read only
- o DCU Port is Read/Write
- o Resolves contention between DCU and Recorder in DCU's favor.
- o Generate DTACK for all Processor Reads or Writes
- o Inserts two Wait States

CIE1 contains the common control logic for both data recorder channels and the dual port memory for data recorder channel A. Figure 3-15 contains the block diagram for the both recorder channels. The memory on CIE1 consists of two 2K word by 8 bit RAMS, a one of two address selector, a 16 bit wide data driver, and a 16 bit wide bi-directional data buffer. There are only seven address lines going to the RAM memory chips from the two to one MUX and this sets the memory size at 128 words although the chips contain 2K words.

3.3.3.1.3.1 Recorder Dual Port Memory (RDPM) Control

The function of the recorder dual port memory control is to control the writing of data into the recorder RAMS and the reading of data from the recorder RAMs'.

The Write operation has only one source and that is the number one processor. The number one processor provides the control signals to the RDPM control logic and the data and address lines to the DPM on CIE1.

On the other hand the Read request has two sources. One is the number one processor request and control lines with the number one address lines (1ADRXX) and access to the number one data bus (1DATXX). The other read request comes from data recorder channel A address lines (AVRCMXX) and access to the A channel recorder data bus (VRCADXX).

All conflicts between the processor and data recorder for access to the RDPM are resolved in favor of the processor except if the read of a word by the recorder is in process. If a recorder read is in process when the processor request access to the RDPM the processor will have to wait until that read is complete before it is granted access to the RDPM and receives its DTACK signal.

A CRYOGENIC MIXED-SIGNAL PROCESS FOR RADIATION-HARDENED APPLICATIONS

Abstract

This paper describes an analog/digital CMOS process optimized for operation at 77K. The process uses 1.2 micron ground rules and has applications in low-temperature signal processing. Typical applications include IR imaging and data acquisition for high-energy particle physics experiments.

Un Procédé CMOS Durci Pour Applications Cryogéniques

Résumé

Cette communication présente un procédé CMOS analogique/digitale optimisé pour opération à 77K. Le procédé a des règles de conception de 1.2 microns et a des applications en traitement de signaux à basse temperature. Des applications spécifiques sont la visualisation de scènes dans le domaine infrarouge et aussi l'acquisition de données pour expériments de physique de particules à haute energie.

Author: N. van Vonno
Harris Semiconductor
Mail Stop 54-101
2401 Palm Bay Road NE
Palm Bay, FL 32905
United States of America

Telephone: 407-724-7546
FAX: 407-729-5005

"A Cryogenic Mixed-Signal Process for Radiation-Hardened Applications"

Nicolaas W. van Vonno, Harris Semiconductor
P. O. Box 883, MS 54-101, Melbourne, FL 32902-0883 USA

Abstract

Signal processing and A/D conversion for cryogenic applications places severe demands on the silicon fabrication process used to implement these functions, particularly in ionizing radiation environments. We describe a process designed for cryo applications such as high-energy collider front-end electronics, with specific optimization in the areas of noise, radiation hardness and predictable operation at 77K. Applications of the technology are reviewed together with device issues and radiation test results.

I. INTRODUCTION

The requirements for analog and mixed-signal electronics operating at cryogenic temperatures place particularly severe demands on both processing and design. Processes must be specifically optimized, and accurate modeling is a requirement for the extreme low-power designs needed to minimize cryo cooler loading. Freeze-out effects lead almost immediately to the elimination of bipolar technology, resulting in domination by CMOS processes. Demands on packing density have concentrated development work on CMOS processes with gate lengths in the .8-1.2 micron range, with at least two and preferably three levels of interconnection.

Initial process development at Harris centered around a 1.25 micron bulk CMOS process in use for SRAM fabrication. These efforts led to basic characterization of the process at 77K and the definition of modifications needed for a robust low-temperature version of the process. A parallel effort in process development and circuit design methodology was then executed, culminating in experimental test device arrays. Program objectives included the following:

- Development of a low-noise cryogenic version of the baseline process, including the addition of a high-quality capacitor.
- Process modifications to provide natural environment, low-level total dose radiation hardness.

This program resulted in the successful development of a low-noise rad-hard cryogenic CMOS technology and the delivery of demonstration unit readout cell arrays. Follow-on development has further refined the process and addressed important issues in characterization, modeling and device physics. Follow-on programs were also undertaken in other applications, of which details will be discussed next.

II. PROCESS APPLICATIONS

We begin our discussion with some example applications for a cryogenic process; this will allow us to evolve a set of process requirements which will then be addressed in the balance of the paper. Present applications are in signal processing for imaging applications and in low-temperature front end detector electronics for high-energy particle physics experiments. Imaging applications stress high-density signal process elements such as transimpedance amplifiers, filters, multiplexers and analog to digital (A/D) converters. These functions place particular emphasis on low-power design since reduction of cryo cooler size enables major cost reductions. Harris has performed numerous designs in this area using the LN77 process, and gained important experience in mixed signal design tools. This experience has led to the release of advanced mixed-signal design tools on the Harris FASTRACK™ design system, including simulation, layout and design verification capabilities.

A second and perhaps even more difficult application is in front-end detector electronics. These devices are commonly operated at liquid argon temperature (80K) and perform low-noise preamplification, filtering, multiplexing and A/D conversion functions. The radiation levels for these civilian applications generally exceed those found in the natural space environment, but are spread out over a larger time period. This application stresses low noise, low power and reliability; accessibility for device replacement is difficult. It should also be noted that data rates in front-end electronics tend to be significantly higher.

The sample applications now allow us to list some of the requirements for a cryogenic mixed-signal process:

- High packing density for complex mixed-signal devices.
- Low noise, particularly in the low-frequency 1/f regime.
- Predictable low-power operation through repeatable subthreshold behavior.
- Compatibility with high reliability requirements, although the exact meaning of these in a cryo context is not yet

clear.

- Freedom of device wear out mechanisms such as hot electron degradation and time-dependent dielectric breakdown (TDDB).

- Adequate radiation hardness, recognizing that damage mechanisms at low temperature are much different from those at standard temperature ranges.

III. PROCESS DESCRIPTION: THE LN77 PROCESS

The basic LN77 technology evolved from an earlier static RAM process, as described earlier. Some key process features are listed in Table 1. At present, the LN77 baseline cryogenic CMOS process is fully developed, and the process is ready for a formal qualification procedure. The process has evolved into a mature 77K process through lengthy efforts in characterization, radiation testing and device modeling; the section on Device Issues will address some of the more important issues. Threshold voltages for the LN77 process were optimized for an operating temperature range of 35K to 150K, total dose hardness of 200 krad(Si) and adequate room temperature operation, although in order to meet the first two goals the room temperature P-channel leakage is somewhat compromised. Achieving these threshold voltages required changes in N well doping, P well doping and CD implants from the original process.

Table 1: LN77 Process Features

- 6 inch N-epi on N+ starting material.
- Twin retrograde implanted device wells.
- Recessed isoplanar field oxide.
- Substrate capacitor with implanted arsenic bottom plate.
- 225 Angstrom gate oxide.
- Lightly-doped drain construction of N channels.
- Optical stepper lithography, 5x stepper.
- 1.2 micron minimum feature size.

The process uses 6" epi substrates to control latchup; as we will see in the section on device issues, latchup is not a problem at cryo, but testability demands the technology be robust at room temperature as well. The implanted substrate capacitor is optimized for high capacitance density as required for unit cells in readout circuitry. A Canon 5X optical stepper provides superior registration and can produce many different die on one wafer. Die size for a single stepped reticle is 20x20 millimeters, and using multiple reticles die sizes of well over an inch are practical.

IV. RADIATION EFFECTS

Radiation physics at 77K has been found to differ significantly from well-known effects at room temperature. The rate of hole trapping is increased, since hole mobility is drastically reduced;[1] threshold voltage shift is more sensitive to gate bias, and the usual room temperature hardening techniques are ineffectual. In the case of thin oxide hardening, a primary approach is to thin this oxide as much as is practical. The thick field oxide, however, cannot be readily hardened.[2] The LN77 process returned to a proven earlier method of preventing N-channel field inversion by the use of P+ guard rings. These structures use a double boron implantation to avoid freeze-out effects; they add 3.6 microns to the length and width of the N-channel device, but are remarkably effective in reducing N-channel device leakage. Extensive total dose testing at 77K has proven out this technique, and Figures 1 through 3 summarize data. In Figure 1, we show results of total dose testing of P-channel devices to 200 krads(Si); note predictable threshold shift of 400 mV at that level and the absence of excessive device leakage. Figure 2 and 3 summarize results of equivalent testing on non-guardringed and guardringed devices, respectively, and the effectiveness of the rings is well demonstrated by this data.

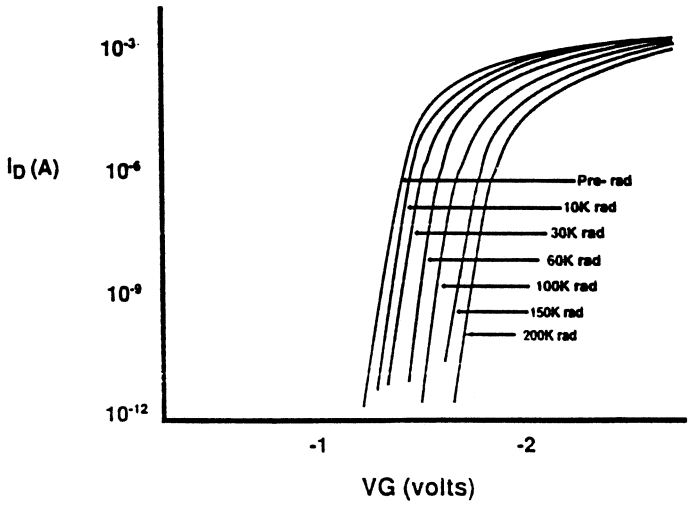


Figure 1: Total Dose Response of P-Channel Devices
^{60}Co Source at 77°K, 25 rad(Si)/sec, 0 volt gate bias

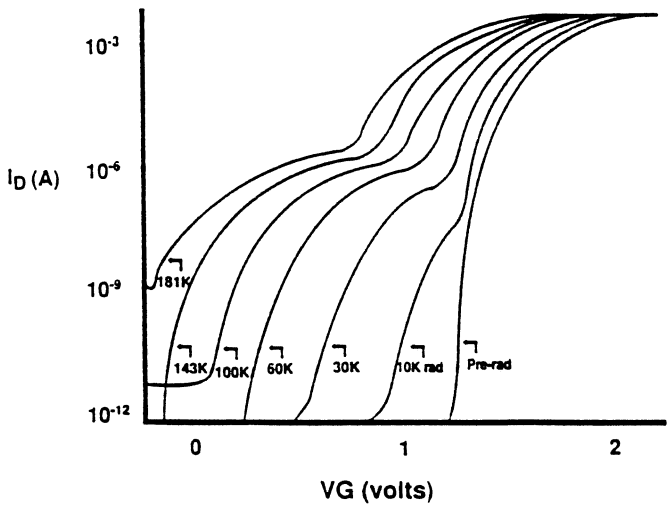


Figure 2: Total Dose Response of Non-Guarded N-channel Devices, ^{60}Co Source at 77°K, 25 rad(Si)/sec, 0 volt gate bias

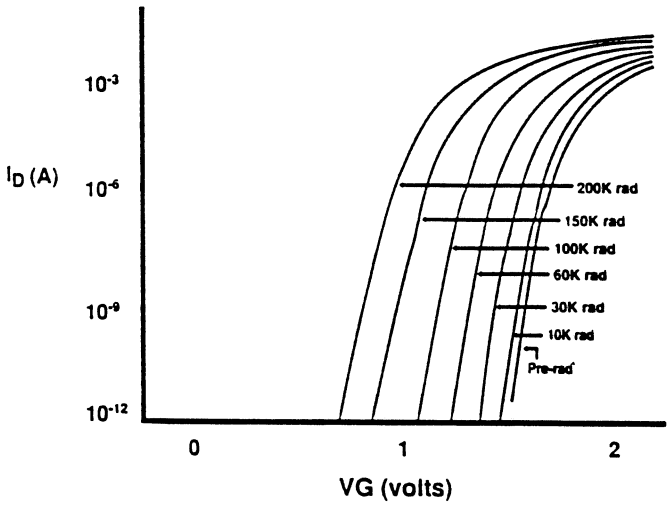


Figure 3: Total Dose Response of Guarded N-Channel Devices, ^{60}Co Source at 77°K, 25 rad(Si)/sec, 0 volt gate bias

Annealing effects have also been studied, and were found to be present although reduced in magnitude from those at room temperature. Irradiating LN77 devices to 200 krads(Si) and then maintaining them under bias at 77K for up to 1500 hours produced over 500 mV anneal; no change in subthreshold slope was observed. This annealing is clearly due to hole detrapping[3] and no threshold changes due to reverse annealing were found upon recooling. Gate bias for this experiment was a worst-case -2.75V.

V. DEVICE ISSUES

77K operation of a CMOS process demands close attention to device issues, and some of the more important ones will be reviewed in this section. Latchup data taken during process development showed the expected temperature variation. As temperature drops, base-emitter shunting resistances are reduced; lateral PNP beta is a base transport factor limited effect, and degrades due to reduced minority-carrier lifetime, while the injection-efficiency limited vertical NPN beta degrades due to bandgap changes. Sustaining voltage was hence found to be greater than 10 volts at 77K, although sample heating makes this a difficult measurement. With the original epi thickness the room temperature sustaining voltage was an unacceptable 3 volts; this has been brought up to 7 volts by optimizing epi thickness from the original 4.7-7.0 microns to the present 1.2-2.8 micron range.

The lightly-doped drain structures were initially used to control hot electron effects,[4] but were found to be very vulnerable to large amounts of positive charge trapped in the deposited spacer oxides; this charge shifts the n-channel LDD towards being less resistive which improves the device's transconductance. The p-channel device of course displays the opposite effect, showing significant GM degradation at 200 kilorads. Outright elimination of the PLDD regions was required to retain sufficient post-radiation transconductance. This also eliminates partial freeze-out effects in these regions which occur at temperatures below 100K.

Perhaps the most significant device issue of the LN77 process has been hot electron degradation.[5-8] This effect becomes more pronounced at low temperature as reduced phonon scattering increases the carrier mean free path and hence the impact ionization probability. Hot electron trapping efficiency is also improved due to reduced thermal trap depopulation. Preliminary work indicates that a 1.2 micron device is marginal at 5.5 volts at room temperature and challenging at 77K. Hot electron testing at low temperature continues; for reliable process operation at supply voltages in excess of 5 volts, composite gate dielectrics are necessary, with positive effects on radiation hardness as well. Current cryo process research is focusing on composite oxynitride dielectrics.[9-13]

VI. CONCLUSION

A brief overview of a mixed-signal cryogenic CMOS process using 1.2 micron ground rules has been given. The process has been optimized for 77K operation and has been used for both in-house and customer-designed signal processors. Applications include supercollider front-end

electronics and infrared image processors.

VII. REFERENCES

[1] J.R. Srour and K.Y. Chiu, "MOS Hardening Approaches for Low-Temperature", *IEEE Trans. Nuc. Sci.*, NS-24, 2140 (1977).

[2] S.D. Clark, P.L. Cole, J.F. Kreig and D.T. Butcher, "Total Dose Hardening of Cryogenic CMOS", *Journal of Radiation Effects Research Engineering*, Vol. 9, Number 1, December 1990.

[3] D. Hemmenway, private communication.

[4] M. Song, J.S. Cable, J.C.S. Woo and K.P. McWilliams, "Optimization of LDD Devices for Cryogenic Operation", *IEEE Elec. Dev. Letters*, Vol 12, Number 7, July 1991.

[5] E. Takeda, "Hot-Carrier and Wear-Out Phenomena in Submicron VLSI's," in *Proc. VLSI Symp.*, 1985.

[6] J.J. Tzou, C.C. Yao, R. Cheung, and H. Chan, "Hot Electron-Induced MOSFET Degradation at Low Temperatures," *IEEE Electron Device Lett.*, vol. EDL-6, 1985.

[7] T.-C. Ong, P.K. Ko, and C. Hu, "50 A Gate-Oxide MOSFET at 77K", *IEEE Trans. Electron Devices*, vol. ED-34, 1987.

[8] P. Heremans, G. van den Bosch, R. Bellens, G. Groeseneken and H. Maes, "Temperature Dependence of the Channel Hot-Carrier Degradation of N-Channel MOSFET's", *IEEE Trans. Electron Devices*, vol. ED-37, April 1990.

[9] J.C. Pickel, J.C. Boisvert, T.E. Bradley, J.S. Cable, and R. Glidden, "Total Dose Characterization of Thin ONO Gate Dielectrics for IR Focal Plane Applications", Presented at 1991 IRIS Conference and Published in Conference Proceedings, August 1991, Boulder, Colorado.

[10] J.C. Pickel, J.C. Boisvert, T.E. Bradley, J.S. Cable, and R. Glidden, "Mechanisms for Total Dose Hardness of Thin ONO Gate Dielectrics at Cryogenic Temperature", presented at the HEART Conference, February 1992, Albuquerque, New Mexico.

[11] J.S. Cable, S. Lizotte, S. Lucia, and A. Miscione, "Rapid Thermal Nitridation of Silicon Dioxide for Rad-Hard Cryogenic CMOS Applications", presented at 1987 Hardened Electronics and Technology Conference, Cocoa Beach, Florida, February 1987.

[12] J.S. Cable and J.C.S. Woo, "Hot Carrier Induced Interface State Generation in Submicron Reoxidized Nitrided Oxide (ONO) Transistors Stressed at 77K", *IEEE Transactions on Electron Devices*, December 1991.

[13] J.S. Cable, J. Liao and J.C.S. Woo, "Improvement in Rapid Thermal Oxide/Re-Oxidized Nitrided Oxide (ONO) Films Using NF_3", presented at 1991 Spring Meeting of Materials Research Society and Published in Conference Proceedings, Anaheim, California, May 1991.

A 256K STATIC RANDOM-ACCESS MEMORY IMPLEMENTED IN SILICON-ON-INSULATOR TECHNOLOGY

Abstract

This paper describes a 256K static random-access memory implemented in the Harris RHD-1 silicon-on-insulator (SOI) process, using .8 micrometer ground rules. The use of an SOI process enhances SEU performance and also enables a worst-case access time of 35 nanoseconds to be achieved. The paper discusses process and performance details of the SRAM, together with SEU and total dose testing results.

Une Mémoire Statique 256K Durcie Implementée en SOI

Résumé

Cette communication présente une mémoire statique de 256K bits fabriquée selon le procédé durci Harris RHD-1 des règles de conception de .8 micromètre sur substrat SOI. L'usage du procédé SOI procure l'immunité SEU et aussi autorise un temps d'accès de 35 ns (pire case). La communication présente des discussions du procédé et de la performance du SRAM, aussi que les resultats de caractérisation en dose cumulée et SEU.

Author: N. van Vonno
Harris Semiconductor
Mail Stop 54-101
2401 Palm Bay Road NE
Palm Bay, FL 32905
United States of America

Telephone: 407-724-7546
FAX: 407-729-5005

A 256K Static Random-Access Memory Implemented in Silicon-on-Insulator Technology

N. van Vonno and B. R. Doyle
Harris Semiconductor
Military and Aerospace Division
P. O. Box 883
Melbourne, Florida 32902-0883, USA

I. INTRODUCTION

Single-event upset (SEU) phenomena have been a topic of intense interest since first being identified in the early 1980's. These soft errors occur in digital electronics, notably static random-access memories, and are caused by high-energy protons or heavy particles. Initial efforts at SEU reduction involved a move away from vulnerable bipolar memories to the current CMOS technology, combined with novel memory cell design to further improve performance. Current practice uses thin-film MOS structures to greatly reduce (and bound) the critical generation volume. Silicon-on-Sapphire (SOS) technology uses a thin Si film grown on single-crystal sapphire substrates; this yields a very thin device layer with important advantages in reduced carrier lifetime reduction due to lattice-mismatch induced strain. An alternative approach uses silicon-on-insulator (SOI) technology, in which a thin Si layer is separated from a bulk substrate by a buried insulator layer; this layer can be established by several methods including ion implantation (SIMOX), wafer bonding and zone-melt recrystallization. These alternative approaches offer the advantage of all-silicon processing and potentially larger wafer size.

As implied by our earlier definition of single-event upset it is clear that random-access memories offer the most leverage in applying SOI technology. These memories are all fully static in nature. Early applications included SRAM devices in silicon-on-sapphire up to 64 Kbits; these have found wide application in space systems due to their excellent SEU resistance, implied not only by the thin active device layer but also by the reduced carrier lifetime in this layer. Recent advances in SOI technology have enabled the design and development of SRAM devices in the 64K bit and up range, and the balance of this paper will discuss an example 256Kbit device designed for space applications. We will first provide a more detailed description of the SOI process used and will describe the device and its performance, followed by a section on radiation testing results to date. Device reliability will also be discussed, as it is an important consideration for space applications.

II. PROCESS DESCRIPTION

The Harris RHD-1 process starts with SOI substrates consisting of a thin single-crystal silicon layer on a buried SiO_2 insulator. These substrates are six inches in diameter and are procured against stringent defect density and film quality standards. Initial processing consists of establishing refilled, planarized trenches for lateral device isolation; this method insures a planar structure, a significant advantage for critical applications. Ion implanted twin retrograde device wells are then established, providing complementary regions for active devices. Active areas are then defined, followed by gate poly silicon deposition and definition. Ion implantation is then used to establish device source/drain regions; these are bottomed out against the buried insulator, resulting in minimized parasitic capacitance. The minimum feature size for the process is .8 micrometer, with as-drawn gate lengths of .9 micrometer; this results in an effective channel length of .7 micrometer. Short channel lengths can lead to device voltage limitations due to hot electron effects, and the RHD-1 process follows conventional submicrometer practice by using lightly-doped drain (LDD) structures to largely eliminate these effects. The active devices are interconnected by a planarized two-level metallization system, continuing the emphasis on device planarity as a key factor in device reliability. Interconnection starts with the siliciding of both the gate poly and source/drain regions, providing excellent contacts as well as a significant reduction in sheet resistivity. A deposited oxide is then applied, following by a via etch and the plugging of these vias with tungsten to planarize the structure. First level metallization is tungsten with a 2.2 micrometer pitch, while second metal is AlSiCu with somewhat looser ground rules. An oxide glassivation provides protection against ionic contamination and mechanical damage. The process results in a complementary MOS structure with the following device parameters:

Parameter	Nominal Value	Units
N-Channel:		
Leff	.7	micrometer
V_T	1.15	volts
K'	56	$\mu A/V^2$
V_{sus}	6.5	volts
P-Channel		
Leffective	.7	micrometer
V_T	1.10	volts
K'	18	$\mu A/V^2$

Note that the sustaining voltage of the N-channel device is a nominal 6.5 volts, well above the 5 volt supply used for the 256K SRAM. Control of V_{sus} in an SOI process depends on conservative body tie rules. Recognize that the MOS device contains a parasitic lateral bipolar device as well, and that the base width of this device equals $L_{effective}$ of the MOS device. As MOS gate lengths are reduced into the submicrometer range, the parasitic device current gain increases, and V_{sus} drops as a result; careful body tie design reduces this effect. Spacing rules used result in a V_{sus} well in excess of 6.8 volts.

III. PART DESCRIPTION

The Harris HS65758 256K SRAM[1] is a high-speed, radiation-hardened static memory built for space applications, with design and process emphasis on total ionizing dose and single-event upset (SEU) performance. The part is available in 32Kx8, 64Kx4 and 256Kx1 configurations; these are selected by second-metal interconnect options. The part is specified over the full military range of -55°C to +125°C, and runs off a single 5 volt supply. The part is presently being sampled and is in the final stages of process/product qualification, a topic that will be covered later in this paper. Physical design aspects include a die size of 8.31x12.15 mm, or 156000 square mils. Circuit design was specifically optimized for SEU hardness, low standby current and fast memory access time. A 6T memory cell is used with added Miller capacitors to provide optimized SEU performance. Total dose hardness improvements to the basic SOI process flow have resulted in the elimination of the substrate bias found necessary in other SOI components, leading to improved application flexibility. Device leakage improvements allow a 1mA pre-radiation static Idd specification, on which we will show further data. Finally, the device uses multiple redundant memory cell columns to enable correction at wafer probe of random or adjacent defects, improving yield at this step.

IV. PERFORMANCE

The HS65758 has been characterized over temperature and has been found to meet or exceed all design goals. This section provides characterization results for some key parameters. In any static RAM, especially for space applications, the static supply current (Iddsb) is critical, and the stringent 1mA specification for the HS65758 reflects this concern. Figure 1 plots Iddsb as a function of temperature, and it is seen to change little over temperature.

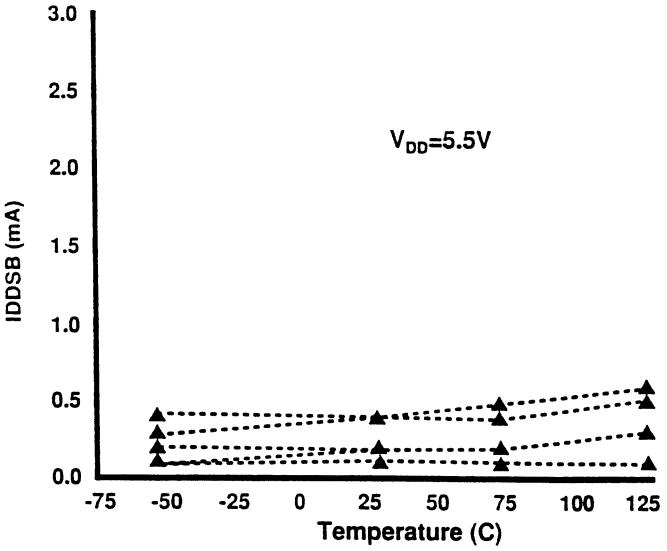


Figure 1
Standby Supply Current (Iddsb) Over Temperature

A key set of performance parameters concerns the AC performance of the memory. We begin by showing (Figure 2) the Address Valid-Q Output Valid delay (t_{AVQV}) as a function of temperature, for both the 4.5V and 5.5V supply voltage cases. Figure 3 similarly shows the minimum write time t_{WLWH} as a function of temperature.

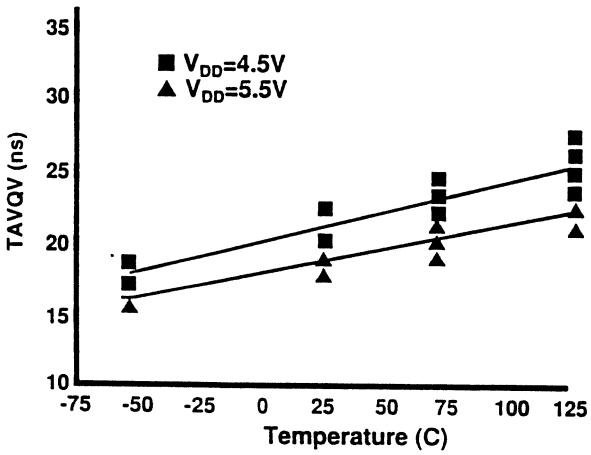


Figure 2
Access Time (t_{AVQV}) Over Temperature

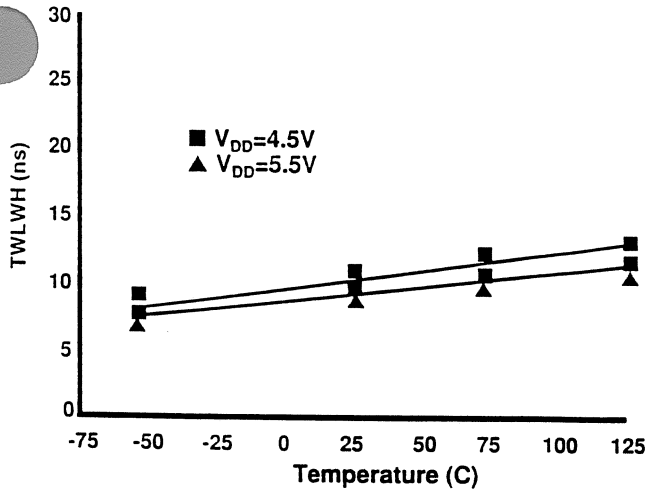


Figure 3
Minimum Write Time (t_{WLWH}) Over Temperature

V. RADIATION EFFECTS

In thin SOI technology with device source/drain regions bottomed out against the buried oxide, the back-gate threshold voltage (V_{TB}) turns into a key issue, especially in its variation over total dose radiation. Clearly, a device structure that enters depletion mode at any point will cause excessive part leakage and, ultimately, nonfunctionality. Figure 4 shows the variation of V_{TBN} as a function of total dose radiation, using a ^{60}CO source at 222 rads(Si)/sec; we study the N-channel device here due to its shift towards depletion mode when irradiated. At levels well in excess of one megarad(Si), the backside N-channel device still retains substantial margin with respect to the 5 volt supply voltage. The curves in Figure 4 also show various bias configurations applied during irradiation.

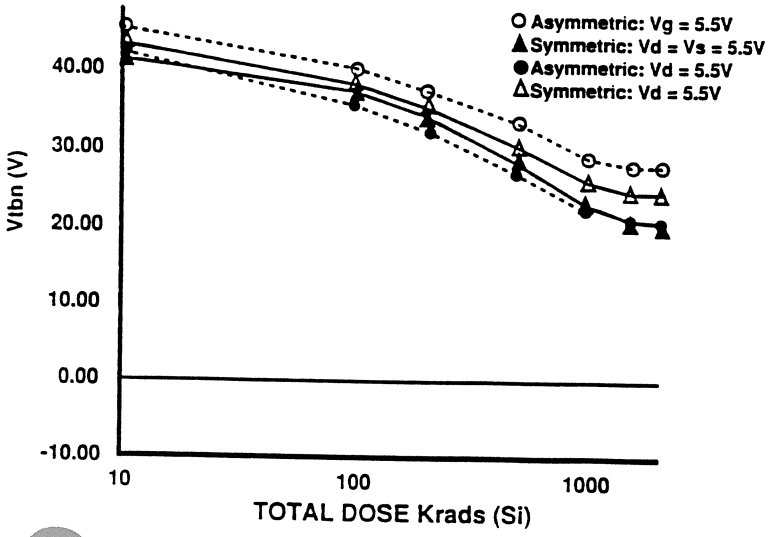


Figure 4
N-Channel Back Gate Threshold Voltage
Over Total Dose Irradiation

Moving next to actual part performance, we first discuss total dose testing. Figure 5 plots standby current as a function of irradiation. Testing was performed in a ^{60}Co Gammacell at 222 rad(Si)/second, at 5.5 volts supply voltage and using no substrate bias. A pattern of logic ONES is written into the memory during irradiation. The standby current shows a monotonic decrease up to one megarad(Si) and then increases again; this is believed to be due to reduction in back-gate P-channel leakage as the threshold voltage of these devices shifts upward.

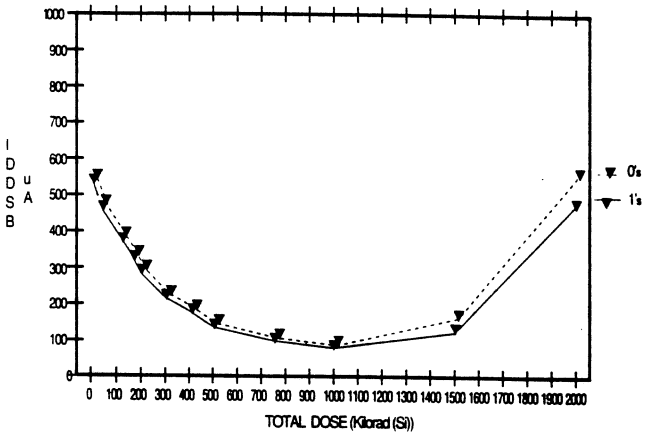


Figure 5
Standby Supply Current (I_{ddsb}) Over Total Dose Irradiation

Figure 6 plots chip enable time (ENABLE high to Q output valid) for the same irradiation conditions. This parameter is seen to change little out to the 2 megarad(Si) maximum level.

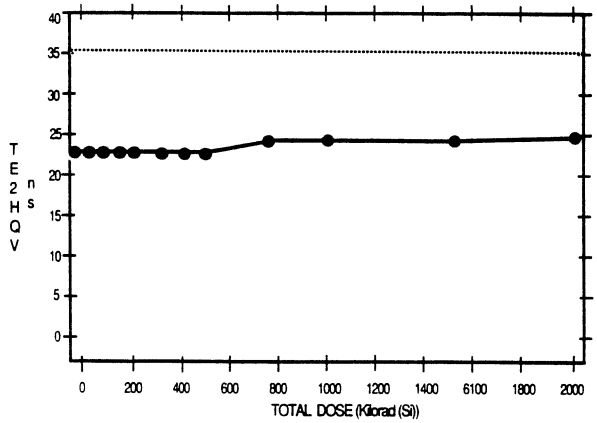


Figure 6
Chip Enable time (t_{E2HQV}) Over Total Dose Irradiation

A second key space radiation issue is single-event upset, and this environment is one of the major reasons for designing e SRAM into SOI technology. SEU testing of the HS65758 was performed at the Brookhaven tandem van de Graaff facility using gold ions at 347 meV and investigating both the room and high temperature cases. Figures 7 and 8 plot cross-section as a function of effective LET for 25° and 125° testing, respectively; applying the CREME code for the Adams 90% worst-case environment yields a 125°C error rate well below $1x10^{-10}$ errors/bit/day. Note we plot data for both 4.5V and 5.5V supply voltage in both cases.

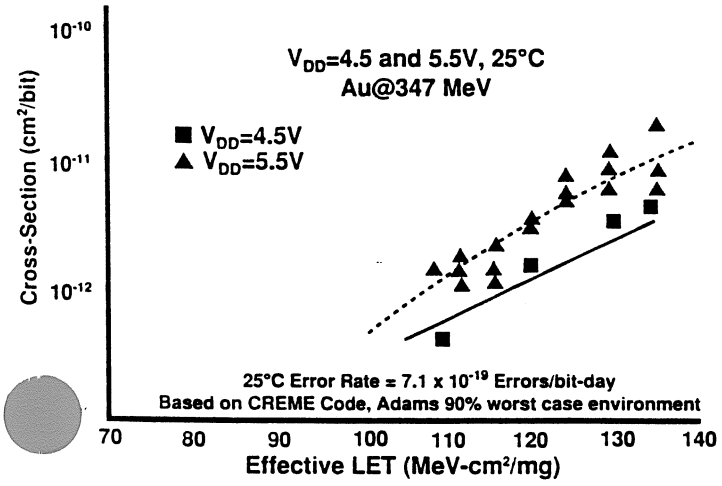


Figure 7
Cross Section as a Function of LET, 25°C Case

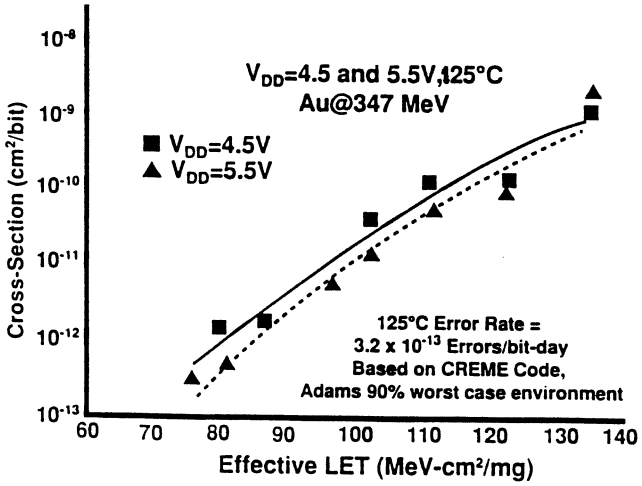


Figure 8
Cross Section as a Function of LET,125°C Case

VI. RELIABILITY ASPECTS

Process and device reliability are obviously key to successful performance in space environments. The RHD-1 process has been evaluated for several key device issues while still in development, leading to a fully engineered and understood process. Areas of investigation have included hot electron effects, basic device stability, dielectric oxide integrity, time-dependent dielectric breakdown and several interconnect-related issues such as electromigration, step coverage and stress-induced voiding. All evaluations have shown acceptable results.(2) Process qualification work has centered on a 64K SRAM Standard Evaluation Circuit (SEC), allowing easier and cost-reduced testing to be carried out. Long-term wear-out testing has passed 2000 hours at 150°C with no failures, either parametric or functional.

VII. CONCLUSION

We discuss a 256K static random-access memory for space applications, implemented in an advanced silicon-on-insulator technology. Results obtained in electrical characterization, radiation testing and reliability evaluations are discussed. The part is being sampled and will be built in a production submicrometer fabrication facility on 6" starting substrates. The HS-65759 will provide a cost-effective solution for SEU-resistant memory for demanding space applications.

VIII. REFERENCES

(1) W.F. Kraus, B.R. Doyle, J.E. Clark, K.L. Jones and D.M. Thornberry, "A 20 ns Multiple Architecture 256K SIMOX SRAM Designed for Harsh Radiation Environments", presented at the 1992 IEEE International SOI Conference, Ponte Vedra, Florida, October 1992.

(2) L. Cohn, H. Hosack, R. Cherne and P. Fechner, "SIMOX Circuit Reliability", presented at the 1993 IEEE International SOI Conference, Palm Springs, California, October 1993.

MILITARY/AEROSPACE REFERENCE MANUAL

DATA CONVERTERS • AMPLIFIERS • ANALOG SIGNAL PROCESSING •
VOLTAGE REFERENCES • SWITCHES AND MULTIPLEXERS •
DATA ACQUISITION SUBSYSTEMS • DIGITAL SIGNAL PROCESSING
COMPONENTS • SPECIAL FUNCTION COMPONENTS •
SPACE QUALIFIED PRODUCTS • RADIATION INFORMATION

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS VOLUME

Contains Data Sheets, Selection Guides and a wealth of background information on military and aerospace products including information on the radiation tolerance of ADI products (see Section 4). In addition, this databook also contains cross references between Analog Devices part numbers and Standard Military Drawings (SMDs) and JAN QPL parts offered by Analog Devices.

This volume is one member of a six-volume set of reference manuals describing and specifying Special Linear, Amplifier, Converter and Audio/Video products from Analog Devices, Inc.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Section-Page location of any data sheet in this volume.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page. Turn directly to the appropriate Section. You will find a functional Selection Tree and Selection Guide at the beginning of the Section. The Selection Tree and Selection Guide will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents is provided for your convenience on pages 1–7 through 1–15.

IF YOU CAN'T FIND IT HERE . . . ASK!

If you can't find the product you are looking for in this databook, please contact your local Analog Devices sales office or phone our Applications Department at 617/937-1428.

See the Worldwide Sales Directory on pages 20–16 and 20–17 at the back of this volume for our sales office phone numbers.

Contents of Other Reference Manuals

AUDIO/VIDEO REFERENCE MANUAL

Operational Amplifiers
Audio A/D Converters
Video A/D Converters
Audio D/A Converters
Video D/A Converters
Special Function Audio Products
Special Function Video Products
Digital Signal Processing Products
Application Notes

DATA CONVERTER REFERENCE MANUAL (VOLUME I)

D/A Converters
S/D Converters
Communications Products
Digital Panel Meters
Digital Signal Processing Products
Bus Interface & Serial I/O Products
Application Specific ICs
Power Supplies

DATA CONVERTER REFERENCE MANUAL (VOLUME II)

A/D Converters
V/F & F/V Converters
Sample/Track-Hold Amplifiers
Switches & Multiplexers
Voltage References
Data Acquisition Subsystems
Analog I/O Ports
Application Specific ICs
Power Supplies

SPECIAL LINEAR REFERENCE MANUAL

Analog Multipliers/ Dividers
Signal Compression Components
RMS-to-DC Converters
Mass Storage Components
ATE Components
Special Function Components
Matched Transistors
Temperature Sensors
Signal Conditioning Components
Automotive Components
Digital Signal Processing Products
Mixed-Signal ASICs
Power Supplies

AMPLIFIER REFERENCE MANUAL

Operational Amplifiers
Comparators
Instrumentation Amplifiers
Isolation Amplifiers
Mixed-Signal ASICs
Power Supplies

If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning 1-800-262-5643.

Radiation Information
Contents

Radiation Effects on Semiconductor Devices

Radiation performance is of critical importance to many of ADI's military customers. Equipment such as satellites will be exposed to ionizing radiation over a period of time. Aircraft, missiles and ships will be subjected to a wide range of effects in a nuclear battlefield environment. There is a major commitment by ADI to supporting customers involved in these programs. This section and the following section are part of that commitment. This section addresses radiation effects on semiconductor devices. The next section discusses specific radiation effects on ADI devices and technologies. The effects of radiation on semiconductor devices are a complex function of radiation type and circuit design. The two sources of radiation are space generated and man made, both of which can be devastating to semiconductor circuits.

Radiation particles can be split into three basic categories: charged particles, neutrons and photons. Electrons with speeds approaching that of light are often referred to as beta particles. The chief offenders that cause damage to military electronic systems are neutrons and photons while space electronic systems are damaged primarily by charged particles such as protons, X-rays and cosmic rays.

Space generated radiation consists of electrons, protons and heavy ion cosmic rays. The radiation from the sun and other galactic sources can be concentrated by the effects of the earth's magnetic fields. This results in bands of higher levels of radiation around the earth. The nuclear battlefield environment can degrade, or even destroy analog integrated circuits that are critical to survival. A nuclear burst generates an X-ray and gamma ray pulse of energy that can have a peak magnitude of 10^{10} to 10^{11} RADs (Si)/sec for hundreds of nanoseconds. These prompt gamma rays travel at the speed of light. Neutrons begin arriving after the prompt gamma rays. Since interactions of the neutrons with the air and ground reduce the energy of the neutrons, the pulse width increases with distance from the nuclear burst. Neutron fluence is given in n/cm^2. The energy spectrum from neutrons depends on the weapon and interactions with other materials.

Nuclear-generated EMP (electro-magnetic pulse) is similar to the phenomenon of lightning. EMP is generated by prompt gamma rays that strip electrons off of air atoms. Shielding must be the primary defense against EMP. In addition, the electronic circuits need to be designed to withstand EMP-induced electrical transients. ICs with good electrostatic discharge tolerance are also of benefit against EMP.

The degradation of performance caused by radiation is the result of two mechanisms: displacement caused by neutrons and ionization produced by gamma rays. Neutron displacement affects the bulk silicon, whereas ionization, the generation of electron-hole pairs, is a surface effect. Both these effects occur as a result of nuclear explosions. The gamma dose rate is many orders of magnitude larger than that experienced in space and results in a much higher level of ionization. Degradation effects are strongly dependent upon transistor structure, processing (particularly temperature steps), circuit layout, and operating current.

The dominant concern of space flight is the long term ionizing effects of Total Dose radiation in RADs (Si), resulting from beta particles, X- and gamma rays. This environment results predominantly in damage to the surface of the devices. Thus the use of surface structures like lateral PNP transistors or CMOS gates are undesirable. It is possible to enhance the radiation performance of these structures with the use of advanced oxidation techniques.

Ionization causes induced leakage currents due to charge trapping at the oxide silicon interface. The removal of electrons from the oxide leaves a net positive charge, which attracts electrons in the silicon resulting in inversion paths effectively changing the surface doping levels. The resulting effect on transistors is to increase leakage and decrease current gain. MOSFET device thresholds shift in the negative direction causing N-channel devices to become depletion mode. This is shown in Figure 1.

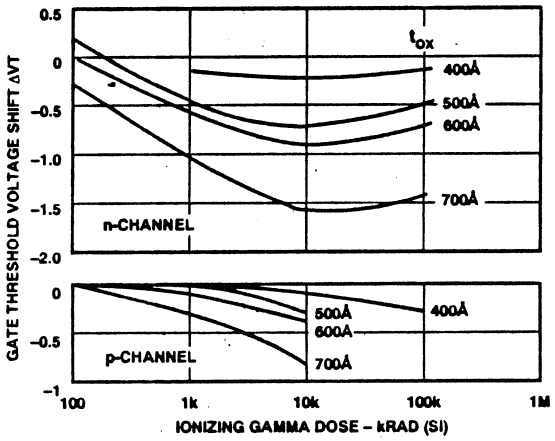


Figure 1. Effect of Total Dose on MOS Transistors

The atomic displacement damage caused by neutron bombardment is independent of applied bias and affects all parameters. In bipolar transistors, it causes an increase in leakage currents and saturation voltages, but most importantly, loss of current gain. It should also be noted that the change in carrier lifetime and resistivity will reduce bandwidth and change circuit resistor values. Figure 2 shows the effects of neutron dose on bipolar transistors with different f_T cutoff bandwidths. Higher f_T transistors are preferred.

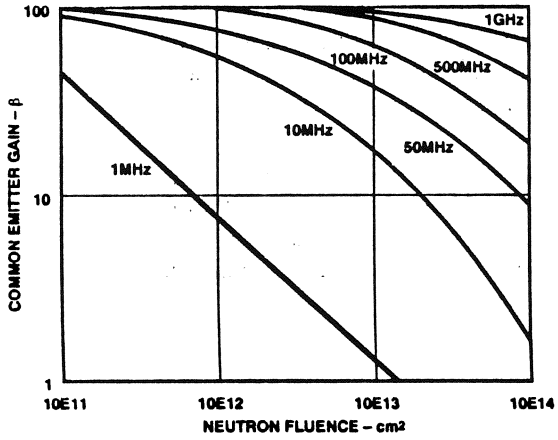


Figure 2. Effect of Neutron on Bipolar Transistor

MOSFET devices on the other hand, are not affected by neutrons except at very high energy levels. This is because 1) MOSFETs are majority carrier devices where minority carrier lifetime degradation is not a factor and 2) they are surface affect devices that are not affected by the bulk silicon damage caused by neutrons.

The photocurrent generated by gamma rays incident on a diode results in increased leakage current. The total leakage for a given dose of radiation depends upon junction size, ionizing level, operating temperature and reverse voltage. Similarly in transistors, photocurrents are generated in both emitter-base and collector-base regions. The combination of junction size and reverse biasing causes the collector-base leakage current to dominate. Typically, the sensitivity will be in the region of 1 pA–100 pA per RAD (Si)/sec. This current is amplified by the transistor resulting in a secondary photocurrent in the collector. It is this current, if large enough, that causes saturation and possibly burn-out.

The exposure of integrated circuits to ionizing radiation results in a variety of performance effects. A radiation pulse of 10 RAD(Si)/sec can generate current spikes sufficient to change logic state, or saturate a LIC (linear integrated circuit). The LIC may remain saturated for several milliseconds after the pulse. Higher levels of radiation can permanently degrade critical parameters such as current gain, leakage current and saturation voltage. It is desirable therefore to select components with tight initial electrical specs. The excessive currents caused by transistor saturation or those produced by SCR latch-up may result in the burn-out of unprotected circuits.

If a transient radiation pulse is sufficient to cause transistor saturation, then the circuit may need a recovery time of many milliseconds. Saturation is of concern for radiation levels on the order of 10^8 RAD (Si)/sec. At even higher radiation levels where the transistors are all driven into heavy saturation or SCR-type latch-up, there is a risk of burn-out. Most linear IC designs have little or no current limiting between positive and negative power supplies. External resistors of at least 2 Ω/V are recommended. A typical op amp operating on ±15 V supplies would need two 30 Ω external resistors. The use of two 100 Ω resistors would be preferable for lower bandwidth application.

Degradation of transistor current gain and increases in leakage currents can cause increased input bias current in op amps and comparators. Under heavy radiation, the NPN transistor may saturate and the collector voltage will drop. Leakages may increase significantly due to photocurrents. Depending on the circuit design, a latch-up condition could occur if the NPN collector voltage drops below the substrate voltage. Conservative design practices can minimize the risk of latch-up under radiation. NPN transistors in their own separate tubs with proper biasing may still saturate, but the parasitic PNP will remain nonconducting.

Photocurrents leaking through the reverse-biased base-emitter junction of the parasitic PNP can be significant. According to the literature and various consultants, a radiation level of 10^8 RAD(Si)/sec will cause photocurrents of 640 A/cm^3. Damage depends on the intensity and duration of the radiation, on the design of the transistor, and on external current-limiting provisions.

The monolithic NPN transistor is electrically isolated from other devices on the same chip by the reverse-biased P-N junction (the isolation wall on the side and the P-type substrate). The P-type substrate is connected to the most negative voltage for the IC. Electrical contacts to the emitter, base, and collector are made at the top surface.

The potential parasitic PNP transistor is formed by the P-type base of the NPN along with the N-type collector and P-type isolation regions (isolation wall and the substrate). In normal operation, the emitter of the parasitic PNP is always at a negative voltage relative to the collector of the NPN (which is the base of the PNP), so the parasitic PNP is reverse-biased and is in a nonconducting state. The subepitaxial N+-type layer reduces the current gain of the parasitic PNP which also helps to hold it off.

The only effective way to avoid latch-up is to remove the parasitic transistor, which is achieved in ADI trench isolation processes. The P-type side wall is replaced with oxide. A trench is etched in the epi-layer and filled with the silicon oxide. The result is a much faster, smaller geometry transistor structure. Examples of these processes at Analog Devices are the STAT-1 process and XFCB process. Both utilize this laterial oxide isolation combined with epitaxy layers and low conductivity buried layer to prevent latch-up.

The effect of an electro-magnetic pulse (EMP) on a system will, at the very least, generate noise spikes, and on an exposed circuit, is likely to result in burn-out. The primary protection against EMP is to use a combination of external shielding and protective circuit elements. ICs with high ESD protection tolerance are also desired.

Radiation-induced EMP transients, or ESD, can damage integrated circuits in several ways. High voltage can rupture a dielectric layer. Metallization can be burned out if the transients generate excessive currents. Transistor junction failure can occur at high energy levels. Some types of integrated circuits, such as MOS or DI, tend to be more vulnerable to EMP/ESD-induced dielectric failure. The ADI process and layout rules for bipolar and CMOS circuits provide good immunity to this failure mode.

Designing linear IC products for operation over the full military temperature range of −55°C to +125°C is already a difficult task. Minimizing the effects of radiation adds another dimension and increases complexity. The need for enhanced radiation hardness may directly conflict with design objectives for the commercial market. At ADI, many of the new linear IC products are specifically designed for military-aerospace use. Design techniques and rules are conservative, and products are fully characterized for operation over the full military temperature range.

When selecting linear IC products for use in a radiation environment, look for circuits that are designed for operation over a wide temperature range. Circuits using NPN or JFET input stages are preferred as is our newer oxide isolated SOI process in development and soon to be available. Figures 3 and 4 summarize the effects of total dose and neutrons on common linear IC parameters.

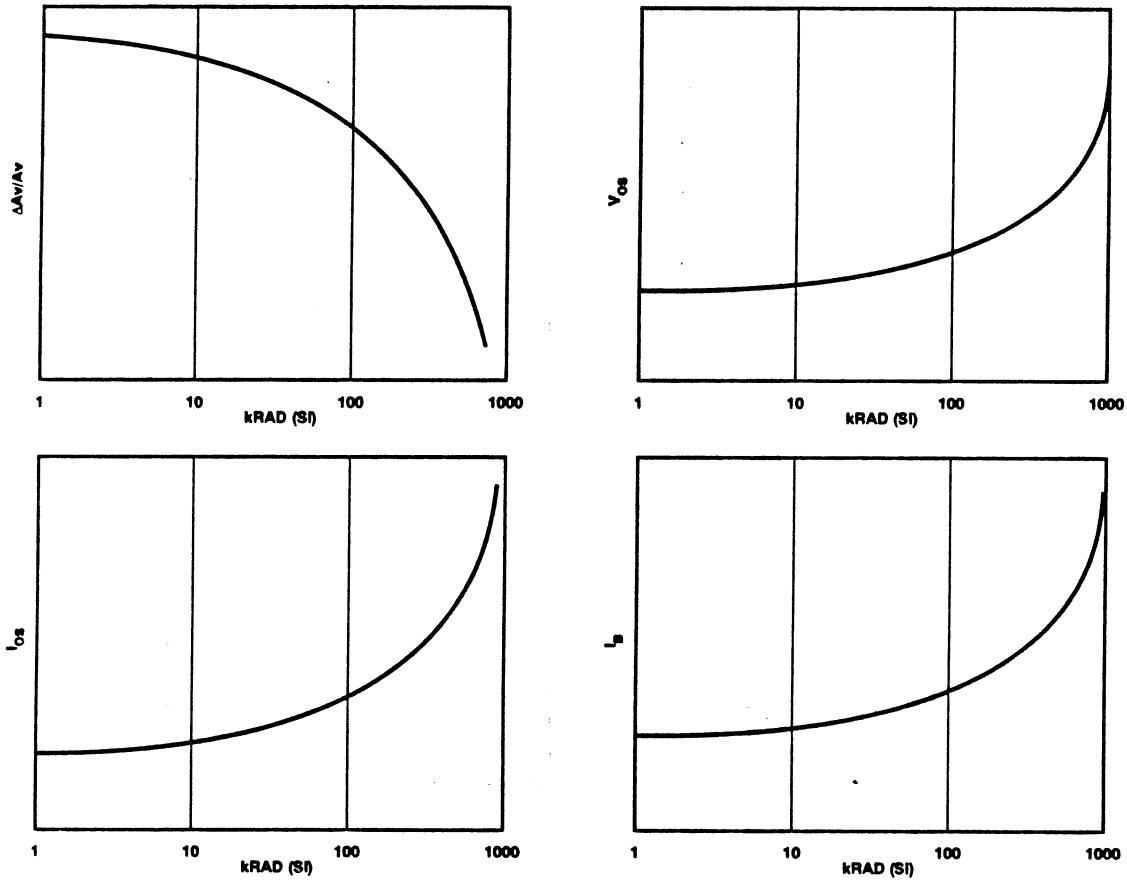


Figure 3. Effect of Total Dose on Linear ICs

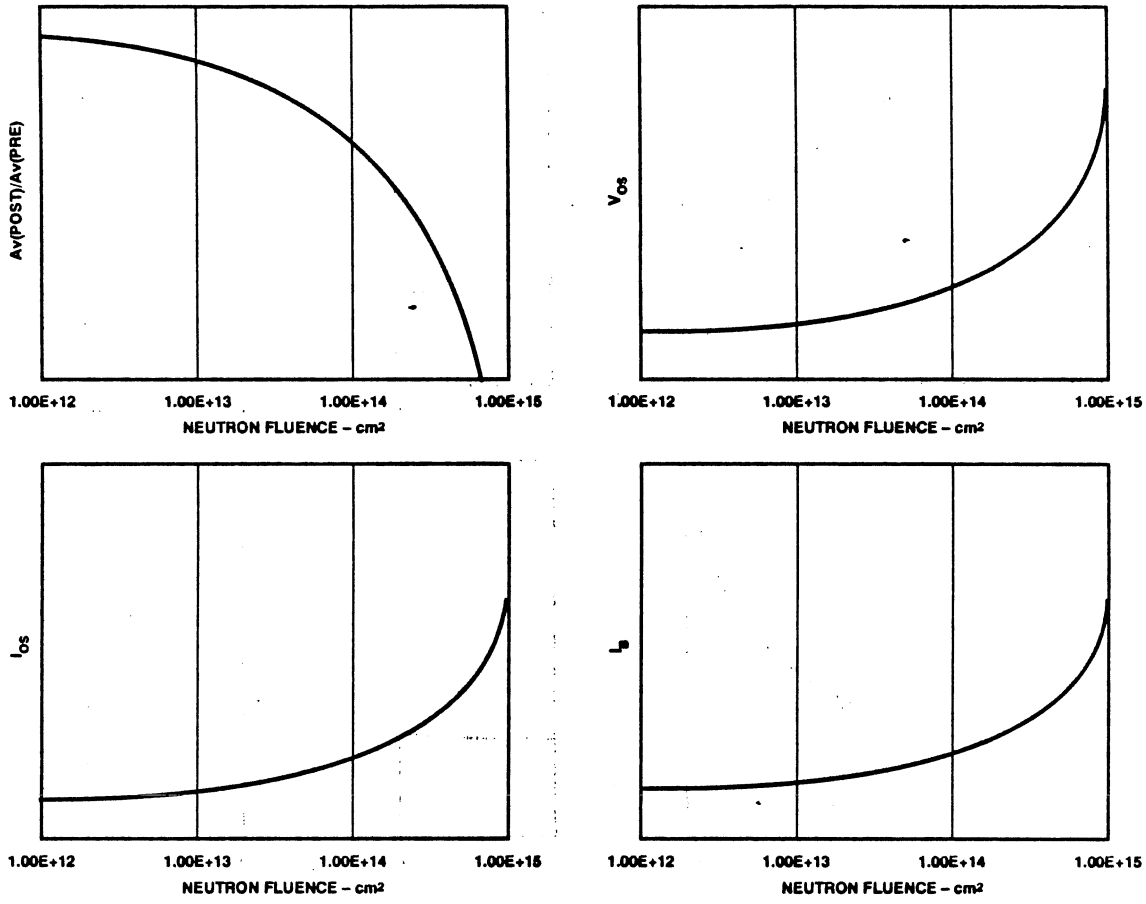


Figure 4. Effects of Neutron on Op-Amp Parameters

Radiation Information on Analog Devices Products

RADTEST^{SM} DATA SERVICE

Through directives of the U.S. Department of Defense and the Ministries of Defense of most countries, all strategic and tactical weapons must now be designed to survive radiation environments consistent with their intended missions. System designers must select components that have been shown to survive the required types and levels of radiation. To aid our customers, Analog Devices offers the RADTEST^{SM} data service. Through this service, customers can obtain radiation-performance information on our products, including data gathered from total-dose, dose-rate, neutron, SEU and SEL testing. You need only to call any of our sales offices to get the latest copy. Our sales engineers can provide this information and assist you in selecting the best product for your application. Our factory radiation-effects experts are available for consultation by calling (617) 937-2685 for this service. In addition, Analog Devices will supply a limited number of free samples of our monolithic products to customers who want to do their own radiation testing and evaluation in exchange for a report of the test results.

ANALOG DEVICES PRODUCT INFORMATION

The products and processes of Analog Devices in general are radiation tolerant. Most of our military-grade products and all of our major wafer-fabrication processes have undergone radiation testing and have passed most of the tactical-level radiation requirements of our customers. Many of the products also qualify for commercial space-system hardness levels. Analog Devices has won many government contracts to develop radiation-hardened products and wafer processes that meet military requirements for hostile-space and strategic environments, for example for the Strategic Defense Initiative.

Table 1 lists our military grade products that have been characterized and shown to be radiation tolerant for most tactical military weapons systems. All of these products exceed a total dose of 1×10^4 RAD(Si), a dose rate of 1×10^9 RAD(Si)/sec, and a neutron fluence of 2×10^{12} neutrons/cm^2. The products in **boldface** exceed a total dose of 1×10^5 RAD(Si). The criteria for classifying these products is that these levels do not degrade a data sheet parameter beyond its specified value for the lowest-grade military product. We recommend that customers ask about the latest characterization results on these and other products as we add them to our RADTEST^{SM} data service.

Analog Devices, Inc., does not guarantee nor take responsibility for maintaining radiation-tolerance levels on any of our products unless under contract to do so. The data supplied by our RADTEST^{SM} data service is for customer information only. For critical applications, we recommend that the customer test and evaluate the products to verify suitability.

All wafer-fabrication, assembly, and test operations, and all design changes are carefully controlled and documented at Analog Devices. Military data sheets and drawings are under documentation control and display revision letters to indicate change status. By selecting our products that considerably exceed program radiation requirements, most customers can satisfy their radiation requirements very economically without expensive testing.

As a further cost savings to our customers, there are no additional charges for our radiation-tolerant products or for the use of our RADTEST^{SM} data service.

Table I. ADI Products That Have Been Tested to Date and Found to Exceed Most Tactical Weapons Radiation Requirements (See text for selection criteria.)

A/D Converters	AD570, AD571, AD573, **AD574**, AD674, AD7572, AD7672, **AD972**, **AD973**, AD1671, AD7820, AD7821, **AD9005**, **AD9048**, AD9002, AD9012, **AD9058**, **ADC910**
D/A Converters	AD392, AD395, AD558, **AD561**, **AD562**, **AD563**, **AD565**, **AD566**, **AD667**, AD7225, AD7245, AD7502, AD7520, AD7522, AD7524, AD7528, AD7541, AD7545, AD7547, DAC08, **DAC100**, DAC312
References	AD580, **AD581**, **AD582**, **AD584**, **AD586**, AD588, AD589, REF01, REF02, REF05, REF10
Amplifiers/SH	**AD582**, AD585, AD640, **AD795**, **AD796**, AD840, AD841, AD842, AD844, AD846, AD847, AD9611, OP01, OP02, OP05, OP06, OP09, OP10, OP11, OP15, OP16, OP17, OP22, OP32, OP37, OP44, OP07, OP27, OP77, **OP160**, OP177, OP42, OP200, **OP260** and OP400 series, OP64, **AD648**, **AD548**, **AD711**, **AD712**, **AD713**, PM108, PM2108, PM155, PM156, PM157, PM4136
Linear Functions	**AD532**, **AD534**, AD536, AD538, AD539, **AD9696**, **AD96687**, AD684
Switches & Muxes	MUX08, MUX16, MUX24, MUX28, SW01, SW02, SW05, SW06, SW201, AD7502, ADG201, ADG202, AD7510, AD7511
Temp Transducer	**AD590**
Digital Signal Microprocessor	ADSP-1010A, ADSP-1016A, ADSP-2100, ADSP-21020
Digital-to-Resolver	DRC1745, DRC1746
Resolver-to-Digital	SDC 1S40, 1S60, 2S80, 2S81
Synchro-to-Digital	SDC1740, SDC1741, SDC1742, SDC1768
Miscellaneous	AD630, AD9500, AD7502, **PM139**, **AD652**, **AD9692**, **AD9901**

Products in **boldface** have withstood a total dose of 1E05 RAD(Si) and still meet data sheet parameters.

RADIATION-TOLERANT PROCESS TECHNOLOGY AT ANALOG DEVICES

Analog Devices products exhibit a high tolerance for radiation across a variety of wafer-fabrication and design technologies. There are many reasons for this. Primarily, we have two decades of experience using proprietary thin-film resistor material to implement the precision circuit elements in our monolithic converters and linear products. This very thin, silicon-based, amorphic material is essentially radiation insensitive and has never been identified as a factor contributing to the radiation degradation of our products. Table 2 shows the radiation tolerance of our major manufacturing process technologies.

In general, our Bipolar Processes show a high degree of radiation tolerance, particularly to total dose. This is because our critical bipolar circuit elements are vertical, highly doped structures and, as such, do not have the sensitivity of MOSFET devices to threshold shifts caused by radiation-induced trapped ionizing charges at the $Si\text{-}SiO_2$ interface. Field-inversion reduction from trapped charges is also reduced because of the higher doping levels in bipolar circuits. Latch-up typically is not a problem for several reasons: the lower substrate resistivity, the use of epi, the use of buried layers, and the conservative layout rules used on these typically low-device-count products. Even though photo currents are high, they generally do not cause device destruction in these high speed products because the metal bus lines are wide enough to handle such currents and the rad-hard, thin-film resistors act as effective current limiters. Finally, neutron tolerance is high because of the high f_T (thin base regions) of the bipolar devices

used in these circuits. This is particularly true for our complementary bipolar, trench, and flash processes. The trench process has very high radiation tolerance because of the device-to-device isolation provided by both the sidewell dielectric isolation, the use of epi, and a low conductivity buried layer below the active devices.

Many of our products made on BiMOS and LC^{2}MOS processes meet minimum tactical-weapons radiation requirements even though they are somewhat lower in resistance to total-dose radiation than our bipolar processes as shown in Figure 1. This lowered tolerance is the result of combining high-temperature bipolar and JFET process steps with the CMOS process. In the case of the Advanced Bipolar CMOS (ABCMOS) process, this problem has been addressed, with significant improvements evident in the radiation hardened version (RBCMOS). Dose-rate tolerance for all three processes is enhanced by utilizing conservative layouts and epi substrates to address the latch-up problem and by laying out wide metal bus lines, which reduce photo-current-induced burnout. The neutron tolerance is extremely high for these three processes, since the bipolar circuit elements have thin base regions, and the MOSFET surface-effect devices are insensitive to bulk damage induced by neutron bombardment.

Our high-density DSP CMOS process has a particularly high total-dose tolerance, exceeding 100 kRAD(Si) at low dose rates on such products as the ADSP-2100. This is because of the fortuitous commonality of the process techniques required both to achieve a high speed, 0.8 μm CMOS source-drain spacing and to minimize radiation-charge trapping in MOS gate and field oxides by the use of thin oxides.

Analog Devices bipolar products generally are not sensitive to the single-event upset (SEU) problem. First, there are no sensitive memory elements on our linear products to be upset by SEU-induced substrate charges. In addition, our products are relatively low-current integrated circuits, and the active devices, when driven by SEU-induced photon currents, saturate at a current level that typically cannot fuse the metal interconnect lines. Finally, the latch-up problem associated with SEL is typically not a problem due to epi isolation and low resistivity substrates.

Table 2. Radiation Tolerance of Analog Devices Processes

Analog Devices' Wafer Processes	Total Dose (RAD(Si))	Dose Rate (RAD(Si)/Sec)	Neutron (N/cm^2)	SEL (LET)
Bipolar I	3E5	1E10	7E12	40
Bipolar II	3E5	1E10	2E12	40
Bipolar III	3E5	1E10	1E12	40
Complementary Bipolar	1E5	9E9	2E12 (Est)	>50 (Est)
STAT-1 (Trench)	1E6	2E10	1E13	>100 (Est)
Flash	5E5	1E9	5E12	>100 (Est)
XFCB (SOI)	1E6	1E10 (Est)	5E12 (Est)	>200 (Est)
BiMOS	1E4	5E9 (Est)	1E13	37
AD7XXX CMOS	2E4	7E9	1E13 (Est)	175
ABCMOS	5E4	1E10	1E13	120
RBCMOS	1E6	1E11	5E13	>100 (Est)
DSP CMOS	1E5	1E9	1E14 (Est)	30

Note: Radiation tolerance of Analog Devices wafer processes based on the highest radiation level that the products survive and still meet lowest-grade data sheet parameters. Since dose rate and SEU/SEL are particularly dependent on circuit design and layout, the levels shown do not necessarily reflect process capability alone.

Table 3. Comparison of Average Radiation Tolerance of all A/D and D/A Converter Products by Two Process Technology Groups

Wafer Process	Total Dose (RAD(Si))	Dose Rate (RAD(Si)/sec)	Neutron (N/cm^2)	SEL/LET ($MeV\text{-}cm^2/mg$)
Bipolar I	113	7E9	2.8E12	40
BiMOS	14	5E9	1E13	37–175

MIXED-SIGNAL ICs

Bipolar processed mixed-signal ICs are generally an order of magnitude harder than those manufactured on BiMOS processes, unless radiation hardening measures are taken. Voltage reference circuits, for example, are generally more radiation tolerant due largely to the fact that they're built on a bipolar process. Both buried-Zener and bandgap references were tested and little difference in circuit performance was noted.

Tests also showed that ADCS and DACS, built on the same wafer process, exhibit relatively equal amounts of radiation tolerance (see Table 4). This is expected since the same basic circuit subfunctions are common to both product types.

Analog's resolver- and synchro-to-digital converters were also tested. In Table 4, all but the monolithic AD2S80 and AD2S81 are hybrids. And a hybrid's radiation tolerance is determined by its "weakest" chip. The AD2S80's total dose is 15 kRAD(Si), neutron fluence is 2E10 N/cm^2, and dose rate is 6E9 RAD(Si)/sec. This monolithic resolver-to-digital converter is manufactured on Analog's proprietary BiMOS II process.

Table 4. Mixed Signal, Linear and DSP Product Families' Radiation Tolerance

Products	AVG	Min	Max
Total Dose (kRAD(Si))			
A/D	46	1	300
D/A	48	5	300
REF	127	17	300
AMP	30	5	200
Linear	420	10	3000
DSP	30	15	50
Resolver/Syn, Con	13	5	15
Neutron Fluence (N/cm^2)			
A/D	4E12	2E12	5E12
D/A	3.5E12	1E12	1E13
REF	7E12	5E12	1E13
AMP	1.5E13	3E9	2E13
Linear	2E13	2E12	1E14
Resolver/Syn, Con	3.6E12	1E10	6E12
Dose Rate (RAD(Si)/sec)			
A/D	4E9	1E9	1E10
D/A	5E9	2E9	1E10
REF	6E9	1E9	1E10
AMP	1.2E10	3E9	3E10
Linear	1.7E12	1E8	1E13
DSP	4E9	4E7	5E9
Resolver/Syn, Con	6E9	3E9	1E10

LINEAR ICs

Linear circuits are a leading contributor to the total radiation sensitivity of a system. Failure of this product class is generally due to excess input bias current and/or offset voltage, causing circuit instability, latch-up, or operation beyond specified circuit parameters. In the case of an amplifier, input specifications are closely related to bipolar device characteristics. Any change to these and matching characteristics contribute to data sheet input specification failures. The current gain to collector current characteristics of an NPN, substrate PNP and lateral PNP transistor is shown in Figure 1.

Linear ICs that use optimally biased NPN transistors in their critical signal path typically exhibit much better radiation tolerance than those using PNP input transistors. Figure 2 clearly displays the minimal effect of total dose radiation on input bias current characteristics of the op amp OP77 which uses vertical NPN input transistors. The input bias current and voltage offset varies only slightly as total doses increases to 100 kRAD, whereas the OP11's I_B *and* V_{OS} performance (Figure 3) is greatly reduced with PNP input transistors.

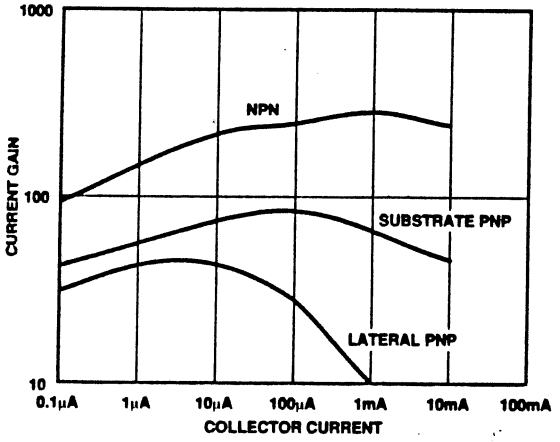


Figure 1.

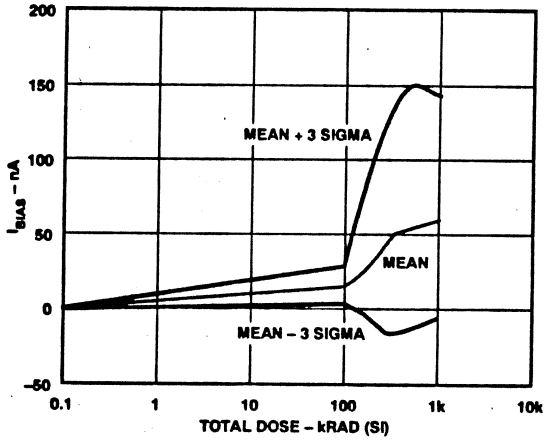


Figure 2. OP77 Input Bias Current

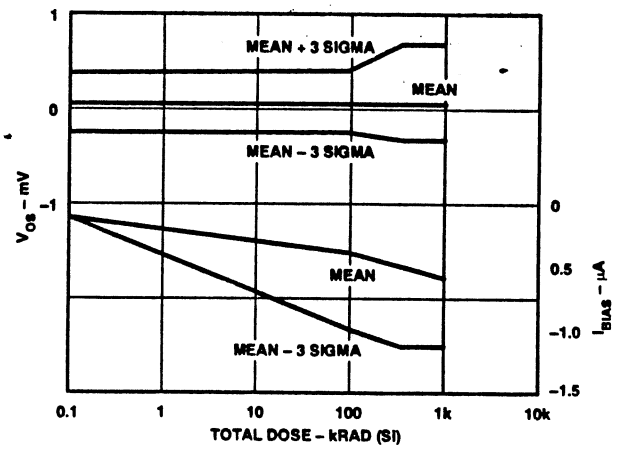


Figure 3. OP11 Input Parameter

Recent results of testing J-FET input op amps has been very encouraging. The AD648 dual, low power, J-FET input op amp was tested up to 200 kRAD and still met specifications. I_B and V_{OS} did not exceed 2.0 nanoamp and 0.5 millivolt respectively. A majority carrier J-FET input stage appears to be much less sensitive to radiation induced junction leakage current than even the NPN transistor stage.

Other linear product functions include analog multiplier/dividers, voltage comparators, and phase discriminators. Analog's AD53x series of multiplier/dividers typically demonstrate total dose tolerances in the 100 kRAD region and exceed 2E12 neutron fluence and 5E9 dose rates. These products are manufactured on a junction-isolated bipolar process. Some AD9xxx products built on Analog Devices' trench-oxide isolated process are among the most radiation tolerant of any semiconductor manufacturer. Total dose can exceed 3 megarads, in some cases with negligible parameter changes. Dose rates of 2E10 and neutron fluence of 1E14 can be achieved on these ICs, and remain within data sheet specifications.

DSPs

Analog's digital signal processor (DSP) family of products include the ADSP-1xxx family of functional building blocks, and the ADSP-2100A complete digital signal microprocessor. All are built on an epi substrate CMOS 0.8 micron process. Total dose levels range from the ADSP-1016A's 15 kRAD(Si) to the ADSP-2100A's 50 kRAD(Si). Neutron testing was omitted due to the high tolerance common to CMOS processing. Dose rates are generally in the high range of 1E9 RAD(Si)/sec for upset. SEU/SEL testing has been completed on the ADSP-2100A, and production units have demonstrated an SEL LET of 14-MeV-cm^2/mg, while specially optimized epi devices range as high as 40-MeV-cm^2/mg LET before latch-up occurred.

RADIATION HARDENING BiCMOS

BiCMOS is the process of choice for space applications and many other low power, high functional density system applications, despite the fact that it has the lowest inherent radiation tolerance of all the processes. Analog Devices' AD2S80 resolver-to-digital converter, built on a BiMOS II process, overcame this problem. The solution was simply to increase the field ion implantation. In order to prevent a reduction in drain breakdown voltage (BV_{DSS}), an expanded active-area mask was used to keep the drain and source junctions from contacting the increased field surface doping. As a result, this product improved from a 5 to 7 kRAD(Si) total dose—enough to pass the RNA level "M" and "D" radiation hardness assurance requirements for tactical military radiation environments.

Similar radiation improvement work has been done under contract to the European Space Agency on future 2-micron LC^{2}MOS selected products. Analog's goal is to reach commercial space radiation levels on selected products (AD7xxx series) in the BiMOS process class.

RBCMOS

The U.S. Army Strategic Defense Command has contracted Analog Devices to work on radiation hardening a BiMOS process. A version of ABCMOS was chosen in order to best design an advanced IR focal plane array interface application-specific IC. The device integrates a 12-bit 10 MHz ADC (AD872) with input multiplexer and auto ranging amplifier and does not dissipate more than 1 W of power. For these types of radiation hardened devices—requiring high-speed precision performance, maximized packing density and low power—the RBCMOS process has been developed. RBCMOS has 3 GHz f_T NPN bipolar transistors with graded base regions to maintain high Early voltage, and a buried collector layer with highly doped plug diffusions to reduce collector resistance. MOS devices are 2 μm CMOS. RBCMOS also features two-layer metal interconnects and laser trimmable thin-film resistors. NPN transistors were found quite tolerant and required little attention.

In order to harden the MOSFET devices to total dose, the single polysilicon deposition used in the commercial process for both the emitter doping interconnections and MOSFET gates had to be modified. The temperature cycling required for the emitter polysilicon diffusion rendered the CMOS gate oxide radiation soft particularly in the bird's beak region. The solution was to use two separate polymasks so that the gate oxide step could be done after the emitter diffusion process. In this way special processing could be done to the gate oxides that would not be perturbed by subsequent thermal processing. The use of guardbanding and higher field doping reduced the susceptibility to prompt-dose induced latch-up and field inversions.

These are just two of the many examples of how wafer processes can be modified to produce inherently better radiation tolerance. Analog Devices uses these techniques on its many in-house DSP, linear- and ixed-signal processes to produce products to meet the demands of today's defense and aerospace arkets.

RADTEST[SM] Data Service

The RADTEST[SM] Data Service is a compilation of radiation test results on Analog Devices' military grade products. It is designed to assist customers in selecting the right products for their applications where radiation is a consideration. Test reports are available on all products listed in the RADTEST[SM] tables. Please be advised that while many products manufactured by Analog Devices, Inc., have been shown to be radiation tolerant to most tactical radiation environments, Analog Devices, Inc., does not make any claim to maintain or guarantee these levels of radiation tolerance unless under specific contractual agreement.

It is the responsibility of the Procuring Activity to screen products from Analog Devices, Inc., for compliance to Nuclear Hardness Critical Items (HCI) specifications.

Product Listing

For radiation test reports on the Analog Devices products in the following section please call:

John M. Hartman
Military/Aerospace Business Development Manager

Analog Devices, Inc., 804 Woburn Street, Wilmington, MA 01887-3462
Tel: (617) 937-2685
Fax: (617) 937-2012

Part Number	Type	Description	Process	Total Dose (kRADs (Si))	Neutron (Neutrons/CM²)	Dose Rate (RADs (Si)/Sec)
AD3[illegible]	DAC	12-Bit, Quad, Voltage Output	Hybrid		1.0E+12	
AD395	DAC	12-Bit, Quad, Four Ref Inputs	Hybrid	<20		
AD396***	DAC	14-Bit, Quad, Four Ref Inputs	Hybrid	<20	>2.0E+12	>1.0E+09
AD507	OP AMP	High Speed, Wideband, Fast Slew	CB			9.0E+09
AD517	OP AMP	Precision, SuperBeta	Bipolar I		3.0E+09	
AD524	IN AMP	Precision In Amp, G = 1 to 1K	Bipolar I		2.0E+12	3.0E+09
AD532	MULT	1 MHz BW, Analog Multiplier	Bipolar I	100		1.0E+13
AD534	MULT	1 MHz BW, Analog Multiplier	Bipolar I	100	3.0E+12	5.0E+09
AD536	RMS-DC	RMS-DC Converter, Gen Purpose	Bipolar I	>48	2.0E+12	5.0E+09
AD537	VFC	150 kHz, Sq Wave, Volt/Freq Conv	Bipolar I		2.8E+12	
AD538	MULT	Analog Computer, Mult/Div/Exp	Bipolar III	10		
AD539	MULT	60 MHz BW, Fast Analog Mult/Div	Bipolar II		3.0E+12	
AD544	OP AMP	Low Ibias, FET	Bipolar I	10	(Vos, Ib only fail)	
AD548***	OP AMP	Low Power, J-FET Input	Bipolar III	200	See AD648 Data File	
AD549	OP AMP	Electrometer, Ultralow Ibias	Bipolar III	10	(Vos only fail)	
AD558	DAC	8-Bit, Voltage Output	Bipolar II	20+	1.0E+12	
AD561	DAC	10-Bit, Current Output	Bipolar I	32–100		5.0E+09
AD562	DAC	12-Bit, Current Output	Bipolar I	50–100		
AD563	DAC	12-Bit, DAC Iout REF	Bipolar I	300	See Other Bipolar IC Products	
AD565	DAC	12-Bit, Current Output	Bipolar II	150	1.7E+13	2.8E+09
AD566	DAC	12-Bit, High Speed	Bipolar II	150	See AD565	See AD565
AD569	DAC	16-Bit, DAC Vout	BiMOS II	10		
AD570	ADC	8-Bit, 25 µs	Bipolar II	75	3.0E+12	See AD574
AD571	ADC	10-Bit, 25 µs	Bipolar II	50	2.0E+12	1.0E+10
AD572	ADC	12-Bit, 25 µs, µP Compatible	Hybrid		1.2E+12	
AD573	ADC	10-Bit, 30 µs	Bipolar II	75		
AD574	ADC	12-Bit, 25 µs Comp, 400 mW	Bipolar II	300	5.0E+12	1.0E+09

Part Number	Type	Description	Process	Total Dose (kRADs (Si))	Neutron (Neutrons/CM^2)	Dose Rate (RADs (Si)/Sec)
AD580	REF	+2.5 V BG Reference	Bipolar I	>17		3.0E+09
AD581	REF	+10 V BG Reference	Bipolar I	300	5.9E+12	7.0E+09
AD582	S/THA	Sample and Hold Amplifier	Bipolar I	300	3.0E+12	
AD584SH	REF	Multitap BG Voltage Reference	Bipolar I	100	5.0E+12	1.0E+10
AD585	S/THA	High Speed, Precision S/H Amp	Bipolar III	25	2.0E+12	1.0E+10
AD586	REF	+5 V BZ Precision Reference	Bipolar III	100–300		
AD588	REF	Programmable Precision BZ Ref	Bipolar III	>25		
AD589	REF	1.22 V Bandgap Ref	Bipolar I	50	See Bipolar IB parts	8.0E+09
AD590	TEMP	Temperature Transducer, 1 μA/K	Bipolar I	100	2.8E+12	8.0E+09
AD598	LVDT	LVDT Signal Conditioner	Bipolar III		3.0E+12	
AD624	IN AMP	High Accry, Low Voltage Noise	Bipolar I	25		
AD630	MULT	2 MHz BW, Balanced Mod/Demod	Bipolar III	75		
AD640	LOG AMP	120 MHz Logarithmic Amplifier	Bipolar III	300	>5.5E+11	8.2E+09
AD648	OP AMP	Dual, Low Power, J-FET Input	Bipolar III	200		
AD652***	VFC	2 MHz V/F & F/V, Pulse Train	Bipolar III	100	2.0E+12	5.0E+09
AD664	DAC	12-Bit, Quad, Low Power	BiMOS II		1.0E+13	
AD667	DAC	12-Bit, Buffered, Voltage Output	Bipolar III	120	2.0E+12	8.0E+09
AD671	ADC	12-Bit, 2 MHz ADC	ABCMOS		2.0E+13	2.0E+10
AD674A	ADC	12-Bit, 15 μs	STAT/FLASH	>33		1.0E+09
AD674B	ADC	12-Bit, 15 μs	BiMOS	10		
AD684***	S/THA	Quad S/H Amp, 12-Bit Accry, 1 μs	BiMOS II	10-15	1E10 to 1E13	2.0E+09
AD707	OP AMP	Precision Amplifier	Bipolar I	25**		
AD708	OP AMP	Precision Amplifier Dual 707	Bipolar III		1.0E+12	
AD711***	OP AMP	Low Distortion FET Op Amp	Bipolar III	200	See AD648 Data File	
AD712***	OP AMP	Dual AD711, Low Distortion	Bipolar III	200	See AD648 Data File	
AD713***	OP AMP	Quad AD711, Precision, Fast, FET	Bipolar III	200	2E12 to 1E13	6.0E+09
AD795***	OP AMP	BiFET, Precision, Low Noise	Bipolar III	200	See AD648 Data File	
AD796***	OP AMP	Dual AD795	Bipolar III	200	See AD648 Data File	
AD829	OP AMP	Video Speed, Low Noise	CB	10	PSRR, Vos Spec	
AD834***	MULT	50 MHz BW, 4-Quad Analog Mult	FLASH	1000	1.0E+13	>2.0E+09
AD840	OP AMP	Wideband, Fast Settling	CB	48**		
AD841	OP AMP	Wideband, Fast Settling	CB	48**	1.0E+13	
AD842	OP AMP	Wideband, Hi Output Current	CB	25**		
AD844	OP AMP	60 MHz, 2000V/μs	CB	>25**		
AD846	OP AMP	WB, Precision, Current Feedback	CB	25**		
AD847	OP AMP	Wideband, Drives Capacitive Loads	CB	25**		
AD972	ADC	12-Bit, 10 MSPS, High Speed	RBCMOS	100	9.5E+13	
AD973	ADC	10-Bit, 18 MSPS, High Speed	RBCMOS	150		>8.0E+09
AD1341***	DAS	12-Bit, 16-Channel Data Acq Sys	Hybrid	20	1.0E+12	
AD1382***	ADC	16-Bit, 500 kSPS	Hybrid	20		
AD1671	ADC	12-Bit, 1.25 MSPS	ABCMOS	80		
AD2700	REF	+10 V Precision Reference	Hybrid		1.0E+13	
AD2702	REF	±10 V Precision Reference	Hybrid			1.0E+09
AD5212	ADC	12-Bit, High Accuracy	Hybrid		2.0E+12	7.0E+09
AD7224	DAC	8-Bit, CMOS, Voltage Out	SAP CMOS	5		
AD7225	DAC	8-Bit, Quad, Voltage Output	SAP CMOS	18		

Part Number	Type	Description	Process	Total Dose (kRADs (Si))	Neutron (Neutrons/CM²)	Dose Rate (RADs (Si)/Sec)
AD7245	DAC	12-Bit, Voltage Output	LOCOS-5	5–25**		
AD7502	MUX	4/8-Channel Multiplexer	HVS CMOS	20		4.0E+09
AD7520	DAC	10-Bit, Multiplying	SAP CMOS	10		2.0E+09
AD7521	DAC	12-Bit, 10-Bit Acc. Inverted R2R	SAP CMOS	8		2.0E+09
AD7522	DAC	10-Bit, Multiplying	SAP CMOS	15		
AD7524	DAC	8-Bit, Multiplying	SAP CMOS	9		
AD7528	DAC	8-Bit, Dual, Multiplying	SAP CMOS	10		
AD7533	DAC	12-Bit, Multiplying Iout	SAP CMOS	6		5.0E+09
AD7541ATD	DAC	12-Bit, Multiplying	SAP CMOS	19		1.0E+10
AD7542	DAC	12-Bit, Multiplying Iout, 4-Bit Bus	SAP CMOS	5		
AD7543	DAC	12-Bit, Multiplying, Iout, Serial	SAP CMOS	5		
AD7545	DAC	12-Bit, Multiplying	SAP CMOS	15–25**		
AD7547	DAC	12-Bit, Dual, Multiplying	SAP CMOS	15		
AD7570	ADC	12-Bit, 100 kSPS, Serial		See AD7672 & AD7543		
AD7572	ADC	12-Bit, 12 µs	LOCOS-5	15–25**		2.0E+09
AD7574	ADC	8-Bit, µP Compatible	LOCOS-3	3–10		4.0E+09
AD7575	ADC	8-Bit, 6 µs, Sampling	LOCOS-3	5		7.0E+09
AD7672	ADC	12-Bit, 10 µs	LOCOS-5	10		
[illegible]	ADC	8-Bit, 2 µs, Sampling	LOCOS-3	15–48**		
[illegible]	ADC	8-Bit, 600 ns, Sampling	LOCOS-3	10		
AD7878	ADC	12-Bit, 10 µs, Sampling	LOCOS-3	1		1.5E+09
AD9002	ADC	8-Bit, 125 MSPS, Flash	BIT	20		
AD9005	ADC	12-Bit, 10 MSPS, Complete	Bipolar	20		
AD9012	ADC	8-Bit, 75 MSPS, Flash	BIT	50		
AD9048	ADC	8-Bit, 35 MSPS Flash	BIT	75		
AD9058	ADC	8-Bit, Dual, 60 MSPS	BIT	25–300		
AD9500	DLYGEN	Delay Generator - 50 MHz	FLASH		2.0E+13	
AD9610	OP AMP	Hybrid Transconductance Amp	Hybrid	5		
AD9611	OP AMP	Wide Bandwidth	Hybrid		2.0E+13	
AD9696	COMP	7 ns Voltage Comparator	STAT I	1000+	1.0E+14	1.0E+08
AD9901	DISCRIM	Hi-Speed, Phase/Freq Discriminator	STAT I	1000	1.0E+13	2.0E+10
AD22302	LVDT	LVDT Signal Conditioner	Bipolar		3.0E+12	
AD96687	COMP	Dual AD96685, 3.5 ns	FLASH	1000+		
ADDAC87	DAC	12-Bit, Voltage Output	Hybrid		5.0E+12	>5.00E+9
ADG201	SWITCH	Quad, SPST, Wide Supply/Signal	HVS CMOS	17		
ADLH0033G	OP AMP	Buffer Amplifier, High Speed	Hybrid			3.0E+10
ADOP07	OP AMP	Precision, Low Offset Voltage	Bipolar I	25**	1.0E+13	
ADOP27	OP AMP	Precision, Low Noise, Fast	Bipolar III	30	(Failed input leakage, otherwise 1 Meg)	
ADREF01	REF	10 V Precision BG Reference	Bipolar		3.0E+12	
ADSP-1010AJD	DSP	16×16 Mult/Accum	CMOS II	40		1.0E+09
ADSP-1016A	DSP	16×16 CMOS Mult	CMOS II	15–25**		1.0E+10
ADSP-1110A	DSP	16×16 Mult/Accum	CMOS II			4.0E+07
ADSP-2100A	DSP	16-Bit, Fixed Point, 122 ns	5–3 V CMOS	50–100		5.0E+09
[illegible]1020***	DSP	32/40-Bit, Floating Point, 33 ns	5–3 V CMOS	>50	>2.0E+121.0E+09	
[illegible]2	VFC	500 KHz, V/F & F/V Converter	Bipolar III		1.0E+12	>1.0E+09
DRC745	RDC	14-Bit, Digital/Resolver Converter	Hybrid	14	6.0E+12	3.0E+09

Part Number	Type	Description	Process	Total Dose (kRADs (Si))	Neutron (Neutrons/CM^2)	Dose Rate (RADs (Si)/Sec)
DRC1746	RDC	16-Bit, Digital/Resolver Converter	Hybrid	14	6.0E+12	3.0E+09
OSC1758/400	SDC	Sine/Cosine Power Amp/Oscillator	Hybrid		1.0E+10	
SDC1740	SDC	14-Bit, Synchro/Digital Converter	Hybrid	15	1.0E+12	1.0E+10
SDC1741	SDC	12-Bit, Synchro/Digital Converter	Hybrid	14	4.0E+12	
SDC1742	SDC	12-Bit, Synchro/Digital Converter	Hybrid	14	4.0E+12	
SDC1768	SDC	12-Bit, Synchro/Digital Converter	Hybrid	15	4.0E+12	3.0E+09
AD2S80A	RDC	Variable Resolution, Tracking	BiMOS II	15	>1.0E+10	
AD2S81	RDC	12-Bit, Monolithic, Low Power	BiMOS II	10		

NOTES:
*The data in this section shows the highest known dose where the lowest grade data sheet parameter did not go out of specification. This summary data is based on test reports on file in the Analog Devices, Inc., RADTEST^{SM} Data Service files.
**25 and 48 kRAD parts tested power down (no bias during irradiation).
***Total Dose, Neutron, and Dose Rate data obtained by analysis.

HEAVY ION RADIATION DATA SUMMARY*

Part Number	Function	Process	SEU - LET (MeV-cm^2/mg)	SEL - LET (MeV-cm^2/mg)	XSection (cm^2)	Heavy Ions
AD562	12-Bit D/A	Bipolar I	15		1 to 10E-06	Cf
AD565	12-Bit D/A	Bipolar II	43		8.0E-05	Cf
AD573	10-Bit A/D	Bipolar II	13		1.1E-04	Cf
AD574	12-Bit A/D	Bipolar II	43		1.0E-04	
AD674B	12-Bit A/D	BiMOS	≤3/4	>120	3.0E-04	I, Br, Ni, CL, F
ADSP2100/883B	DSP µP	Std CMOS, 17 µm Epi	8	12	1.0E-04	Xn, Cf, Various
ADSP2100/883S	DSP µP	Optimized, 13 µm Epi	10	30	1.0E-05	Kr, Cf, Various
AD7543	12-Bit D/A	SAP CMOS		No Latch-up	4.0E-06	Cf
AD7672	12-Bit A/D	LOCOS-5	<40	>175	1.0E-04	Br, I/285, 320 MeV
AD9012	8-Bit A/D	BIT	12–37	37		Br, CL/275, 204 MeV
AD9058	Dual 8-Bit A/D	BIT	12–75	>75		Br, CL/275, 320 MeV
AD9048	8-Bit A/D	BIT	<3.2	7–8	2.8E-04/1.0E-05	Br, CL, Si, F-19
AD2S80	10-16 Bit R/D	BiMOS II	3.38	37	1.6E-04	

NOTE:
*The data in this section is very general due to test condition variations and lack of standards of evaluation. Test reports are available for review by Procuring Agencies.

RADTEST[SM] Data Service

The Radiation Effects Department at Analog Devices maintains a library of radiation test reports. The following table lists a summary of the reports that are available to share with our customers for generic reference. The table identifies as much detail about each test report as was possible to obtain for traceability to the product mask set and the FAB run number. The radiation environment, test date, and levels tested are listed along with the media available. Most test reports are available on PC disks, Lotus 1-2-3 format, that can be printed or loaded into your spreadsheet program.

Database Listing

For radiation information on the Analog Devices' products in the following section please call:

Bob Gardner
Program Manager
Radiation Effects

Analog Devices, Inc., P.O.Box 58020, 1500 Space Park Drive, Santa Clara, CA 95052-8020
Tel: (408) 562-7156
Fax: (408) 727-1853

Product	Mask Set	Run No./ Filename	Media (Note)	Radiation Environment	Test Date	Radiation Test Levels
AD2S80	B2S80	DC9036	H	Gamma RAD(Si)	Feb-91	0-3K-6K-9K-12K-15K
AD534	E534	2154,401,& 454	DH	Gamma RAD(Si)	Apr-91	50K-100K-200K-300K-400K-500K-48Hr-168Hr
AD558		AD558.WK1	DH	Gamma RAD(Si)	Aug-91	0-50K-100K-200K-300K-400K-500K
AD565		DC8728	H	Gamma RAD(Si)	Sep-89	0-20K-50K-100K-200K-72Hr Anneal
		DC9119G	DH	Gamma RAD(Si)	Jan-92	0-50,100,200,300,400,500K-24&160Hr
AD571	D571	d/c 9122/9121	DH	Gamma RAD(Si)	Jun-91	0-50K-100K-200K-24Hr-48Hr-168Hr
AD574A		LOG1086.TD	H	Gamma RAD(Si)	Jul-85	0-30K-75K-150K-300K
	BM574	LOG1126.TD	H	Gamma RAD(Si)	Jul-85	0-30K-75K-150K
		0DC8920G	DH	Gamma RAD(Si)	Dec-89	0-50K-100K-200K-500K-5.5 Hr-1Meg
		DC8932	H	SEU	May-90	
		DC9218	DH	Gamma RAD(Si)	Jun-92	0-50K
		DC9226	DH	Gamma RAD(Si)	Jul-92	0-100K-72Hr-240Hr
AD584		Various	H	Gam,Neut,DRate		G = 300K, N = 1.7E11, DR = 1E10
AD590	C590	d/c 9123	DH	Gamma RAD(Si)	Jun-91	0-50K-100K-200K-300K-400K-500K-1M
AD834		DC9149	H	Gamma RAD(Si)	Mar-93	0,21K,41K,59K,80K,104K,115K,80Hr,235Hr
AD1671			H	Gamma RAD(Si)	Sep-92	0-1.25K-2.5K-5K-10K-20K-40K-80K-160K-240K-320K
AD9002			H	Total Dose	Nov-91	0-50K-100K-150K-200K-250K
AD9012			H	Gamma RAD(Si)	Aug-91	0-10K-50K-100K-250K
AD9048		DC8817	H	Gamma RAD(Si)	Oct-89	0-25K-75K-24Hr-48Hr

Product	Mask Set	Run No./ Filename	Media (Note)	Radiation Environment	Test Date	Radiation Test Levels
AD9617		AD9617	DH	Gamma RAD(Si)	Aug-91	0-10K-50K-100K-250K-500K-1M
AD96687		AD96687	DH	Gamma RAD(Si)	Aug-91	0-10K-50K-100K-250K-500K-1Meg
		DC8951	H	Gamma RAD(Si)	Oct-90	0-50K-100K-300K-500K-1Meg-3Meg
AD9696		AD9696.WK1	DH	Gamma RAD(Si)	Aug-91	0-10K-50K-100K-250K-500K-1Meg
ADSP-2100		Various	H	SEU, Total Dose		
ADC910	1203X-6A	d/c 8829	DH	Gamma RAD(Si)	Jan-91	0-75K-150K-300K-600K-1M
AMP01		DC8913	DH	Gamma RAD(Si)	Jan-90	0-20K-50K-100K-200K
	1411W-6A1	H8466201	DH	Gamma RAD(Si)	Jun-92	0-50K-72Hr-240Hr
		H84668xx	DH	Gamma RAD(Si)	Jun-92	0-50K-72Hr-240Hr
AMP02	1416Y-6B	d/c 9026	DH	Gamma RAD(Si)	Jan-91	0-75K-150K-300K-600K-1M
CMP02		H23929xx	DH	Gamma RAD(Si)	Nov-84	0-600K-1Meg-3Meg
	1501X-6B	H43739xx	DH	Gamma RAD(Si)	Feb-86	0-600K-1Meg-3Meg
		A23929xx	H	Neutron n/cm^2	Apr-85	0-6E12-1E13-3E13
		H43739xx	DH	Neutron n/cm^2	Aug-86	0-2E12-6E12-1E13
CMP04	1504Y-6A	H13537xx	DH	Gamma RAD(Si)	Dec-85	0-100K-250K-500K
DAC05		H41010xx	DH	Gamma RAD(Si)	Mar-86	0-600K-1Meg-3Meg
	1100Y-6A	H41010xx	H	Neutron n/cm^2	Feb-86	0-2E12-6E12-1E13
		H44615xx	DH	Gamma RAD(Si)	May-86	0-600K-1Meg-3Meg
		H44615xx	DH	Neutron n/cm^2	Jul-86	0-2E12-6E12
DAC08		H20872xx	DH	Gamma RAD(Si)	May-85	0-500K-1Meg-3Meg
	1108W-6A	H20872xx	DH	Neutron n/cm^2	Oct-85	0-2E12-6E12-1E13
		H21391xx	DH	Gamma RAD(Si)	May-85	0-500K-1Meg-3Meg
		H21391xx	DH	Neutron n/cm^2	Apr-85	0-6E12-1E13-3E13
		DC8925	DH	Gamma RAD(Si)	Aug-91	0-50K-100K-500K-1Meg-24Hr-240Hr
		DC9140	DH	Gamma RAD(Si)	Nov-91	0-100K-24Hr
		DC8920	DH	Gamma RAD(Si)	Jul-92	0-100K
DAC100		H26646xx	DH	Gamma RAD(Si)	Apr-85	0-600K-1Meg-3Meg
	1106U-6A1/	H35680xx	DH	Gamma RAD(Si)	Oct-85	0-600K-1Meg-3Meg
	1300U-6A	H35680xx	DH	Neutron n/cm^2	Mar-86	0-2E12-6E12-1E13
		H37022xx	DH	Gamma RAD(Si)	Jul-86	0-600K-1Meg-3Meg
		H37022xx	DH	Neutron n/cm^2	Aug-86	0-2E12-6E12-1E13
DAC312		K7264302	DH	Gamma RAD(Si)	Sep-88	0-30K-60K-100K-300K
	1117Y-6B1	K7264302	DH	Neutron/Gamma	Sep-88	0-3E11-30K-60K-100K-300K
		DC8819	DH	Gamma RAD(Si)	Dec-90	0, 75K, 150K, 300K, 600K, 1M
PM108		108LMSC	DH	Gamma RAD(Si)	Jul-87	0-20K-50K-100K
	4002Z-6B	K60408xx	DH	Gamma RAD(Si)	Sep-88	0-75K-150K-300K
		DC8719	H	FLASH X-RAY	Sep-88	Dose Rate testing
		Q75257xx	DH	Gamma RAD(Si)	May-89	0-25K-50K-75K-100K
		Q75976xx	DH	Gamma RAD(Si)	May-89	0-25K-50K-75K-100K
		DC9207	DH	Gamma RAD(Si)	Apr-92	0-10K-50K-100K

Product	Mask Set	Run No./ Filename	Media (Note)	Radiation Environment	Test Date	Radiation Test Levels
PM111	3004Z-6A	B5098726	DH	Gamma RAD(Si)	Sep-88	0-75K-150K-300K-600K-1Meg
	3004X-6B	E86045	DH	Gamma RAD(Si)	Sep-90	0-75K-150K-300K-600K-1Meg
PM119		PM119TD	DH	Gamma RAD(Si)	Jun-87	0-50K-100K-200K
PM139		ENG139G	DH	Gamma RAD(Si)	Oct-85	0-20K-70K-300K-600K
	3003Z-6A	J65562xx	DH	Gamma RAD(Si)	Oct-88	0-75K-150K-300K
		E6527002	H	Neutron n/cm^2	Apr-88	0-1E12-3E12-1E13
		S22273	DH	Neutron n/cm^2	Jun-88	0-1E12-3E12-1E13
		DC8909	DH	Gamma RAD(Si)	Aug-90	0-75K-150K-48Hour-300K
	3003Y-6A	Q9019903	DH	Gamma RAD(Si)	Dec-91	0-100K
		DC9103	DH	Gamma RAD(Si)	Dec-91	0-50K
PM1008	4008Z-6A1	K64241xx	DH	Gamma RAD(Si)	Jul-88	0-75K-150K-300K-600K
PM562	1118Y-6A	d/c 8440	H	Gamma RAD(Si)	Feb-87	0-10K-25K-100K-200K
MAT01	2101X-6A	CIRCA89	H	Gamma RAD(Si)	Dec-89	0-30K-75K-150K-300K
16	1902X-6C	d/c 8852	DH	Gamma RAD(Si)	Nov-90	0-75K-150K-300K-600K-1Meg
OP01	1401S-6B	H23934xx	H	Neutron n/cm^2	Apr-85	0-6E12-1E13-3E13
		H26614xx	DH	Gamma RAD(Si)	Apr-85	0-300K-600K-1Meg
		H26614xx	DH	Neutron n/cm^2	Nov-85	0-2E12-6E12-1E13
		Mixed	H	Neutron/Gamma	Nov-88	0-3.4E12-250Krad
OP07		H27945xx	DH	Gamma RAD(Si)	Feb-85	0-300K-600K-1Meg
	1407X-6A	H27945xx	DH	Neutron n/cm^2	May-85	0-6E12-1E13
	1407W-6A	H71490xx	DH	Neutron/Gamma	Aug-88	0-3.0E12-250Krad
		H71493xx	DH	Neutron/Gamma	Aug-88	0-3.0E12-250Krad
		H71496xx	DH	Neutron/Gamma	Aug-88	0-3.0E12-250Krad
	1407U-6A	H80962xx	DH	Neutron/Gamma	Oct-90	0-6.0E11-250Krad
	(OP207)	H90154xx	DH	Neutron/Gamma	Jan-92	0-6E11-60K-100K-300K
	(OP207)	H90155xx	DH	Neutron/Gamma	Jan-92	0-6E11-60K-100K-300K
OP08		H26316xx	DH	Gamma RAD(Si)	Jan-85	0-300K-600K-1Meg
	1402X-6A	H26316xx	DH	Neutron/Gamma	Nov-86	0-4E12-500K
		H32746xx	DH	Gamma RAD(Si)	Jul-85	0-300K-600K-1Meg
		H32746xx	DH	Neutron n/cm^2	Oct-86	0-2E12-6E12-1E13
		H38746xx	DH	Gamma RAD(Si)	Mar-86	0-300K-600K-1Meg
		H44384xx	DH	Gamma RAD(Si)	Sep-86	0-300K-600K-1Meg
		H44384xx	DH	Neutron n/cm^2	Oct-86	0-2E12-6E12-1E13
		H63094xx	H	Neutron/Gamma	Aug-88	0-2.8E12-170Krad
		H71585xx	H	Neutron/Gamma	Aug-88	0-2.8E12-170Krad
	1402V-6A	DC8825G	DH	Gamma RAD(Si)	Jan-92	0-5K-10K-20K-30K-50K-100K
		H63094xx	DH	Gamma RAD(Si)	Apr-92	0-20K-50K

Product	Mask Set	Run No./ Filename	Media (Note)	Radiation Environment	Test Date	Radiation Test Levels
OP11		H37939xx	DH	Gamma RAD(Si)	Mar-86	0-100K-300K-600K
	1404Y-6B	H37939xx	DH	Neutron n/cm^2	Aug-86	0-2E12-6E12-1E13
		H36440xx	H	Neutron n/cm^2	Mar-86	0-2E12-6E12-1E13
		A8573314	DH	Neutron/Gamma	Feb-92	6E11, 60K, 100K, 300K
OP12		H34141xx	DH	Gamma RAD(Si)	Oct-85	0-300K-600K-1Meg
	1402X-6B	H34141xx	H	Neutron n/cm^2	Mar-86	0-2E12-6E12-1E13
		H37016xx	DH	Gamma RAD(Si)	Oct-85	0-300K-600K-1Meg
		H37016xx	H	Neutron n/cm^2	Mar-86	0-2E12-6E12-1E13
		H21673xx	H	Neutron n/cm^2	Apr-85	0-6E12-1E13-3E13
		H39297xx	H	Neutron n/cm^2	Oct-86	0-2E12-6E12-1E13
		H39297xx	H	Neutron/Gamma	Nov-88	0-3.2E12-170Krad
		Q9069918	DH	Gamma RAD(Si)	Dec-92	0-10K-25K-50K-72Hr-240Hr
OP15/PM155		OP15NEU	DH	Neutron n/cm^2	Jan-86	0-2E12-5E12-2E13
	1406W-6B	H78374xx	H	Gamma RAD(Si)	May-89	0-100Krad
	1406U-6B	DC9207	DH	Gamma RAD(Si)	Apr-92	0-10K-50K-100K
		DC8928	DH	Gamma RAD(Si)	Jul-92	0-10K-50K-100K
		H78423xx	DH	Gamma RAD(Si)	Oct-92	0-10K-50K-100K
OP16/PM156		H25278xx	DH	Gamma RAD(Si)	Feb-85	0-300K-600K-1Meg
	1406W-6C	H25278xx	DH	Neutron n/cm^2	Jun-85	0-2E12-6E12-1E13
		H38424xx	DH	Gamma RAD(Si)	May-86	0-300K-600K-1Meg
		H38424xx	DH	Neutron n/cm^2	Aug-86	0-2E12-6E12-1E13
	1406U-6C1,3B	E73857xx	DH	Gamma RAD(Si)	Jun-88	0-100K-300K-600K
		H73939xx	H	Neutron/Gamma	Dec-88	0-6.0E12-600Krad
		H73938xx	H	Neutron/Gamma	Dec-88	0-6.0E12-600Krad
		H73934xx	H	Neutron/Gamma	Jan-89	0-6.0E12-600Krad
OP17/PM157		H2940501	DH	Gamma RAD(Si)	May-85	0-300K-600K-1Meg
		H2940502	DH	Gamma RAD(Si)	Apr-85	0-300K-600K-1Meg
	1406W-6D	H2940502	DH	Neutron n/cm^2	Feb-86	0-2E12-6E12-1E13
	1406U-6D	H81100xx	H	Gamma RAD(Si)	Jan-90	0-100K-300K-240hr anneal
OP22		d/c 8437	DH	Neutron n/cm^2	Jan-87	0-3E12
		H80145xx	H	Gamma RAD(Si)	Feb-90	0-50K-75K-100K-150K
OP27		E66076xx	DH	Gamma RAD(Si)	Jul-88	0-75K-150K-300K-600K-1Meg
	1427V-6A	DC8733	H	FLASH X-RAY	Aug-88	Dose Rate testing
		J73953xx	DH	Gamma RAD(Si)	May-89	0-1Meg
	1427U-6A	E85384xx	DH	Gamma RAD(Si)	Aug-90	0-75K-150K-300K-600K-1Meg
		DC9126G	DH	Gamma RAD(Si)	Jan-92	0-5K-10K-20K-30K-50K-100K
		DC9123	DH	Gamma RAD(Si)	Jan-92	0-10K-20K-75K-150K-300K-600-1Meg
		DC9143	DH	Gamma RAD(Si)	Jan-92	0-5K-10K-20K-30K-50K
		H1288201	DH	Gamma RAD(Si)	Jun-92	0-25K-50K-100K-72Hr-240Hr
OP37		H21672xx	DH	Gamma RAD(Si)	Jul-85	0-300K-600K-1Meg
	1418Z-6B2	H21672xx	DH	Neutron n/cm^2	Oct-85	0-2E12-6E12-1E13
		H31067xx	DH	Gamma RAD(Si)	Jul-85	0-300K-600K-1Meg
		H31067xx	DH	Neutron n/cm^2	Oct-85	0-2E12-6E12-1E13
OP41		K73670xx	DH	Gamma RAD(Si)	Nov-89	0-1K-4K-7K-30K-100K-300K-1M-2.5M
	1410Z-6A					

Product	Mask Set	Run No./ Filename	Media (Note)	Radiation Environment	Test Date	Radiation Test Levels
OP42		OP42CO	DH	Gamma RAD(Si)	Oct-86	0-50K-100K-150K-300K-600K-1Meg
	1432Z-6A5	K5425403	H	Gamma RAD(Si)	Jun-87	0-10K-30K-100K-300K-1Meg
		K5425403	H	Neutron n/cm^2	Jun-87	0-1E12-3E12-1E13-3E13
		H79581xx	DH	Neutron/Gamma	Jan-90	0-6E11-100K-150K-200K-300K
		H9046301	DH	Gamma RAD(Si)	Jun-92	0-25K-50K-100K-72Hr-240Hr
		Q17053xx	DH	Gamma RAD(Si)	Dec-92	0-100K-72Hr-240Hr
		H90463xx	DH	Gamma RAD(Si)	Jan-93	0, 25K, 50K, 72Hr, 240Hr
		H9046301	DH	Gamma RAD(Si)	Jan-93	0, 25K, 72Hr, 240Hr
OP43	1410Z-6B	OP43DBSE	DH	Total Dose SEM	Jun-86	0-300K-600K-1Meg
OP44	1432Z-6B1	d/c 8743	DH	Gamma RAD(Si)	Jan-88	0-300K-600K-1Meg
OP50		7434/01	DH	Gamma RAD(Si)	Jul-87	0-15K-25K-50K-75K-100K-150K
OP64		K7597102	DH	Gamma RAD(Si)	Oct-89	0-25K-50K-75K-300K-600K-1Meg
	1464Z-6A1	K75971xx	DH	Neutron n/cm^2	Jul-90	0-2E12-6E12-1E13-3E13
		d/c 8911	DH	Gamma RAD(Si)	Sep-90	0-75K-150K-300K-600K-1Meg
		d/c 8635	DH	Gamma RAD(Si)	Mar-87	0-5K-10K-30K-50K-100K
	1415Y-6A1	d/c 8729	DH	Gamma RAD(Si)	Jul-88	0-75K-150K-300K-600K-1Meg
		d/c 8610	DH	Neutron n/cm^2	Dec-86	0-1E12-5E12-1E13
		DC8852	DH	Gamma RAD(Si)	Apr-90	0, 75K, 72Hr, 240Hr
OP90	1490Z-6B	d/c 9022	DH	Gamma RAD(Si)	Oct-90	0-5K-10K-15K-20K-25K
OP97/PM1012		H87705xx	DH	Gamma RAD(Si)	Nov-90	0-10K-20K-30K-40K-50K-75K-100K
	4007Z-6A3	d/c 9009	H	Gamma RAD(Si)	Oct-90	0-20K-50K-100K-200K-Anneal
		DC8943	DH	Gamma RAD(Si)	Jan-91	0-75K-150K
		DC9029	H	Gamma RAD(Si)	Jan-91	0-5K-10K-20K-30K-50K-100K-168Hr, 200K-300K
OP177		K78764xx	DH	Gamma RAD(Si)	Dec-89	0-1K-4K-7K-30K-100K-200K-500K
	1415Y-6A1	DC8923	DH	Gamma RAD(Si)	Nov-90	0-75K-150K-300K-600K-1Meg
OP200	1424Y-6A1	d/c 9024	DH	Gamma RAD(Si)	Nov-90	0-25K-50K-75K-100K-125K
OP215		K67738xx	DH	Gamma RAD(Si)	Nov-88	0-75K-150K-300K-600K-1Meg
	1466W-6A	d/c 8728	DH	Gamma RAD(Si)	Apr-88	0-10K-20K-30K
		d/c 8649	DH	Neutron n/cm^2	Nov-87	0-1E12-2E12-4E12-1E13-2E13
OP215		Q79731xx	DH	Neutron/Gamma	Oct-90	0-6E11-60K-100K-300K
	1466W-6A1	DC8943	DH	Gamma RAD(Si)	Dec-90	0-75K-150K-300K-600K-1Meg
		DC9130	DH	Neutron/Gamma	Aug-91	0-6E11-60K-100K-300K-500K
		Q90454xx	DH	Neutron/Gamma	Jan-92	0-6E11-60K-100K-300K
OP221		H78500xx	H	Gamma RAD(Si)	Jul-89	0-20K-10 day anneal
	1430X-6B	d/c 8803	DH	Gamma RAD(Si)	Apr-89	0-10K-20K-30K
		d/c 8738	DH	Neutron n/cm^2	Nov-87	0-1E12-2E12-4E12-1E13-2E13

Product	Mask Set	Run No./ Filename	Media (Note)	Radiation Environment	Test Date	Radiation Test Levels
OP249		E78781xx	DH	Neutron n/cm^2	Jul-90	0-2E12-6E12-1E13-3E13
	1417Z-6A	d/c 8930	H	Gamma RAD(Si)	Nov-90	0-75K-150K-300K-600K-1Meg
OP260		d/c 8943	DH	Gamma RAD(Si)	Jan-91	0-75K-150K-300K-600K-1Meg
	1460Y-6A1					
OP271		DC8827	DH	Gamma RAD(Si)	Sep-90	0-75K-150K-300K-600K-1Meg
	1425Z-6A1					
OP290		d/c 9032	DH	Gamma RAD(Si)	Dec-90	0-5K-10K-15K-20K-25K
	1492Z = 6A					
OP400		K84028xx	DH	Gamma RAD(Si)	Aug-90	0-75K-150K
	1414X-6A2	H8647501	DH	Gamma RAD(Si)	Dec-92	0-25K-75K-24Hr-240Hr
OP471		DC9026	DH	Gamma RAD(Si)	Dec-90	0-75K-150K-300K-600K-1Meg
	1470X-6A3					
OP490		d/c 9001	DH	Gamma RAD(Si)	Mar-90	0-1-3-10-15-20-30K-312 Hr ANNEAL
REF01/10		H27821xx	DH	Gamma RAD(Si)	Aug-85	0-300K-600K-1Meg
	1800Y-6A	H27821xx	DH	Neutron n/cm^2	Oct-85	0-2E12-6E12-1E13
		H27821xx	H	Neutron/Gamma	Nov-88	0-3.3E12-300Krad
		H29763xx	DH	Gamma RAD(Si)	Aug-85	0-300K-600K-1Meg
		H29763xx	DH	Neutron n/cm^2	Oct-85	0-2E12-6E12-1E13
	1800W-6A1	DC9109	DH	Gamma RAD(Si)	Jan-92	0-5K-10K-20K-30K-50K-100K
REF02/05		H66633xx	DH	Gamma RAD(Si)	May-89	0-1Meg
	1800Y-6B	d/c81-84	DH	Neutron/Gamma	Nov-84	0-3E12-100K-300K-500K-1Meg
		Q85739xx	DH	Gamma RAD(Si)	Feb-93	0-3.5K-7K-15K-35K
REF43		B72580xx	DH	Gamma RAD(Si)	Oct-88	0-300K-600K-1000K
	1802Z-6A1	DC9205	DH	Gamma RAD(Si)	Apr-92	0-20K-50K-100K-24Hr
SMP11		Various	H	Gamma RAD(Si)	Various	Up to 600K
SW06		d/c 8951	DH	Gamma RAD(Si)	Oct-90	0-75K-150K-300K-600K-1Meg
	1905Y-6E					
CMOS Products						
ADC912		DC9217	H	Gamma RAD(Si)	May-92	0-733-1.1K-2.2K-2.5K-3K-4.4K
AD7533		DC9101	H	Gamma RAD(Si)	Apr-91	0-2K-48Hr-3K-72Hr-4K-48Hr-168Hr-312Hr
DAC8222		d/c 8835	H	Gamma RAD(Si)	Jun-90	0-.9K-1.8K-2.7K-3.6K-4.5K-5.4K
	5004Z-8B1					
PM7533		DC8912	H	Gamma RAD(Si)	Aug-90	0-2K-5K

Media Note:
D = Disk,
H = Hardcopy

Product/Process Listing

This section lists the wafer processing technology that is used to manufacture major products at Analog Devices. This information is useful to determine probable radiation tolerance of products not yet tested and listed in the preceding RADTEST^{SM} section of this databook.

HOW TO USE THIS SECTION

If a part is not found in the RADTEST^{SM} section, look the part up in this section and note the wafer process technology used. Then go back to the RADTEST^{SM} section and look for similar part functions and performance manufactured with the same wafer process technology. The resulting radiation information for those parts will likely be similar to the part you are interested in but for which no radiation data is yet available.

Sorting in this section is alphanumeric by the data in the first column. The numeric arrangement is left-justified, thus the model AD1385 appears before the model AD532.

If You Still Need to Test an Analog Devices Part

Analog Devices has the policy to provide free samples of most of our products to agencies and customers wishing to do radiation testing on parts not already listed in RADTEST^{SM} in exchange for a resulting test report and the right to distribute this test report to other customers and agencies under current ITAR rules.

Limited electrical test support may also be provided by Analog Devices at the Wilmington, Massachusetts, and Santa Clara, California, manufacturing and engineering locations. Independent, licensed radiation test facilities are conveniently located near both of these locations at reasonable fees.

If you are interested in such services or you need free copies of test reports or more radiation information on Analog Devices products, please call the following 24-hour hotline numbers:

For "AD" prefixed Analog Devices Parts: (617) 937-2685 (937-2012 fax)

For all other Analog Devices parts: (408) 562-7156 (562-1853 fax)

NOTE: Sorting in this section is alphanumeric by the data in the first column. The numeric arrangement is left-justified, thus the model AD1385 appears before the model AD532.

Part Number	Process	Part Number	Process
AD1334	Hybrid	AD566	Bipolar II
AD1341	Hybrid	AD567	Bipolar III
AD1362	Hybrid	AD568	CB
AD1378	Hybrid	AD569	BiMOS II
AD1385	Hybrid	AD570	Bipolar II
AD1671	ABCMOS	AD571	Bipolar II
AD1674	BiMOS II	AD572	Hybrid
AD2700	Hybrid	AD573	Bipolar II
AD2701	Hybrid	AD574A	Bipolar II
AD2702	Hybrid	AD578	Hybrid
AD2S80A	BiMOS II	AD579	Hybrid
AD346	Hybrid	AD580	Bipolar I
AD380	Hybrid	AD581	Bipolar I
AD386	Hybrid	AD582	Bipolar I
AD390	Hybrid	AD584	Bipolar I
AD394	Hybrid	AD585	Bipolar III
AD396	Hybrid	AD586	Bipolar III
AD507	CB	AD587	Bipolar III
AD509	ELBIP	AD588	Bipolar III
AD510	Bipolar I	AD589	Bipolar I
AD517	Bipolar I	AD590	Bipolar I
AD518	Bipolar I	AD598	Bipolar III
AD521	Bipolar I	AD600	FLASH
AD5212	Hybrid	AD602	FLASH
AD5214	Hybrid	AD603	FLASH
AD5215	Hybrid	AD620	Bipolar III
AD522	Hybrid	AD621	Bipolar III
AD524	Bipolar I	AD624	Bipolar I
AD526	Bipolar III	AD625	Bipolar I
AD532	Bipolar I	AD630	Bipolar III
AD534	Bipolar I	AD632	Bipolar I
AD536A	Bipolar I	AD637	Bipolar III
AD537	Bipolar I	AD639	Bipolar I
AD538	Bipolar III	AD640	Bipolar III
AD539	Bipolar II	AD642	Bipolar I
AD542	Bipolar I	AD644	Bipolar I
AD544	Bipolar I	AD645	Bipolar III
AD547	Bipolar I	AD647	Bipolar I
AD548	Bipolar III	AD648	Bipolar III
AD549	Bipolar III	AD650	Bipolar III
AD5539	FLASH	AD652	Bipolar III
AD558	Bipolar II	AD660	BiMOS II
AD561	Bipolar I	AD664	BiMOS II
AD562	Bipolar I	AD667	Bipolar III
AD563	Bipolar I	AD668	CB
AD565	Bipolar II	AD669	Bipolar II
AD565A	Bipolar II	AD670	Bipolar II

Part Number	Process
AD671	ABCMOS
AD673	Bipolar II
AD674A	STAT/FLASH
AD674B	BiMOS
AD676	BiMOS
AD678	BiMOS II
AD679	BiMOS II
AD682	BiMOS II
AD684	BiMOS II
AD688	Bipolar III
AD689	Bipolar III
AD704	Bipolar III
AD705	Bipolar III
AD707	Bipolar I
AD708	Bipolar III
AD711	Bipolar III
AD7111	LOCOS-3
AD7118	LOCOS-5
AD712	Bipolar III
AD713	Bipolar III
AD7224	SAP CMOS
AD7225	SAP CMOS
AD7226	SAP CMOS
AD7228	SAP CMOS
AD7237	LOCOS-5
AD7243	LOCOS-5
AD7245	LOCOS-5
AD7245A	LOCOS-5
AD7247	LOCOS-5
AD7248	LOCOS-5
AD7248A	LOCOS-5
AD734	CB1
AD741	Bipolar I
AD743	BiFET
AD744	BiFET
AD745	BiFET
AD746	BiFET
AD7501	HVS CMOS
AD7502	HVS CMOS
AD7503	HVS CMOS
AD7506	HVS CMOS
AD7507	HVS CMOS
AD7510DI	HVS/DI CMOS
AD7511DI	HVS/DI CMOS
AD7512DI	HVS/DI CMOS
AD7520	SAP CMOS
AD7521	SAP CMOS

Part Number	Process
AD7522	SAP CMOS
AD7524	SAP CMOS
AD7528	SAP CMOS
AD7533	SAP CMOS
AD7534	SAP CMOS
AD7535	SAP CMOS
AD7536	SAP CMOS
AD7537	SAP CMOS
AD7538	SAP CMOS
AD7541	SAP CMOS
AD7541A	SAP CMOS
AD7542	SAP CMOS
AD7543	SAP CMOS
AD7545	SAP CMOS
AD7545A	SAP CMOS
AD7547	SAP CMOS
AD7548	SAP CMOS
AD7549	SAP CMOS
AD7569	LOCOS-3
AD7572	LOCOS-5
AD7574	LOCOS-3
AD7575	LOCOS-3
AD7576	LOCOS-3
AD7578	LOCOS-5
AD7579	LOCOS-3
AD7580	LOCOS-3
AD7582	LOCOS-5
AD7590	HVS/DI CMOS
AD7591	HVS/DI CMOS
AD7592	HVS/DI CMOS
AD7628	SAP CMOS
AD766	BiMOS II
AD767	Bipolar III
AD7672	LOCOS-5
AD7701	LOCOS-2
AD774	BiMOS II
AD779	BiMOS II
AD780	Bipolar III
AD781	BiMOS II
AD7820	LOCOS-3
AD7821	LOCOS-3
AD7824	LOCOS-3
AD7828	LOCOS-3
AD783	ABCMOS
AD7837	JSOG CMOS
AD7840	LOCOS-3
AD7845	LOCOS-5

Part Number	Process
AD7846	LOCOS-5
AD7847	JSOG CMOS
AD7870	LOCOS-3
AD7874	LOCOS-3
AD7875	LOCOS-3
AD7876	LOCOS-3
AD7878	LOCOS-3
AD790	CB
AD797	CB
AD810	CB
AD811	CB
AD827	CB
AD829	CB
AD830	CB
AD834	FLASH
AD840	CB
AD841	CB
AD842	CB
AD843	CB
AD844	CB
AD845	CB
AD846	CB
AD847	CB
AD848	CB
AD849	CB
AD872	ABCMOS
AD9000	FLASH
AD9002	BIT
AD9005A	Hybrid
AD9012	BIT
AD9020	BIT
AD9028	BIT
AD9032	Hybrid
AD9034	Hybrid
AD9038	BIT
AD9048	BIT
AD9058	BIT
AD9060	BIT
AD9100	STAT/FLASH
AD9300	FLASH
AD9500	FLASH
AD9501	FLASH
AD9610	Hybrid
AD9617	STAT/FLASH
AD9618	STAT/FLASH
AD9630	STAT/FLASH
AD96685	FLASH

Part Number	Process
AD96687	FLASH
AD9696	STAT I
AD9698	STAT II
AD9712B	STAT II
AD9713B	STAT II
AD9720	STAT II
AD9721	STAT II
AD9901	STAT I
ADADC85	Hybrid
ADC908	PM CMOS
ADC910	PM CMOS
ADC912	PM CMOS
ADDAC85	Hybrid
ADDAC87	Hybrid
ADG201A	HVS CMOS
ADG201HS	HVS CMOS
ADG202A	HVS CMOS
ADG221	HVS CMOS
ADG222	HVS CMOS
ADG411	HVS/DI CMOS
ADG412	HVS/DI CMOS
ADG506A	HVS CMOS
ADG507A	HVS CMOS
ADG508A	HVS CMOS
ADG509A	HVS CMOS
ADG526A	HVS CMOS
ADG527A	HVS CMOS
ADG528A	HVS CMOS
ADG529A	HVS CMOS
ADOP07	Bipolar I
ADOP27	Bipolar I
ADOP37	Bipolar III
ADSP-1008	5-3V CMOS
ADSP-1009	5-3V CMOS
ADSP-1010	5-3V CMOS
ADSP-1012	5-3V CMOS
ADSP-1016	5-3V CMOS
ADSP-1024	5-3V CMOS
ADSP-1080	5-3V CMOS
ADSP-1081	5-3V CMOS
ADSP-1110	5-3V CMOS
ADSP-1402	5-3V CMOS
ADSP-2100	5-3V CMOS
ADSP-2100A	5-3V CMOS
ADSP-2101	5-3V CMOS
ADSP-21020	5-3V CMOS
ADSP-2111	5-3V CMOS

Part Number	Process
ADSP-3128	5-3V CMOS
ADSP-3212	5-3V CMOS
ADSP-3222	5-3V CMOS
ADV453	5-3V CMOS
ADVFC32	Bipolar III
ADXL50	BiMOS III
AMP01	PM BiPolar
AMP02	PM BiPolar
AMP03	PM BiPolar
AMP05	PM BiPolar
BUF03	PM BiPolar
CMP01	PM BiPolar
CMP04	PM BiPolar
CMP05	PM BiPolar
CMP08	PM BiPolar
CMP404	PM BiPolar
DAC01	PM BiPolar
DAC05	PM BiPolar
DAC06	PM BiPolar
DAC08	PM BiPolar
DAC10	PM BiPolar
DAC100	PM BiPolar
DAC1508	PM BiPolar
DAC312	PM BiPolar
DAC8012	PM CMOS
DAC8043	PM CMOS
DAC8143	PM CMOS
DAC8212	PM CMOS
DAC8221	PM CMOS
DAC8222	PM CMOS
DAC8229	PM CMOS
DAC8248	PM CMOS
DAC8408	PM CMOS
DAC8412	CB CMOS
DAC8413	CB CMOS
DAC8426	PM CMOS
DAC8800	PM CMOS
DAC888	PM BiPolar
HDS-1250	Hybrid
HOS-050	Hybrid
HOS-060	Hybrid
HTC-0300	Hybrid
MAT01	PM BiPolar
MAT02	PM BiPolar
MAT03	PM BiPolar
MUX08	PM BiPolar
MUX16	PM BiPolar

Part Number	Process
MUX24	PM BiPolar
MUX28	PM BiPolar
OP01	PM BiPolar
OP02	PM BiPolar
OP04	PM BiPolar
OP05	PM BiPolar
OP06	PM BiPolar
OP07	PM BiPolar
OP08	PM BiPolar
OP09	PM BiPolar
OP10	PM BiPolar
OP11	PM BiPolar
OP12	PM BiPolar
OP14	PM BiPolar
OP15	PM BiPolar
OP16	PM BiPolar
OP160	PM BiPolar
OP17	PM BiPolar
OP177	PM BiPolar
OP200	PM BiPolar
OP207	PM BiPolar
OP215	PM BiPolar
OP22	PM BiPolar
OP220	PM BiPolar
OP221	PM BiPolar
OP227	PM BiPolar
OP249	PM BiPolar
OP260	PM BiPolar
OP27	PM BiPolar
OP270	PM BiPolar
OP271	PM BiPolar
OP290	PM BiPolar
OP32	PM BiPolar
OP37	PM BiPolar
OP400	PM BiPolar
OP41	PM BiPolar
OP42	PM BiPolar
OP420	PM BiPolar
OP421	PM BiPolar
OP43	PM BiPolar
OP44	PM BiPolar
OP470	PM BiPolar
OP471	PM BiPolar
OP490	PM BiPolar
OP50	PM BiPolar
OP61	PM BiPolar
OP64	PM BiPolar

Part Number	Process
OP77	PM Bipolar
OP90	PM BiPolar
OP97	PM BiPolar
PKD01	PM BiPolar
PM1008	PM BiPolar
PM1012	PM BiPolar
PM108	PM BiPolar
PM111	PM BiPolar
PM119	PM BiPolar
PM139	PM BiPolar
PM148	PM BiPolar
PM155	PM BiPolar
PM156	PM BiPolar
PM157	PM BiPolar
PM2108	PM BiPolar
PM4136	PM BiPolar
PM562	PM BiPolar
PM7224	PM CMOS
PM7226	PM CMOS
PM741	PM BiPolar
PM7524	PM CMOS
PM7528	PM CMOS
PM7533	PM CMOS

Part Number	Process
PM7541	PM CMOS
PM7541A	PM CMOS
PM7542	PM CMOS
PM7543	PM CMOS
PM7545	PM CMOS
PM7545A	CM1
PM7548	PM CMOS
PM7574	PM CMOS
PM7628	PM CMOS
PM7645	PM CMOS
REF01	PM BiPolar
REF02	PM BiPolar
REF05	PM BiPolar
REF08	PM BiPolar
REF10	PM BiPolar
REF43	PM BiPolar
SMP10	PM BiPolar
SMP11	PM BiPolar
SW01	PM BiPolar
SW06	PM BiPolar
SW201	PM BiPolar
SW7510	PM BiPolar
SW7511	PM BiPolar

Space Qualified Products
Contents

Class S Products

Analog Devices has over 15 years experience in supplying products for military and commercial space applications. We are committed to serve the needs of the world space community through the manufacture of the highest quality data conversion and signal processing products. Over the last two years Analog Devices has qualified for aerospace applications 63 state-of-the-art data conversion and signal processing products that were previously only available as commercial or military Class B products.

Analog Devices' space level operations located in Santa Clara, California, coordinates all space activities, including business development, manufacturing and engineering. There are 177 aerospace qualified parts offered by Analog Devices. For a complete aerospace parts listing, please refer to the latest edition of the "Space Qualified Products from Analog Devices" brochure. This brochure is available from your local Analog Devices sales office, or from the aerospace business development group in Santa Clara, California.

AEROSPACE PROCESSING FLOWS

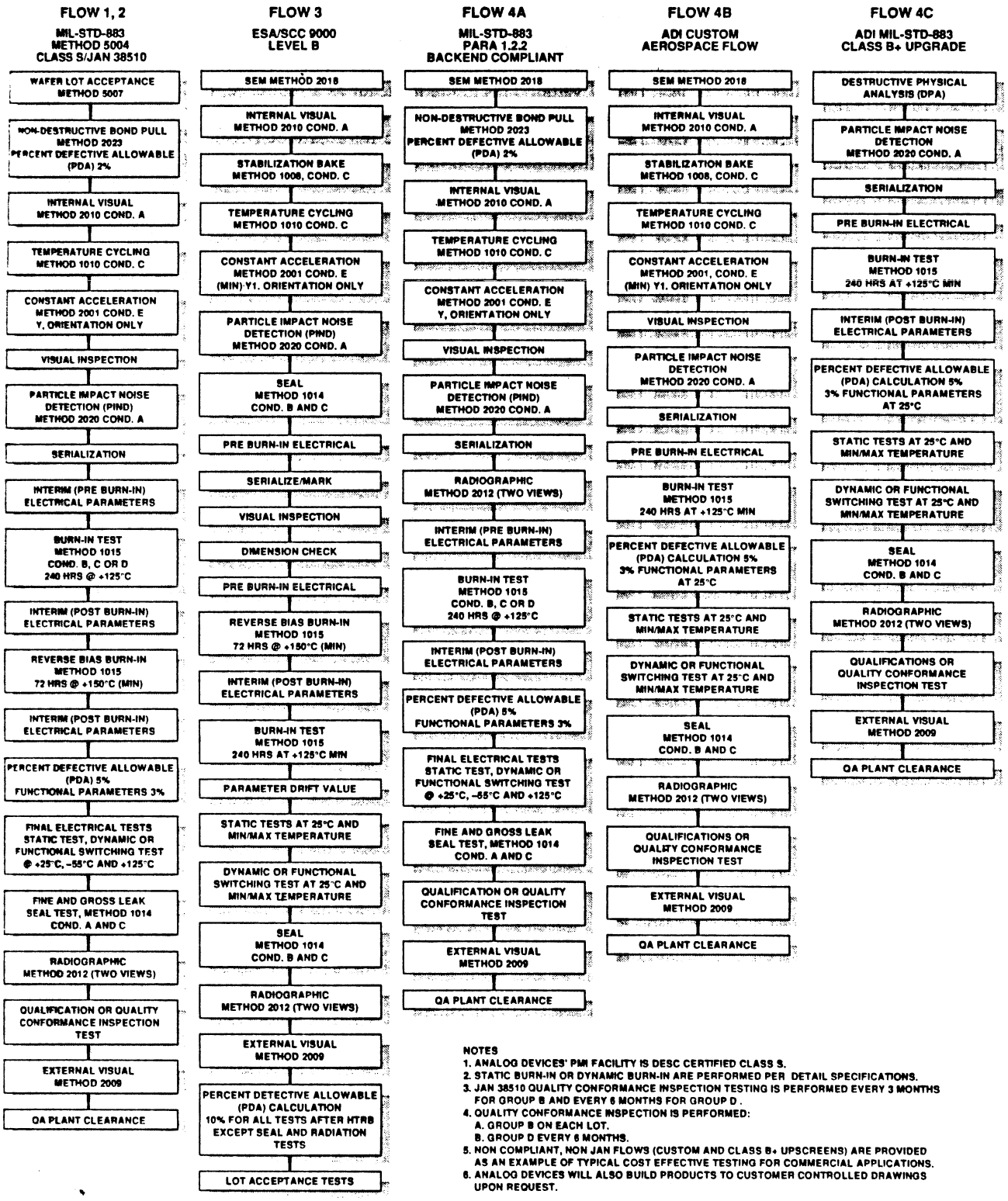
In order to meet the diverse needs of our aerospace customers, Analog Devices offers several aerospace processing flows, as follows:

1. MIL-M-38510, JAN S QPL. Analog Devices offers 25 parts that are certified QPL by the Defense Electronics Supply Center (DESC) of Dayton Ohio. JAN S parts are processed on a certified line, with inspections by a government source inspector. JAN S parts are processed to the electrical requirements of the slash sheet, which is a drawing developed by DESC to define processing for JAN products.
2. MIL STD 883 CLASS S. Analog Devices offers 137 parts which are compliant to MIL-STD-883, Paragraph 1.2.1 for Class S devices. MIL STD 883 Class S parts use many of the processing steps used in JAN S processing. Major differences for 883 S processing (compared to JAN S processing) include source inspection by customer (instead of the government source inspector) and electrical tables per MIL drawing, 883 data sheet or customer source control drawing (instead of JAN slash sheet).
3. ESA 9000 LEVEL B PROCESSING. Analog Devices is fully capable of processing to the requirements of ESA SCC 9000 Level B for European customers. Most of the Class S qualified parts can be made to the ESA 9000 Level B flow.
4. MIL-STD-883 PARA. 1.2.2 Processing. Where Paragraph. 1.2.1 processing is not available or required, the acquiring activity (buyer) needs to specify the MIL STD 883 test methods to be used in the processing. Analog Devices has three Paragraph 1.2.2 Aerospace Processing Flows:
   A) Backend Compliant Class S. For this group of products, the wafer fabrication plant is not a Class S compliant facility. Since the "front-end" wafer fab is not Class S, Analog Devices describes this aerospace process flow as "Backend Compliant Class S," where MIL-STD-883 Class S assembly and testing are performed on the JAN S Line in Santa Clara, California. Analog Devices has 18 products which are Backend Compliant Class S.
   B) Commercial Aerospace "Custom Build" Flow. For noncritical spacecraft and experimental applications, Analog Devices offers commercial aerospace "Custom Build" processing. This flow uses core features of MIL-M-38510 and MIL-STD-883 to achieve reliability goals, yet has shorter throughput time and lower cost. Parts are custom-built to individual customer requirements. Most Class S Qualified Products can be made to this flow.

C) Class B+ Upgrade. For those aerospace customers needing quick delivery and willing to accept standard Class B military parts with additional processing, Analog Devices offers complete upgrade services. Most Class S Qualified products can be made to this flow.

Process Diagrams of the Class S Flows previously described are shown below. For further information about processing and parts options, please contact your local Analog Devices Sales Office or the Aerospace Business Development Group in Santa Clara, California, U.S.A.

CLASS S PROCESS FLOWS



NOTES
1. ANALOG DEVICES' PMI FACILITY IS DESC CERTIFIED CLASS S.
2. STATIC BURN-IN OR DYNAMIC BURN-IN ARE PERFORMED PER DETAIL SPECIFICATIONS.
3. JAN 38510 QUALITY CONFORMANCE INSPECTION TESTING IS PERFORMED EVERY 3 MONTHS FOR GROUP B AND EVERY 6 MONTHS FOR GROUP D.
4. QUALITY CONFORMANCE INSPECTION IS PERFORMED:
   A. GROUP B ON EACH LOT.
   B. GROUP D EVERY 6 MONTHS.
5. NON COMPLIANT, NON JAN FLOWS (CUSTOM AND CLASS B+ UPSCREENS) ARE PROVIDED AS AN EXAMPLE OF TYPICAL COST EFFECTIVE TESTING FOR COMMERCIAL APPLICATIONS.
6. ANALOG DEVICES WILL ALSO BUILD PRODUCTS TO CUSTOMER CONTROLLED DRAWINGS UPON REQUEST.

650222

National Semiconductor

Radiation Guide

RADIATION GUIDE

1992 Edition

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

ABiC™
Abuseable™
Anadig™
ANS-R-TRAN™
APPS™
ASPECT™
Auto-Chem Deflasher™
BCP™
BI-FET™
BI-FET II™
BI-LINE™
BIPLAN™
BLC™
BLX™
BMAC™
Brite-Lite™
BSI™
BSI-2™
CDD™
CheckTrack™
CIM™
CIMBUS™
CLASIC™
Clock✓Chek™
COMBO®
COMBO I™
COMBO II™
COPS™ microcontrollers
CRD™
DA4™
Datachecker®
DENSPAK™
DIB™
DISCERN™
DISTILL™
DNR®
DPVM™
E²CMOS™
ELSTAR™
Embedded System Processor™
EP™
E-Z-LINK™
FACT™
FACT Quiet Series™
FAIRCAD™
Fairtech™
FAST®
FASTr™
5-Star Service™
Flash™
GENIX™
GNX™
GTO™
HAMR™
HandiScan™
HEX 3000™
HPC™
HyBal™
I³L®
ICM™
INFOCHEX™
Integral ISE™
Intelisplay™
Inter-LERIC™
Inter-RIC™
ISE™
ISE/06™
ISE/08™
ISE/16™
ISE32™
ISOPLANAR™
ISOPLANAR-Z™
KeyScan™
LERIC™
LMCMOS™
M²CMOS™
Macrobus™
Macrocomponent™
MAPL™
MAXI-ROM®
Meat✓Chek™
MenuMaster™
Microbus™ data bus
MICRO-DAC™
μtalker™
Microtalker™
MICROWIRE™
MICROWIRE/PLUS™
MOLE™
MPA™
MST™
Naked-8™
National®
National Semiconductor®
National Semiconductor Corp.®
NAX 800™
Nitride Plus™
Nitride Plus Oxide™
NML™
NOBUS™
NSC800™
NSCISE™
NSX-16™
NS-XC-16™
NTERCOM™
NURAM™
OPAL™
OXISS™
P²CMOS™
PC Master™
Perfect Watch™
Pharma✓Chek™
PLAN™
PLANAR™
PLAYER™
Plus-2™
Polycraft™
POSilink™
POSitalker™
Power + Control™
POWERplanar™
QUAD3000™
QUIKLOOK™
RAT™
RIC™
RTX16™
SABR™
SCAN™
Script✓Chek™
SCX™
SERIES/800™
Series 900™
Series 3000™
Series 32000®
Shelf✓Chek™
Simple Switcher™
SofChek™
SONIC™
SPIRE™
Staggered Refresh™
STAR™
Starlink™
STARPLEX™
ST-NIC™
SuperAT™
Super-Block™
SuperChip™
SuperScript™
SYS32™
TapePak®
TDS™
TeleGate™
The National Anthem®
Time✓Chek™
TINA™
TLC™
Trapezoidal™
TRI-CODE™
TRI-POLY™
TRI-SAFE™
TRI-STATE®
TROPIC™
TURBOTRANSCEIVER™
VIP™
VR32™
WATCHDOG™
XMOS™
XPU™
Z STAR™
883B/RETS™
883S/RETS™

PAL® is a registered trademark of and used under license from Advanced Micro Devices, Inc.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, California 95052-8090 1-800-272-9959 TWX (910) 339-9240

Table of Contents

National Semiconductor

Providing a Unique and Cost-Effective Approach to Your Radiation Resistance Needs

Exposure to high-energy radiation can result in transient and/or permanent changes to a semiconductor's material and electrical properties. Use of radiation resistant products, however, can prevent system malfunction or failure.

In harsh space environments, the lack of accessibility to institute repairs as well as the space system's longevity mandate the semiconductors used in these systems maintain the highest reliability levels. Beyond withstanding temperatures that can fluctuate hundreds of degrees within hours, devices are subjected to mechanical stresses that often exceed anything land-based, while radiation particles erratically bombard all aspects of the system in potentially lethal doses. Through all of this, electronic components must retain complete parametric integrity. As man ventures deeper and deeper into space, it is increasingly necessary to harden systems against space's natural radiation environments.

Radiation effects are also a concern for tactical applications. Today's rapidly changing global political climate is significantly impacting the military strategies of all countries. Regardless of political changes, however, nuclear weaponry remains a viable threat. As long as a first-strike capability exists, radiation-hardened strategic and tactical systems will be designed.

Designing and producing radiation-hardened systems is time extensive and financially expensive. Rather than risk premature demise, myriad precautions must be taken to ensure that satellites, for example, will survive their life expectancies. Sometimes orbiting for ten or more years, satellites incur very high costs due to emphasis on performance, reliability, and radiation resistance. Radiation hardening entire systems is a paramount concern.

National's Mil/Aero Radiation Effects Laboratories (REL) in South Portland, Maine, and in Santa Clara, California, certify that products are resistant to defined radiation levels. It is an industry leader in radiation-resistant Logic products. Flexible testing flows meet the needs of strategic, space, and tactical applications. Complete radiation data can be supplied with each order, providing detailed radiation information. Customers may choose JAN Class S and B products or they may specify SCDs to either Level S or Level B process flow. Electrical requirements for post-radiation performance may also be specified by customers' SCDs and may include:

- Fully meeting pre-radiation electrical parameters
- Meeting specified drift limits on specified parameters
- Meeting relaxed post-radiation electrical parameters as defined by customer

THE GROWING RADIATION MARKET

With the advent of more man-made radiation environs as well as growing worldwide interest in exploring and employing the knowledge of space, use of semiconductors in radiation-intensive environments is expanding at an unprecedented rate.

Applications that require radiation resistance are generally segmented as outlined below. The majority of radiation-resistant applications are in the tactical arena and low/high space orbits.

Radiation Resistance Level	Application
0–3 krad	Commercial: industrial, robotic, nuclear, biomedical, space shuttle
3–30 krad	Tactical: submarines, tanks, missiles, airborne, ground (field radar, communications), space station
20–50 krad	Space: low orbit
50–200 krad	Space: high orbit
200 + krad	Deep space Strategic: SDI, military

INCORPORATING RADIATION DESIGN

Most critical at the conceptional stage is a thorough understanding of the system's mission relative to its potential radiation environment. Depending on the mission [i.e., satellite (commercial or military), tactical avionics system (nuclear event), or commercial application (nuclear power plant or medical)], decisions can be made to use different types of components in different circuit applications. Occurring at this stage are proper semiconductor technology evaluation, determination of the extent of shielding, and evaluation of prototype IC technologies that will offer full availability by the time the system is in production.

Exposure to space radiation is generally more severe than in the tactical arena. In the past, radiation-sensitive space systems have been shielded in a variety of materials. But because the payload pound-to-thrust cost ratio is a critical concern, better methods, such as radiation-resistant ICs, are required to harden a system. Where shielding space systems is very expensive, shielding for tactical radiation environments can be economical (notable exceptions are avionic systems, some tank systems, and shipboard equipment).

Shielding remains a viable and economical approach for today's industrial, robotic, nuclear, and biomedical applications.

DEALING WITH AN ARRAY OF RADIATION EXPOSURES

A system exposed to radiation must resist a variety of potentially lethal doses. Gamma rays, cosmic rays, neutrons, electrons, alpha particles, and prompt dose radiation are ever present in space and ground environments. In large doses, all wreak havoc with standard off-the-shelf semiconductors, influencing the dependability and longevity of the system they are in. Exposure to high-energy radiation can change the electrical properties of a semiconductor or even destroy the device.

Initial decisions for space system design are based on whether the use will be military or commercial. Radiation hardness requirements also differ based on low orbit, high orbit, geosynchronous orbit, or polar orbit. Semiconductors in a satellite experience varying degrees of radiation degradation depending on whether they reside on the satellite's exterior panels or are buried within its body. In space environments, major exposure comes from electron/proton irradiation and Single Event Phenomena (SEP).

When designing a tactical system (such as for aircraft, shipboard, ground hardware, or equipment housed in missile silos or ground bunkers), designers must know if that system must operate throughout a nuclear event or if it will be shut down until the event has passed. Systems subjected to a nuclear event must withstand gamma ray dose rate irradiation and neutron radiation.

The commercial environment has the easiest-to-accommodate radiation hardness levels. Although some equipment parts are exposed to severe hostile radiation environments, most parts can be protected with lead shielding or thick cement walls. Major concerns here stem from gamma ray total dose and neutron radiation.

Radiation is essentially generated from two sources:

- Those occurring naturally via the sun, galactic and extra-galactic, the Earth's Van Allen belt, and naturally-occurring radioactive materials found on Earth.
- Those initiated by man, i.e., nuclear burst, nuclear reactors, and biomedical.

System and circuit designers contend with these major radiation environments:

- Total dose ionization (gamma ray)
- Transient irradiation (dose rate/gamma ray)
- Single event phenomena (SEP)
- Neutron radiation
- Electrical magnetic pulse (EMP)

The two most important space radiation effects are Total Dose Ionization (at a low dose rate) and Single Event Phenomena.

In the tactical environment, transient (dose rate) radiation (primarily associated with nuclear explosion) and neutron effects are the major concerns. Neutron radiation is not a concern for CMOS logic radiation design as long as the fluence is under 10^{13}neutrons/cm^2.

At the present time, EMP environments are addressed at the system level, not by the component's technology.

Market Segment Current Needs

Segment	Total Dose	Dose Rate Upset	Dose Rate Latchup	Neutron	Single Event Upset	Single Event Latchup
Tatical	<30 krad (Si)	>1E9 krad(Si)/sec	>1E10 rad(Si)/sec	3E12 neutron/cm^2	N/A	N/A
Space Low Orbit (military)	20–50 krad(Si)	N/A	N/A	N/A	>40 MeV/ (mg/cm^2)	>100 MeV/ (mg/cm^2)
Space High Orbit (military)	100–200 krad(Si)	N/A	N/A	N/A	>40 MeV/ (mg/cm^2)	>100 MeV/ (mg/cm^2)
Commercial Satellites	20–100 krad(Si)	N/A	N/A	N/A	>40 MeV/ (mg/cm^2)	>100 MeV/ (mg/cm^2)
Strategic Systems (military)	>1 Mrad(Si)	1>1E12 rad(Si)	>1E12 rad(Si)	1E14 neutron/cm^2	>40 MeV/ (mg/cm^2)	>100 MeV/ (mg/cm^2)
Nuclear (power plant)	<20 krad(Si)	N/A	N/A	1E14 neutron/cm^2	>40 MeV/ (mg/cm^2)	>100 MeV/ (mg/cm^2)
Robotics and Biomedical	unknown	unknown	unknown	unknown	unknown	unknown

TOTAL DOSE ENVIRONMENT

The total dose environment is a composite of gamma rays, x-ray radiation, and other ionization radiation. The total amount of absorbed radiation energy varies according to the absorption material. As applied to semiconductors, the material is silicon dioxide and total dose is expressed as rad(Si) or rad(SiO_2), respectively.

Total dose radiation can degrade parameters to the point where a circuit's operation is detrimentally affected. For example, increased propagation time can result. Parametric concerns include changes to I_{CC} (standby current), I_{OZ} (TRI-STATE® leakage current), V_{IL}, V_{IH}, V_{OL}, and V_{OH}. Prevention comes through understanding degradation, how device parameters are affected, and how to achieve a radiation-hardened design by properly applying the device in both the circuit and the system.

Ionization radiation in a total dose environment affects the gate and field oxide of a CMOS semiconductor. When gamma rays strike the gate oxide that has an electrical field across it, photons generate electron-hole pairs. The electrons are swept out of the gate oxide leaving the holes behind (trapped charge). This trapped charge causes threshold voltages to change. Trapped-positive charge and interface-state generation combine with subsequent annealing effects to constitute Time Dependent Effects (TDE).

With National Semiconductor's FACT™ logic, the only degraded parameters are I_{CC} (standby current) and I_{OZ} (TRI-STATE leakeage current). All other DC and AC parameters remain within published pre-rad limits.

TRANSIENT (DOSE RATE) RADIATION

In today's military radiation environment, transient (dose rate) radiation is a major concern. Transient radiation is defined as gamma dot ($\dot{\gamma}$).

Transient irradiation is associated with nuclear explosion and is a major concern for designers of tactical equipment. Characterized by a narrow pulse width (usually 3 ns–10 μs) containing a total dose of 1000 rad(Si) or greater, it represents the amount of total dose irradiation given in a specified time interval. Transient radiation is expressed in rad(Si)/sec or rad(SiO_2)/sec.

Because an ionizing pulse occurs at a faster rate than electron holes can be recombined, a dose rate pulse will generate excess charge in a short period of time. Adverse effects of transient irradiation include upset (soft error), latchup, junction burn-out, short transient pulse on the output, and saturated outputs which depend on the amount of photocurrent (excess charge) generated and the output loading.

Semiconductors subjected to transient radiation generate a large magnitude of photocurrent within each device. When a threshold level of excess charge is attained in a CMOS device, adverse effects can cause:

- Device latchup—a parasitic SCR (Silicon Controlled Rectifier) effect that may cause catastrophic failure.
- Junction burnout—also catastrophic to the device.
- Transient upset—a "soft" error that causes temporary degradation. Upset error can be addressed through a circumvention approach, by recycling the computer, or with error detection and correction (EDAC) techniques.

Other effects are short transient pulse on the output and saturated outputs which depend upon the amount of photocurrent (excessive charge) generated and the output loading.

The worst-case scenario for transient latchup testing is a short radiation pulse, high V_{CC} voltage, and high temperatures. This assures that the largest amount of photocurrent can be generated in the shortest amount of time and with the greatest efficiency of electron-hole pair generation. The high temperature causes changes that permit a lower triggering current level of the parasitic SCR. In turn, the parasitic SCR turns ON and the device has latchup.

The worst-case condition for transient upset is a wide radiation pulse (greater than 100 ns), low temperature (generally room temperature), and V_{CC} set at a low voltage. Slower devices have better radiation upset tolerance than faster devices. Sequential logic circuits suffer from "soft" error. Combinatorial logic devices see a "transient" upset before returning to their original output state. The concern with transient upset is that the upset spike may be propagated down the transmission line with sufficient amplitude and energy to cause a sequential circuit to upset.

In addition, upset level sensitivity is affected by:

- The output states of the device
- The relative position between the occurrence of the radiation pulse and the device's clock pulse.

Thin Epi-CMOS, such as FACT, is inherently latchup immune to transient radiation.

SINGLE EVENT PHENOMENA (SEP)

SEP is associated with trapped radiation in space. Observed in the early 1960s, this was not a concern until the late 1970s. As technology evolved to decreased geometries, feature sizes, and gate oxide volume while increasing device speed, the energy required for gate switching was reduced. As a result, low energies (0.5 pico joules) can now switch device gates, making SEP-charged particles an important radiation concern.

SEP hardness design is dependent on mission requirements and circuit application of the part type. Mission requirements affecting SEP design include orbit placement (polar or geosynchronous), space duration, and orbit inclination. Because the Earth's geomagnetic field acts as an energy filter, minimal SEP effects occur in low altitude orbits with inclination angles lower than 45 degrees.

Single Event Phenomena is generated by these charged particles:

- Alpha particles cause upset in sequential logic or memory devices. The weakest of these particles in causing Single Event Effects (SEE), they are caused by decay of radioactive materials. Thorium, a radioactive material used in ceramic packages, is a source for alpha particles.
- High-energy protons originate in the Van Allen Belts or by solar flares. Only protons having energy greater than 10 MeV will cause an SEE problem.
- Heavy ions are also caused by solar flares and galactic cosmic rays. They provide the worst-case SEP environment for electronic space systems.

Detrimental SEP effects on electronic systems include transients, soft errors, and permanent damage. Latchup is the major permanent damage. This and other effects, such as funnel effect, result when a high-energy charged particle passes through a sensitive area.

In general terms, if a device doesn't suffer from Single Event Upset (SEU) or latchup in a heavy ion environment, it will be unaffected in a high-energy proton or alpha environment. If an alpha particle upsets a component, upset or, more likely, latchup will occur in a proton or heavy ion environment.

NEUTRON RADIATION

Neutron radiation causes lattice structure damage in bipolar devices, thereby affecting a device's minority carrier life time and transistor gains. CMOS technology is immune to neutron irradiation below 10^{13} neutrons/cm^2.

RADIATION DESIGN CONSIDERATIONS

Designing a radiation-hardened system requires establishing guidelines based on the system's mission and its required survivability. Following the conceptual phase of system design, components must be determined and selected for the investigative Engineering Development Phase.

Most older logic technologies have low radiation-tolerance limits. Their use, therefore, precipitates costly design-assurance techniques. Mature technologies are also subject to the uncertainties associated with continued assured supply.

While using customized products can reduce the cost of design-assurance techniques, this one-of-a-kind approach significantly extends leadtimes and substantially escalates product costs.

Logic design, and CMOS technology in particular, is inherently hard against radiation degradation. Beyond its high radiation resistance characteristics, advanced CMOS logic (such as National Semiconductor's FACT and FACT Quiet Series™ families) provides the lowest power consumption, high advanced bipolar speeds, high packing density, and high noise immunity. Immune to neutron radiation and offering excellent total dose, transient, and single event effects characteristics, CMOS logic—and FACT logic in particular—should be used in new designs and to replace older technologies. FACT logic has the same low power consumption as HC logic, can operate at much higher clock rates, and is substantially more radiation resistant for vastly improved system performance. In terms of ECL (such as National's F100K 300 Series), while this bipolar technology is very hard in the total dose environment, it is susceptible in neutron and single event effect environments. The recessed oxide and walled emitters of advanced bipolar logic technology (FAST®, ALS) make it susceptible to neutron, total dose, dose rate, and SEE.

To ensure the best Radiation Hardness Assurance (RHA) design, it is necessary to understand how each component will respond in the system circuit, e.g., what electrical parameters are affected by which radiation environments. This includes variable and functionality (attribute) data to the level of radiation failure. Variable data (as performed in a step-stress radiation approach) permits observance of non-monotonic behavior for each electrical parameter's radiation response. For example, standby current of a non-hardened field oxide is non-linear and exhibits significant increases in value above its pre-radiation value. As 90% of all space projects require less than 200 krad(Si), radiation-hardened products such as FACT logic easily provide more than the required amount of resistance.

When designing a radiation-hardened CMOS system circuit, devices which use NAND gates are more tolerant than those with NOR gates. Depending on circuitry, CMOS device response may degrade, e.g., a flip-flop comprised of NAND gates has a different total dose degradation than one using inverters and transmission gates.

As the number of inputs increases for a particular gate, radiation degradation accelerates as total dose levels increase. With increased circuit complexity, radiation degradation shifts from parameter failure to circuit functionality failure. Therefore, a microprocessor may fail functionality prior to circuit parameter failure. This is also true for gate array designs. Each gate array has its own radiation response because of the internal "personalization" of metal connections to each cell; radiation hardness characteristics change with the design of each gate array.

Once a technology is selected, the next step is choosing RHA components to reduce cost, improve reliability, and ensure the system's radiation hardware requirements. RHA component qualification guarantees that devices have end-point electrical values which account for radiation-effects-generated responses. National's FACT AC products are DESC-approved for RHA.

IMPORTANCE OF CHARACTERIZATION DATA

By having characterization data, system designers can review a function's response to each radiation environment and thereby tailor their approach to hardening the circuit and system design. This data also identifies radiation-sensitive parameters, enabling designers to adjust system circuitry for minimal parametric degradation or for evaluating the product's applicability.

Device design margins and circuit design margins are determined from characterization data. However, the most important use of characterization data is to establish parameter-end-point-limits for device qualification.

For example, a device to be used in the tactical environment is typically specified with a radiation level of 3 krad(Si). To eliminate lot acceptance testing, a design margin of 10× total dose level [30 krad(Si)] would have to be attained with an acceptable parametric-end-point limit and no functional failure.

National Semiconductor

Logic Radiation Testing

TEST PHILOSOPHY

National's Mil/Aero Logic group offers a solution to reduce extensive shielding measures while maintaining cost effectiveness. By testing inherently radiation-resistant standard devices, National provides products that offer:

- JAN Class B or S testing, or custom testing as outlined in customer SCDs (Source Control Drawings)
- Guaranteed specifications for reliable radiation designs
- Cost effectiveness
- Timely delivery

Through our Mil/Aero Logic Radiation Program, products are fully qualified wih respect to different radiation environments. Complete total dose radiation data is supplied with each customer order.

National recognizes that radiation resistance needs differ within tactical and space environments. Our radiation testing program is flexible to individually address your radiation and processing needs. Process flows include JAN S and B, Standard Military Drawings (SMDs), MIL-STD-883, and SCDs to Levels S and B.

All of the company's logic and linear radiation research and development is performed in National's South Portland Radiation Effects Laboratory (REL). This REL is:

- Certified by the National Institute of Standards and Technology (NIST).
- Licensed by the Nuclear Regulatory Commission (NRC) to handle neutron-irradiated material. This capability permits testing product for both total dose and neutron irradiation. National currently contracts Sandia National Labs to perform neutron irradiation.
- Certified by the Defense Electronics Supply Center (DESC) for Total Dose Lab Suitability. This signifies that our REL meets all government requirements to perform total dose testing. This certification is one of only two presently granted by DESC.
- Lab Suitability certification denotes that testing performed at National's South Portland REL facility and the data generated are fully recognized and acceptable by all government agencies, their contractors, and subcontractors. This qualifies the South Portland REL to support JAN Class S RHA programs for FACT product as well as for any customer-requested testing that requires total dose data from a DESC-certified laboratory.

REL research includes evaluation of National's logic families as well as any other products requested by customers.

TEST METHODOLOGY

Under National's test methodology, sample devices are tested to establish the peak radiation operating levels of each FACT, FACT Quiet Series, FACT FCT, and F100K 300 Series ECL function. While "pass/fail" or attribute testing is important, National's Mil/Aero Logic REL endorses parametric or variable testing. These test results are based on step-stress irradiation responses.

National's wafer radiation testing provides consistent device radiation tolerance performance. Wafer testing eliminates any variability from lot-to-lot or wafer-to-wafer. All devices have complete lot and wafer traceability, and each device is guaranteed to be compliant with your SCD. In fact, typical test results exceed the minimum requirements specified in customers' SCDs.

Comprehensive data reduction and statistical analysis is performed and provided with each order, including electrical performance based on device test results and radiation testing with compliance to Level S and Level B process flows. National also offers customers an opportunity to review test results prior to accepting products from any particular wafer.

Offering the best partnership relationship possible, we work with you to ensure that all testing completely suits your needs.

THE STEP-BY-STEP PROCESS

Mil/Aero Logic processes radiation-resistant FACT, FACT Quiet Series, FACT FCT, and F100K 300 Series ECL products under these guidelines:

1. All wafers are fabricated according to Level S specifications. This includes SEM (Scanning Electron Microscope) inspection of two metallization steps and wafer lot acceptance data.
2. Each wafer selected for radiation testing is classified as a "wafer lot" and is stored in a wafer bank for radiation-hardened product.
3. Total dose testing is performed at room temperature (+25°C) in full accordance with MIL-STD-883, Method 1019.4
4. The twelve (minimum per wafer) radiation test die subjected to testing are chosen just beyond the DESC area. This DESC area is defined as that part of the wafer enclosed by ⅔ of the wafer's radial dimension as drawn from the center toward the edge of the wafer. Die within this area are utilized if the customer invokes this JAN requirement. Otherwise, die just beyond the DESC area are used.
5. Sample die is packaged in a ceramic DIP then irradiated.
6. Every product type is qualified under worst-case bias conditions for total dose radiation response on a step-stress irradiation basis, e.g., at radiation interval levels of 3 krad(Si), 10 krad(Si), etc., up to 100 krad(Si).

7. Radiation characterization includes determining the total dose level where parametric and functionality failures occur. The lowest total dose failure level is dictated by whichever failure occurs first—parametric or functionality.
8. Each completed wafer that is accepted for radiation-qualified products is die-banked for future use.
9. A customer may purchase a whole or partial wafer lot. If the entire lot is purchased, the radiation-qualified wafer is die banked pending the customer's release of the remaining die or until all usable die from that lot are delivered. If only a small quantity of die is purchased from a radiation-qualified wafer lot, the die balance remains available to other customers.
10. Various types of data are provided to the customer, i.e., raw data, statistical data, delta data, or box plots (distribution) of the radiation data, as requested on the customer SCD.
11. There are several approaches to purchasing radiation-guaranteed product. Radiation-hardened space products generally incur the highest cost due to the extra non-radiation test issues and requirements of Level-S processing.
12. Wafer and lot traceability are automatic on **all** FACT, FACT Quiet Series, FACT FCT, and F100K 300 Series ECL radiation-resistant products.
13. Radiation data on National's logic products is guaranteed if NSC in South Portland, Maine, performs the radiation tests.

COMPLETE TESTING AND CHARACTERIZATION

Total dose testing is performed by National Semiconductor in South Portland, Maine, using an NRC-licensed and NIST-certified Gammacell 220. Both IN-FLUX and Remote radiation testing are performed on each device type. After each total dose radiation level, MCT automatic testers are used to perform complete parametric and functional testing. All irradiation testing is performed in full accordance with MIL-STD-883, Method 1019.4. As requested by our customers, other testing can also be completed. FACT wafer fabrication is DESC-certified to JAN Class S.

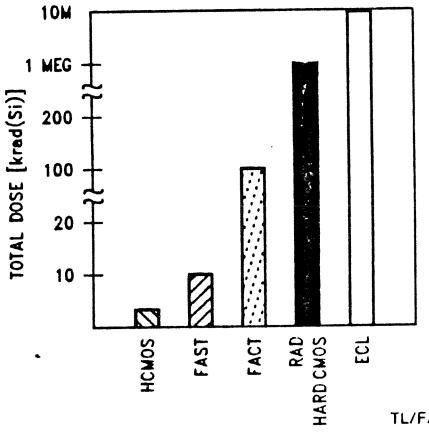
National's Mil/Aero Logic testing goes beyond radiation qualification. Research & Development radiation testing is regularly performed, providing insight to threshold voltage shifts, field oxide hardness, time dependent effects, and more. Radiation testing is performed on transistors, diodes, and capacitors of wafer fab process monitors. As progress is made toward more in-depth understanding of various radiation effects, changes in processing, layout, and circuit design will occur to increase FACT logic's radiation resistance.

Transient radiation testing has been performed on FACT product by Boeing Radiation Effects Lab (BREL) in Seattle, Washington. These tests verify the inherent latchup-free capability of FACT-Epi product. FACT products have been manufactured on a thin Epi-CMOS process with low-resistivity material since December, 1987.

Upset data is also available. While sequential circuits and memories (SRAM) will suffer from a soft error (upset), a system's design approach can correct this problem. However, combinatorial circuits experience temporary upset before recovering to its original state.

Total Dose Test Results

Technology	Recommended Up To
CMOS Technologies:	
FACT AC (2.0 micron process)	200 krad(Si)
FACT ACT (2.0 micron process)	100 krad(Si)
FACT Quiet Series (ACQ) FACT Quiet Series (ACTQ) FACT FCT	Preliminary testing indicates that these families are resistant in excess of 30 krad(Si). Further testing will determine the maximum level.
TTL Technologies:	
FAST	7 krad(Si)
ECL Technologies:	
F100K 300 Series ECL	>1Mrad(Si)



TL/F/11301–22

FACT Logic (AC and ACT)

- FACT products are insensitive to neutron radiation up to 10^{13} neutrons/cm^2.
- Single Event Phenomena latchup is not a problem.
- FACT AC/ACT are guaranteed to 100 krad(Si) with post irradiation parametric limits (PIPL).
- Low voltage (3 volts) parameters for 54ACxxx products begin to degrade between 300–500 krad(Si), depending on part type; for 54ACTxxx, 250–500 krad(Si). Normal (4.5V–5.5V) functionality failures for some devices occur after 1 Mrad(Si).
- I_{CC} (standby current), I_{OZ} (TRI-STATE Standby Current), and I_{CCT} (54ACTxxx products)— are the only DC parameters that are radiation-sensitive and that may require change from National's Table 1 limits.
- All other parameters are within +25°C Table 1 limits.
- Testing results vary from part type to part type due to inherent differences in internal device circuitry.

FACT is the optimum logic family for radiation-resistant designs, providing low power, high performance, and radiation resistance to cost-effectively reduce weight and board

space. Its products are ideally suited for use in logic-based systems and for interfacing with ASIC designs in all applications requiring radiation-resistant devices.

Logic Family	Low Power	High Performance	Radiation Resistant
FACT	X	X	X
HC	X	—	—
HCS	X	—	X
F100K 300 Series ECL	—	X	X
FAST	—	X	—
ALS	—	—	—
LS	X	—	X

FACT's resistance to ionizing radiation is attributable to a thin-gate oxide, p-well design, and low-temperature fab processing. Its Epi (epitaxial layer) and low-resistivity substrate provide inherent latchup resistance under dose rate and SEP conditions. The FACT product portfolio spans the complexity gamut from the simplest SSI functions to high-speed octal buffers and drivers as well as LSI functions. Guaranteed MIL-Class 3 (greater than 4,000 volts) electrostatic discharge (ESD) protection is typical for all FACT functions. All FACT products are manufactured in a DESC-certified JAN Class S wafer fabrication facility.

TOTAL DOSE TEST RESULTS

FACT logic provides high resistance in all radiation environments. For total ionization dose, its 100 krad(Si) capability provides the same post-irradiation drive as its pre-radiation value with propagation time deltas of less than 0.5 ns at high dose rate levels. At lower space dose rates, FACT logic is superior to other logic families. FACT is resistant to total ionization radiation because of its thin gate oxide and low temperature processing.

NOTE: National only subjects its JAN-certified FACT wafers to radiation testing. Because the SMD and JAN processes differ, it should not be presumed that JAN FACT radiation performance characteristics also pertain to FACT SMD products.

National is in the process of qualifying FACT devices to RHA (Radiation Hardness Assurance) standards. Select FACT JAN devices now bear an "R" designation as part of the JM38510 Slash Sheet number, denoting RHA certification to 100 krad(Si).

Radiation Tolerant Qualified FACT AC Product

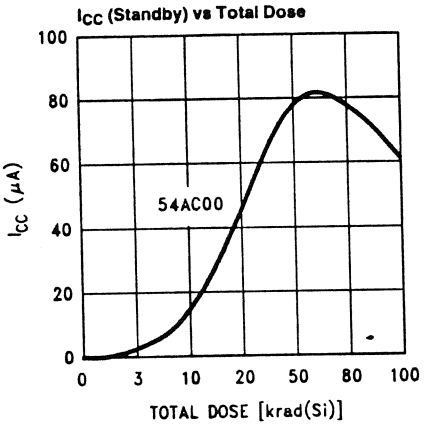
Exceptions: Parameters Which Do Not Stay Within Pre-Rad Values

Device Type	Parameter	@ 3 krad(Si)	@ 10 krad(Si)	@ 100 krad(Si)	Post Anneal
54AC00	I_{CC}	15 μA	75 μA	500 μA	40 μA
54AC02	I_{CC}	15 μA	75 μA	500 μA	40 μA
54AC04	I_{CC}	15 μA	75 μA	500 μA	40 μA
54AC08	I_{CC}	15 μA	75 μA	500 μA	40 μA
54AC10	I_{CC}	15 μA	75 μA	700 μA	40 μA
54AC14	I_{CC}	15 μA	350 μA	700 μA	40 μA
54AC20	I_{CC}	15 μA	75 μA	500 μA	40 μA
54AC32	I_{CC}	15 μA	75 μA	700 μA	40 μA
54AC74	I_{CC}	15 μA	75 μA	500 μA	40 μA
54AC86	I_{CC}	50 μA	200 μA	500 μA	40 μA
54AC138	I_{CC}	15 μA	350 μA	1000 μA	80 μA
54AC151	I_{CC}	15 μA	75 μA	500 μA	80 μA
54AC161	I_{CC}	15 μA	75 μA	1000 μA	40 μA
54AC240	I_{CC}	15 μA	100 μA	500 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	10 μA
54AC244	I_{CC}	15 μA	100 μA	500 μA	160 μA
	I_{OZ}	1 μA	10 μA	10 μA	10 μA
54AC245	I_{CC}	15 μA	100 μA	500 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	10 μA
54AC273	I_{CC}	75 μA	350 μA	2000 μA	160 μA
54AC373	I_{CC}	15 μA	75 μA	500 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	10 μA

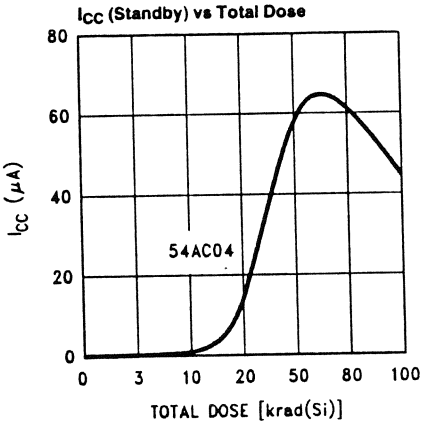
Notes:

- Data presented is for the FACT JAN-qualified process. Because the JAN process differs from the MIL-STD-883/SMD and commercial processes, non-JAN devices should not be presumed to exhibit similar performance.
- Testing per MIL-STD-883, Method 1019.4
- Anneal is performed for 168 hours at +100°C.

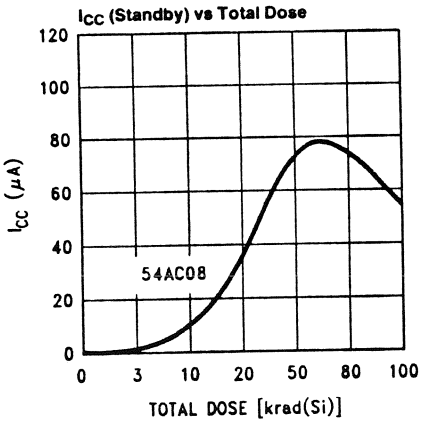
Typical Performance Characteristics



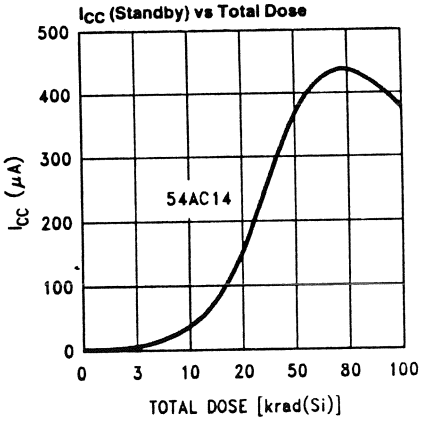
Radiation Input Bias = High



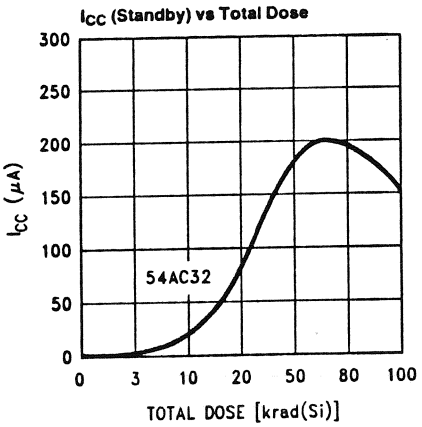
Radiation Input Bias = High



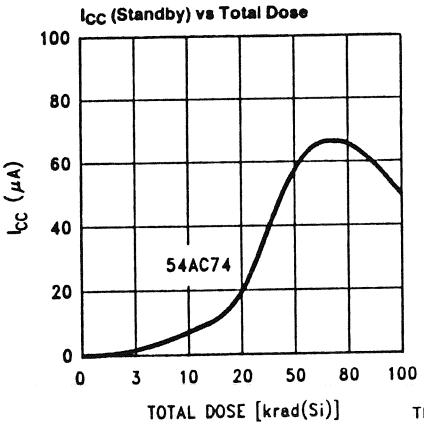
Radiation Input Bias = Low



Radiation Input Bias = Low



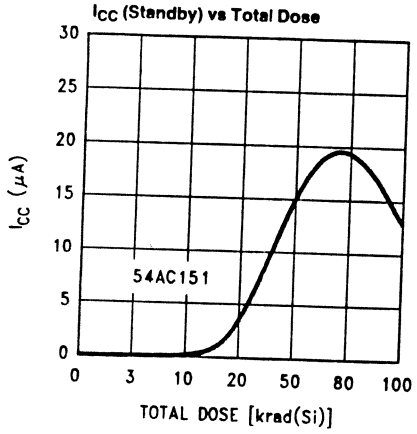
Radiation Input Bias = Low



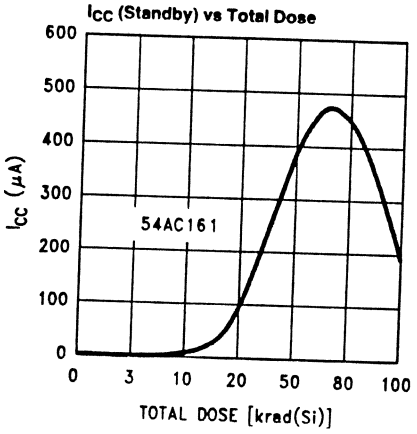
Radiation Input Bias = High

TL/F/11301-1

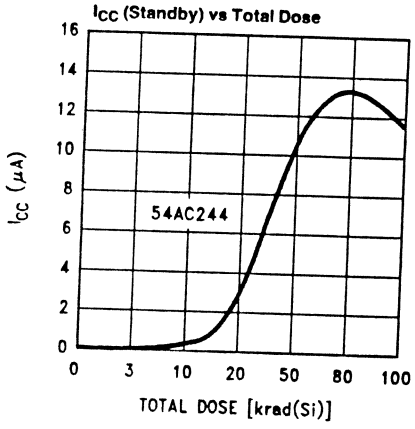
Typical Performance Characteristics (Continued)



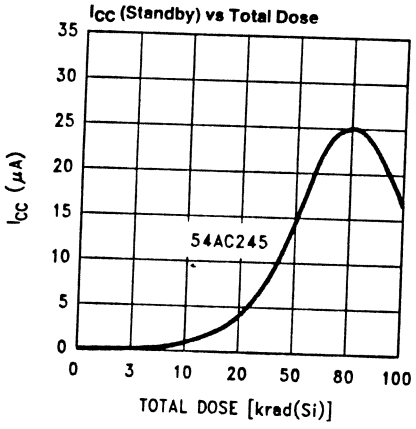
Radiation Input Bias = High



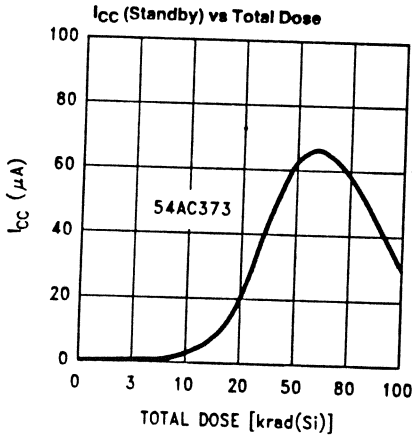
Radiation Input Bias = Low



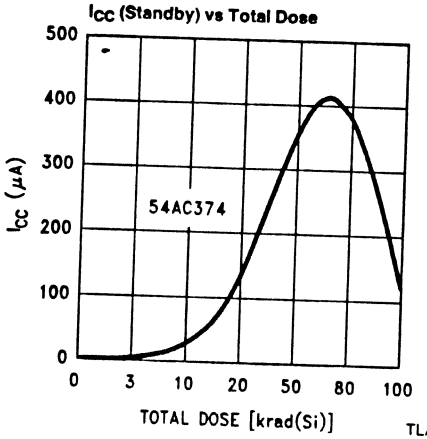
Radiation Input Bias = High



Radiation Input Bias = High



Radiation Input Bias = Low

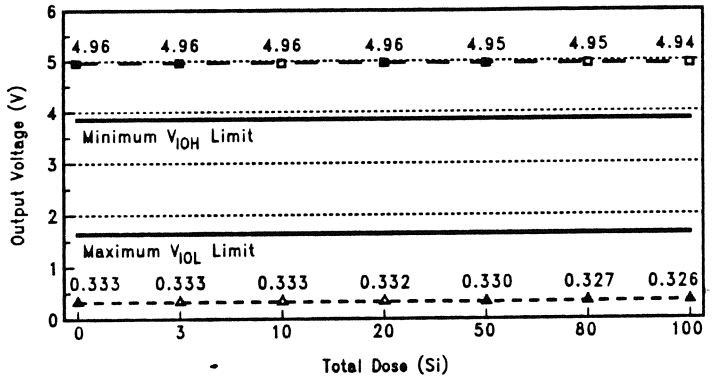


TL/F/11301–2

Radiation Input Bias = Low

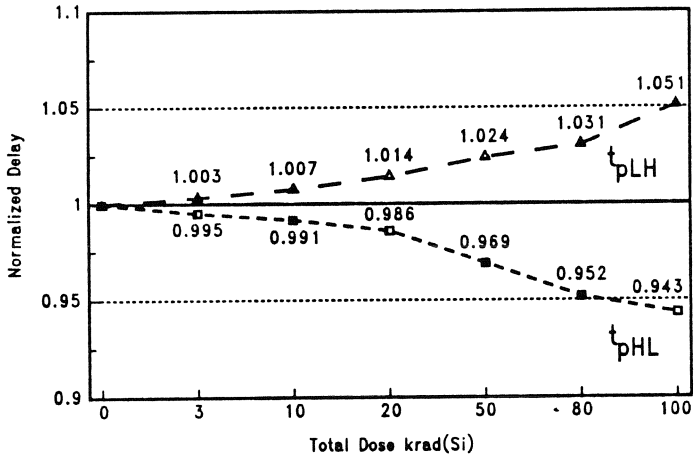
Typical Performance Characteristics (Continued)

54AC00 RH Performance
V_{IOH}/V_{IOL} at ±50 mA, V_{CC} = 5.5V, +25°C



TL/F/11301–30

54AC00 AC Performance



TL/F/11301–3

Radiation Tolerant Qualified FACT ACT Product

Exceptions: Parameters Which Do Not Stay Within Pre-Rad Values

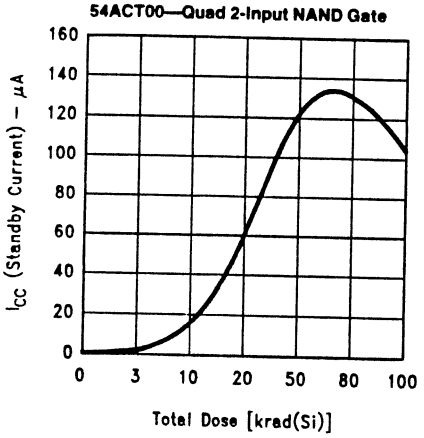
Device Type	Parameter	@ 3 krad(Si)	@ 10 krad(Si)	@ 100 krad(Si)	Post Anneal
54ACT00	I_{CC}	15 μA	75 μA	500 μA	40 μA
54ACT109	I_{CC}	15 μA	75 μA	500 μA	40 μA
54ACT138	I_{CC}	15 μA	200 μA	1000 μA	80 μA
54ACT151	I_{CC}	15 μA	100 μA	500 μA	80 μA
54ACT153	I_{CC}	15 μA	350 μA	700 μA	80 μA
54ACT175	I_{CC}	15 μA	75 μA	500 μA	80 μA
54ACT244	I_{CC}	15 μA	100 μA	2000 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	
54ACT245	I_{CC}	15 μA	350 μA	2500 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	
54ACT373	I_{CC}	15 μA	100 μA	700 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	
54ACT521	I_{CC}	15 μA	75 μA	500 μA	160 μA
54ACT825	I_{CC}	15 μA	75 μA	500 μA	160 μA
	I_{OZ}	1 μA	3 μA	10 μA	

Notes:

- Data presented is for the FACT JAN-qualified process. Because the JAN process differs from the MIL-STD-883/SMD and commercial processes, non-JAN devices should not be presumed to exhibit similar performance.
- Testing per MIL-STD-883, Method 1019.4
- Anneal is performed for 168 hours at +100°C.

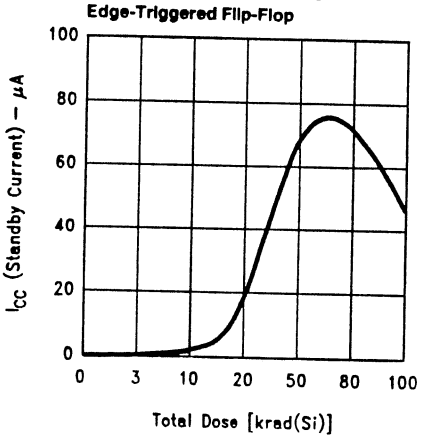
Typical Performance Characteristics (Continued)

I_{CC} vs Total Dose
54ACT00—Quad 2-Input NAND Gate



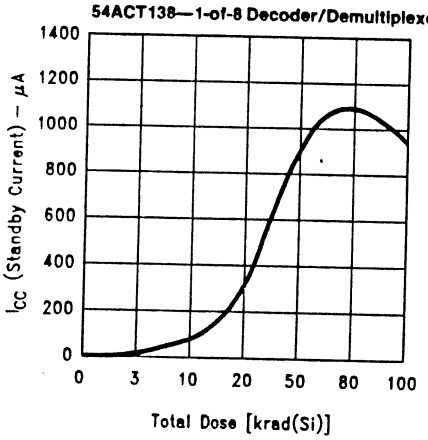
Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Radiation Input Bias = High

I_{CC} vs Total Dose
54ACT109—Dual JK Positive Edge-Triggered Flip-Flop



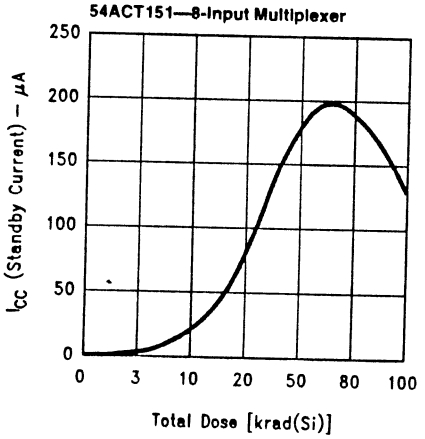
Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

I_{CC} vs Total Dose
54ACT138—1-of-8 Decoder/Demultiplexer



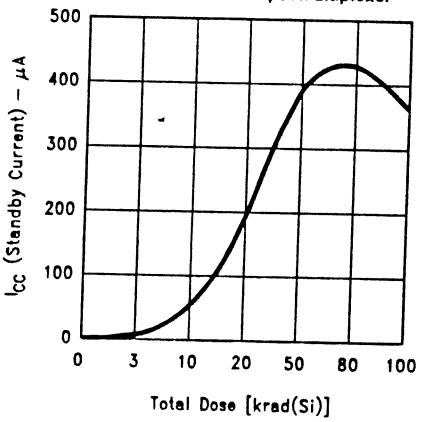
Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

I_{CC} vs Total Dose
54ACT151—8-Input Multiplexer



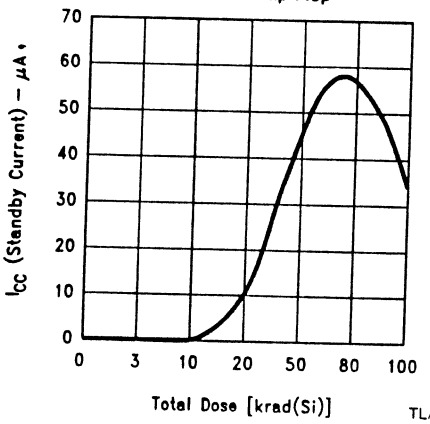
Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

I_{CC} vs Total Dose
54ACT153—Dual 4-Input Multiplexer



Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

I_{CC} vs Total Dose
54ACT175—Quad D Flip-Flop

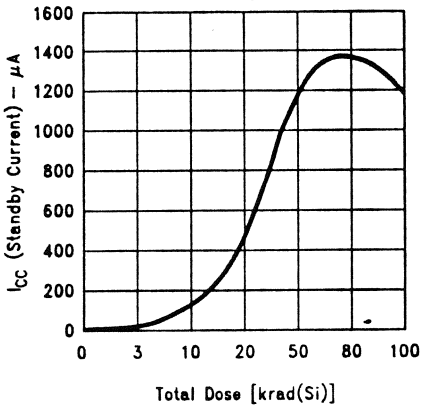


TL/F/11301–4

Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

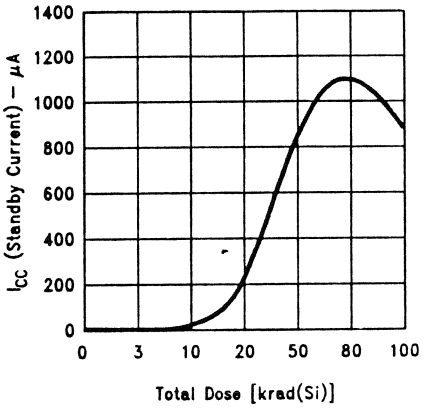
Typical Performance Characteristics (Continued)

I_{CC} vs Total Dose
54ACT244—Octal Buffer/Line Driver with TRI-STATE Outputs



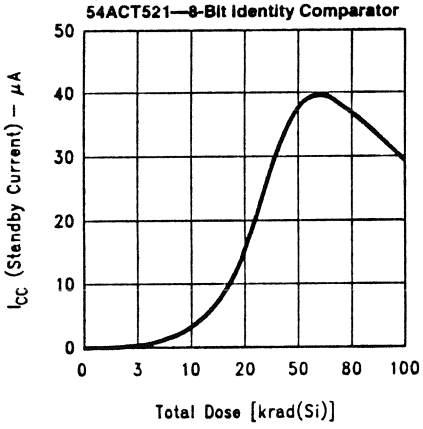
Dose Rate - 124 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

I_{CC} vs Total Dose
54ACT245—Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs



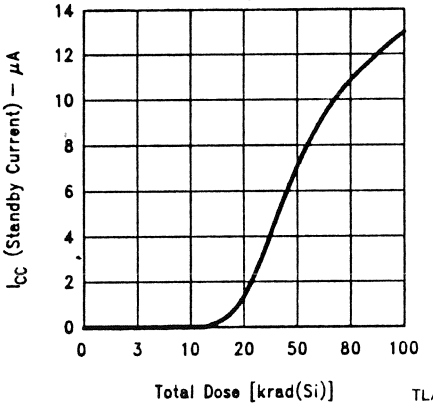
Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

I_{CC} vs Total Dose
54ACT521—8-Bit Identity Comparator



Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = Low

I_C vs Total Dose
54ACT825—8-Bit D Flip-Flop with TRI-STATE Outputs



TL/F/11301-5

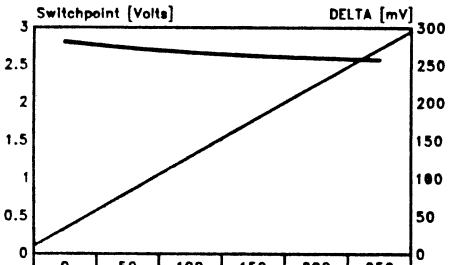
Dose Rate - 123 rad(Si)/sec, Temp: +25°C,
Input Radiation Bias = High

TOTAL DOSE DEGRADATION OF THE DEVICE'S SWITCHPOINT

An important design parameter for circuit designers is the switchpoint of a function. In the past, this parameter was not measured directly by an IC manufacturer but was verified indirectly by measuring other parameters. The figure below shows the switchpoint of a 54AC08 Quad 2-Input AND Gate degrading very slowly with increasing total dose accumulation. The change in switchpoint value is less than 250 mV and does not exceed switchpoint limits as established by using V_{OL} and V_{OH} measurements to validate these limits (1.85 V_{dc} and 3.65 V_{dc}).

One variable that affects the circuit's switchpoint is the threshold voltage value of each "p" and "n" MOSFET. The figure below depicts the typical threshold voltage total dose radiation response for these CMOS transistors. It shows that the n-channel transistor degrades more slowly than the p-channel transistor. This degradation affects the edge rates of the function's output waveform. Because many different size transistors are used in the function's design, the switchpoint's degraded value represents the sum effect of the MOSFET's threshold voltage changes and other circuit parasitic effects as caused by the total dose environment. Therefore, when designing a radiation-hardened system, the switchpoint is more important than the individual MOSFET's total dose radiation response.

Switchpoint Degradation 54AC08



	0	50	100	150	200	250
Switchpoint	2.8	2.71	2.66	2.61	2.58	2.56
SIGMA (+)	2.81	2.72	2.66	2.61	2.59	2.57
SIGMA (−)	2.8	2.7	2.65	2.6	2.57	2.55
DELTA [mV]	0	92	150	200	224	247

Total Dose [krad(Si)]

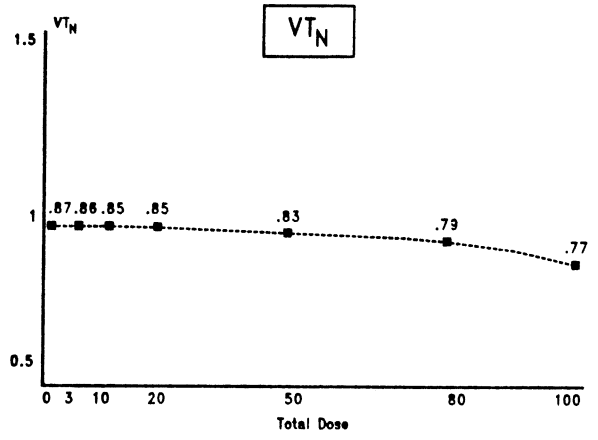
Inputs = High, Dose Rate = 129 rad(Si)/sec. TL/F/11301–6

To control the process relative to radiation-induced defects, it is more important to understand individual transistor radiation responses at the IC fabrication level than at the system or circuit design level. As a MOSFET accumulates total dose, its threshold voltage changes due to the trapped charge generated in its gate oxide. The p-channel MOSFET is driven more toward the enhancement mode as total dose accumulation is increased. This generally results from trapped holes (positrons) in the gate oxide causing a more negative voltage level to turn ON the p-channel device. In the case of an n-channel CMOS transistor, as the total dose level is increased, the positive trap charge dominates at the lower values of accumulated total dose and the device is driven toward the depletion mode of operation. However, at a high total dose level [300–450 krad(Si)], the threshold voltage begins to rebound and the device will start to become more "enhanced". This positive increase in the n-channel device threshold voltage results from the interface state generation dominating at the higher total dose level.

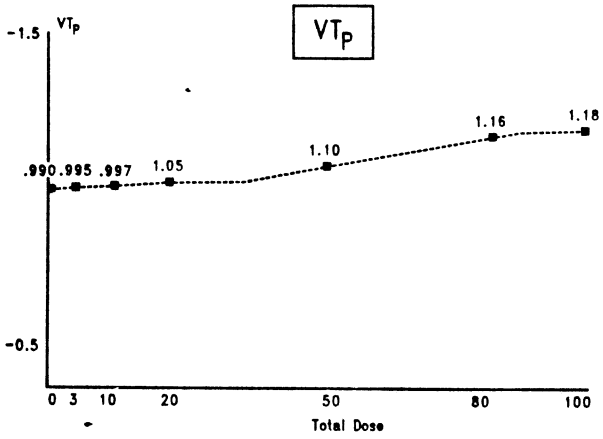
Trapped holes and interface states are competing effects. Trapped holes dominate at a high dose rate while interface states usually dominate at a low dose rate. Other conditions which affect the generation of trapped holes and interface states are temperature and bias conditions.

Radiation hard oxides are inefficient in generating trapped holes and interface states.

FACT Thresholds



TL/F/11301–23



TL/F/11301–7

TOTAL DOSE IRRADIATION AND ANNEALING

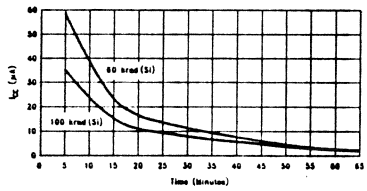
Two types of total dose annealing effects are currently important for radiation-hardened system designs:

- Self-Annealing
- Accelerated temperature anneal as required by MIL-STD-883, Method 1019.4

The total dose radiation-induced defects in the CMOS oxides and associated changes in electrical performance of CMOS devices are not stable and are difficult to evaluate as to their exact radiation responses. These post-irradiation effects are time and temperature dependent, as well as dose rate and bias sensitive.

The figures below show self anneal data curves which demonstrate the rapid recovery of FACT products. After receiving an accumulative total dose of 100 krad(Si), the irradiated parts were allowed to self anneal under bias at room temperature. Once withdrawn from the Cobalt-60 source, Group A electrical end-point tests were performed at five-minute intervals. Since I_{CC} (standby) current or I_{OZ} (TRI-STATE) current are the only parameters that degrade with total ionizing dose, curves were plotted for radiation-induced parasitic leakage current.

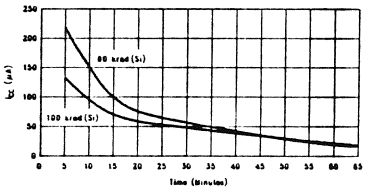
Post-Irradiation Anneal Data
54AC04—Quad 2-Input NOR Gate



TL/F/11301–24

Dose Rate = 128 rad(Si)/sec
Temperature = +25°C
Radiation Input Bias = High

Post-Irradiation Anneal Data
54AC374—Octal D Flip-Flop with TRI-STATE Outputs



TL/F/11301–25

Dose Rate = 128 rad(Si)/sec
Temperature = +25°C
Radiation Bias Inputs = High

After plotting data points at 5 minutes to 20 minutes as well as at 45 minutes to 55 minutes, a curve fit was used to plot the intermediate points between these two intervals. As the curves depict, the standby current reduces exponentially and establishes a minimum value at the 55-minute time point between 60% and 90% of its original initial post-irradiation value (5-minute time point).

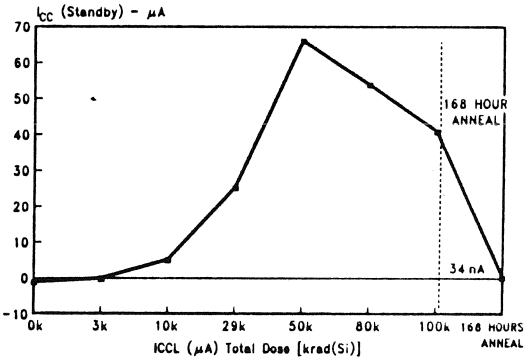
Early time interval values of I_{CC} are of interest for radiation-hardened system designs that are concerned with the high dose rate environments. I_{CC} values at the later time intervals (50 minute or 60 minute) are of major concern to the radiation-hardened system designs associated with space radiation environments.

To help address system designers' needs for a more viable simulation of the space total dose environment, MIL-STD-883 Method 1019 was recently modified. This Method provides a conservative approach in determining a function's total ionizing does radiation hardness in a space environment. The methodology essentially performs a high dose rate [50–300 rad(Si)/sec] irradiation to 1.5 times the specification limit then executing Group A tests at 1.0 and 1.5 times the specification limit. Assuming all devices pass the post-irradiation parametric and functional tests, devices are placed under worst case bias at a temperature of +100°C ±5°C for one week (168 ±12 hours). At the end of this one-week accelerated temperature anneal, these devices are again tested for post-irradiation parametric and functional failures. This new methodology (MIL-STD-883C, Method 1019.4) provides procedures for observing the prime detractors for CMOS products in a space radiation environment:

- Trapped oxide-charge-related failures
- Interface-state-related failures

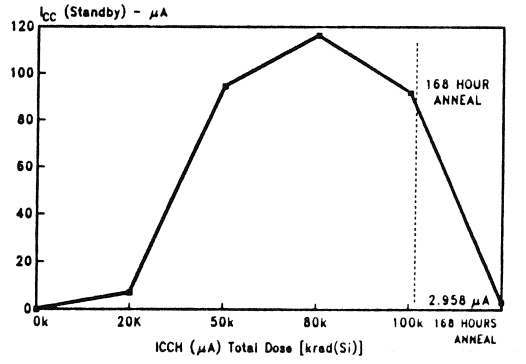
The figures below depict the FACT 54AC00's typical radiation response when using the new method, 1019.4. Note that the two parameters (I_{CC} and I_{OZ}) that degrade under high dose rate testing recover significantly as a result of the accelerated temperature anneal procedures of the new method. After the one-week anneal, the 54AC299 recovers and is able to pass pre-irradiation worst-case values (160 μA), typically less than 1 μA. At a 100 krad(Si) total dose level, an insufficient amount of interface states is generated after performing the new method. This is verified by observing the change in propagation times which does not change by more than 1 ns after a total dose of 100 krad(Si) and the accelerated temperature anneal method. Typical propagation values are 300 ps–500 ps.

54AC00 Radiation and Accelerated Anneal Evaluation



TL/F/11301–8

54AC299 Radiation Accelerated Anneal Evaluation



TL/F/11301–20

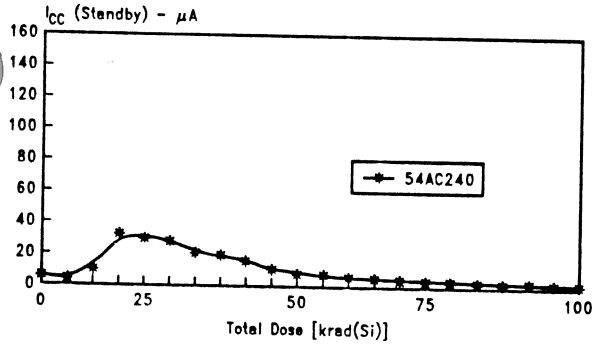
Inputs = High, No Bias, Room Temperature

LOW DOSE RATE IRRADIATION TESTING

Designing radiation-hardened space systems is difficult, especially when the radiation data is not representative of the environment. This is particularly true for the total ionizing dose that occurs in space. In space, the dose rate is very low [much less than 200 rad(Si)/hour] and the resulting radiation response is very different from that simulated by MIL-STD-883C, Method 1019 using the Colbolt-60 source. In general, the low dose rate condition dominates the space arena. However, there are certain situations in space where a system can experience a total dose level of 100 krad(Si) within one hour.

In a low dose rate condition, interface state generation manifests itself as the dominate mechanism for causing failure. The figure below shows a typical response of a FACT 54AC240 Octal Buffer/Line Driver in a low dose rate Cobalt-60 test. The dose rate was 0.055 rad(Si)/sec. It took 522 hours to complete 110 krad(Si) total dose level. When this test result was compared with the high dose rate test results, the magnitude of the I_{CC} standby leakage current was greatly reduced by a factor of 10 times. The current peak occurred at a much lower total dose level than at the high dose rate condition. The same response occurs for I_{OZ} (TRI-STATE leakage current) in a low dose rate environment. These are the only two parameters affected by total ionizing dose effects. Up to the 200 krad(Si) total dose level, FACT products are not severely affected by interface generation. Therefore, no other electrical parameter or circuit functionality is affected.

Low Dose Rate Testing
Dose Rate—200 rad(Si)/hr



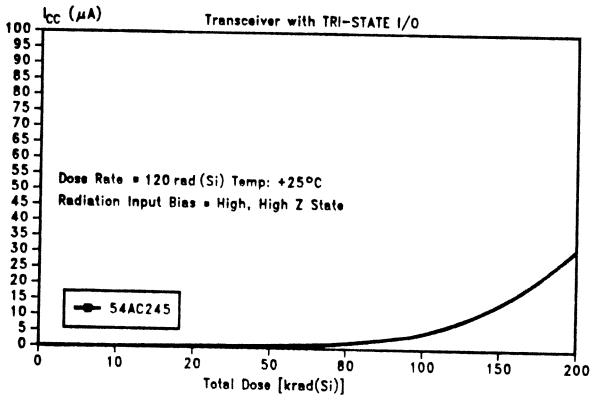
TL/F/11301–26

LOW-VOLTAGE TOTAL IONIZING DOSE RADIATION RESPONSE

With the arrival of VHSIC technology and its insertion into military and space systems, low-voltage power supplies are becoming very popular. Low-voltage power systems are those supplies with 3.0V to 3.3V DC range. Such reduction in voltage levels has an impact on the radiation response of a system or integrated circuit.

Total dose testing has been conducted on the FACT 54AC245 Bidirectional Transceiver with TRI-STATE Input/Output. This device was irradiated by a Cobalt-60 source with 3.3V DC bias conditions. The results showed a significant improvement in the reduction of I_{CC} (standby) leakage current as compared with a radiation response using 5.5V DC bias conditions. The figure below shows the standby leakage response to a total dose of 200 krad(Si) at a dose rate of 119 rad(Si)/sec using low biasing voltage of 3.3V DC.

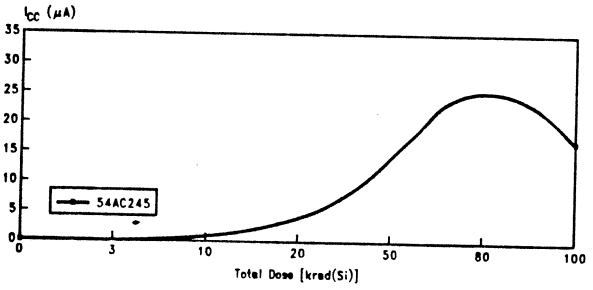
54AC245 V_{IN} = V_{CC} = 3.3 V_{DC}



TL/F/11301–9

The figure below shows the total ionizing dose response at a dose rate of 120 rad(Si)/sec using 5.5V DC bias conditions.

I_{CC} (Standby) vs Total Dose 54AC245—
Octal Bidirectional Transceiver with TRI-STATE I/O



TL/F/11301–21

Dose Rate = 119 rad(Si) Temp: +25°C
Radiation Input Bias = High
V_{IN} = 5.0 V_{DC}, V_{CC} = 5.5 V_{DC}

Employing a low voltage power system not only reduces the magnitude of the radiation-induced leakage current, but also minimizes the threshold voltage shifts and the total dose enhancement of the "hot electron" effect. Dose rate and SEP (Single Event Phenomena) latchup performance is also improved.

Care must be used when using a low-voltage power system in a radiation environment. While improvements are observed as previously mentioned, there are trade-offs to be considered, particularly concerning non-radiation performance. However, one issue of concern in the radiation environment is radiation-induced upset due to dose rate or SEP. As supply voltages are reduced, this function becomes more easily upsettable.

When there is full understanding of the total radiation environment as well as each system's particular design, low-voltage supply is a viable choice.

DOSE RATE TEST RESULTS

Analysis of the FACT 54AC299 8-Bit Universal Shift Register upset test data indicates that minimum upset threshold levels occurred under the worst-case conditions of a wide pulse (1 μs), lowest V_{CC} voltage (4.0V DC), and the device under test (DUT) in the dynamic operating mode.

Measured minimum upset levels were 1.90 to 2.22 $\times$ 10^9 rad(Si)/sec. Narrow pulse (50 ns) data demonstrated radiation upset levels from 4.40 to 5.66 $\times$ 10^9 rad(Si)/sec under dynamic operation.

The lowest threshold (for transient output as well as for internal upset) occurred with the outputs in the HIGH state and the radiation pulse occurring on the rising clock edge.

Power supply surge currents were associated with these radiation upset levels. Peak surge current values ranged between 300 mA and 1000 mA. The table on this page shows data for narrow pulse and wide pulse upset testing. While considerable effort was made to reduce and eliminate inductance, the final upset threshold levels may still be partially due to inductive effects, both internal and external to the 54AC299. Upset threshold levels in the high impedance (disabled) state of the DUT consist of:

- A state change in the internal storage elements
- Transient voltages at the I/O pins which could be falsely detected by interfacing circuitry as a change in logic state.

The magnitude and duration of the transient voltages on the I/O pins in the disabled state were dependent on the output loading on these pins. Transient response was always positive-going with its amplitude rising with the increasing dose rate. These test results demonstrate that the transient characterization of the disabled state is complex without specific loading conditions and/or upset criteria being defined.

Using more resistive loading than reactive loading on I/O pins reduced the disabled state recovery time. Disabled state testing also showed that the internal upset level was unaffected whether the output pin was active or disabled.

Upon completion of radiation upset testing, latchup and survivability tests were performed at +25°C, +80°C, +100°C, and +116°C for V_{CC} = 4.5V DC, 5.0V DC, and 5.5V DC. These results indicated no latchup occurred for either narrow pulse (50 ns) or wide pulse (1 ms) radiation. The radiation test level for narrow pulse was 10^{10} rad(Si)/sec at +25°C. Due to heating of the circuit, the highest radiation level was limited at +116°C to 7.5 $\times$ 10^9 rad(Si)/sec.

After completing latchup and survivability tests, verification of latchup windows was performed. Test results indicate no existence of latchup windows under worst-case conditions for narrow and wide pulse radiation.

Observations show that the peak surge current was linear with dose rate for both 50 ns and 1 μs pulse widths. The wide pulse surge current indicates both prompt and delayed components. The delayed component has a 1 μs fall time. Both the narrow and wide pulse widths for these latchup tests had surge current recovery times at the highest levels of 2 μs or less. The table on this page shows latchup test results.

Overall results of this comprehensive Dose Rate testing indicate that products built on the FACT process, such as the 54AC299, are latchup immune with an upset level greater than 10^9 rad(Si)/sec.

FACT products offer system and circuit designers a cost-effective solution for radiation hardness in both tactical and space environments.

54AC299 Dose Rate Upset Summary, Active Outputs

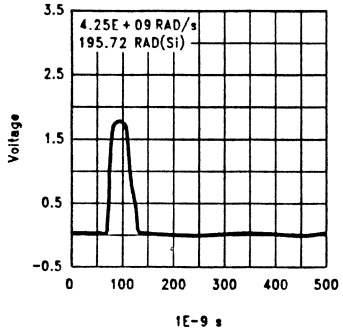
	Static Condition		Dynamic Condition	
V_{CC} S/N	4.0V	5.0V	4.0V	5.0V
	[E9] rad(Si)	[E9] rad(Si)	[E9] rad(Si)	[E9] rad(Si)
50 ns UPSET THRESHOLD				
11	6.11	8.44	5.66	—
12	6.54	8.50	4.65	—
13	6.29	7.99	4.74	—
14	6.39	8.02	5.34	—
15	5.69	8.26	4.65	—
16	5.42	8.11	4.85	—
17	6.35	8.13	4.87	—
18	6.11	8.10	4.79	—
19	5.99	7.84	4.40	—
20	6.29	7.68	4.94	—
Minimum:	5.42	7.68	4.40	—
Maximum:	6.54	8.50	5.66	—
Mean:	6.11	8.11	4.89	—
1 μs UPSET THRESHOLDS				
21	—	—	1.90	2.27
22	—	—	1.93	2.46
23	—	—	1.99	2.40
24	—	—	2.08	2.66
25	—	—	2.10	2.57
26	—	—	1.94	2.66
27	—	—	1.99	2.64
28	—	—	2.11	2.42
29	—	—	2.11	2.32
30	—	—	2.22	2.44
Minimum:	—	—	1.90	2.27
Maximum:	—	—	2.22	2.66
Mean:	—	—	2.04	2.48

Latchup Test Results
Static and Dynamic Condition

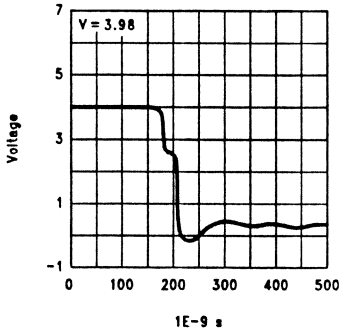
Radiation Pulse Width	Temperature			
	+25°C	+80°C	+100°C	+116°C
50 ns	No Latchup	No Latchup	No Latchup	No Latchup
1 μs	No Latchup	No Latchup	No Latchup	No Latchup

National 54AC299 Dose Rate Characterization
Upset Threshold Test at +25°C

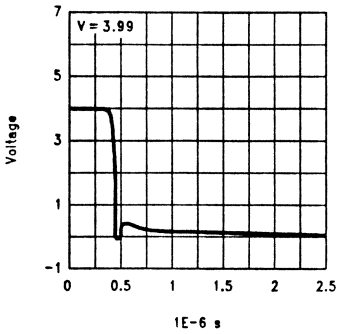
Dosimetry
File: 4608CL



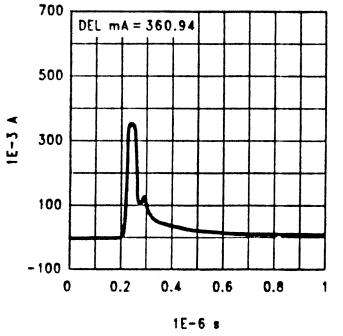
Q0



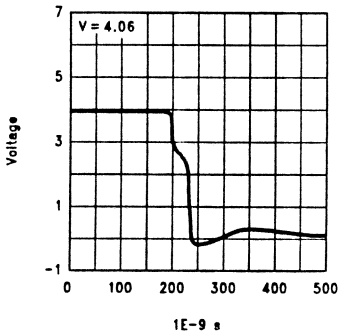
I/O 0



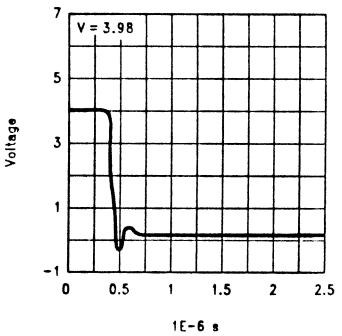
Delta I_{CC}



Q7

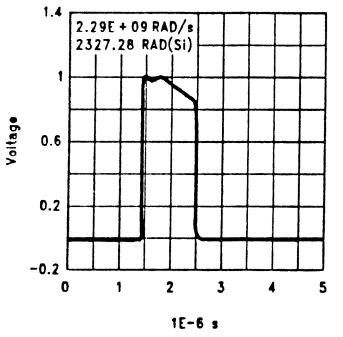


I/O 7

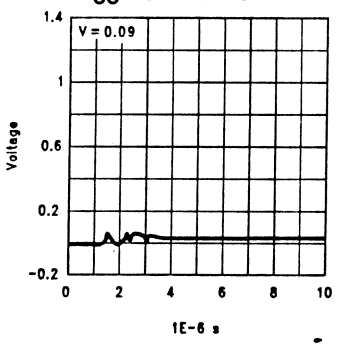


TL/F/11301–10

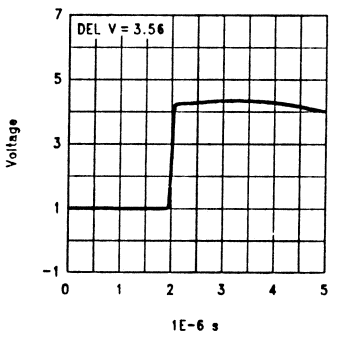
Dosimetry
File: 4608CL



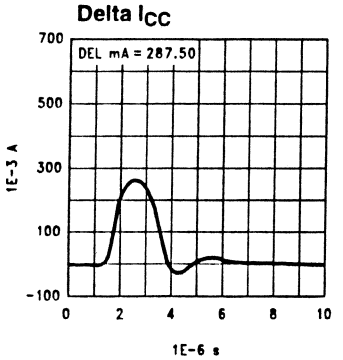
V_{CC} AC Inverted



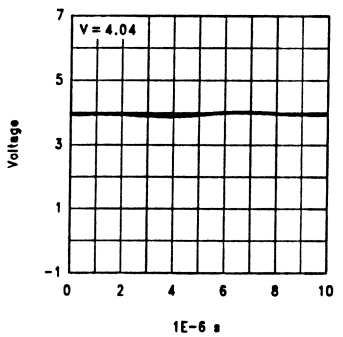
I/O o



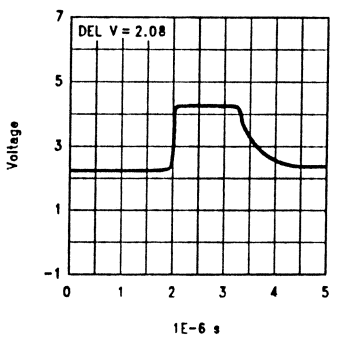
Delta I_{CC}



Q7



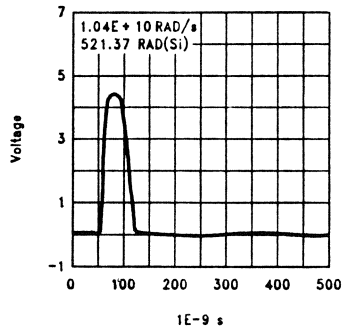
I/O 7



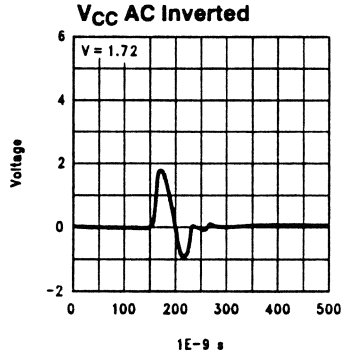
TL/F/11301–11

National 54AC299 Dose Rate Characterization
Reliability Study at +25°C

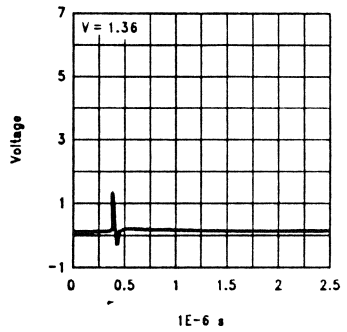
Dosimetry
File: 4608CL



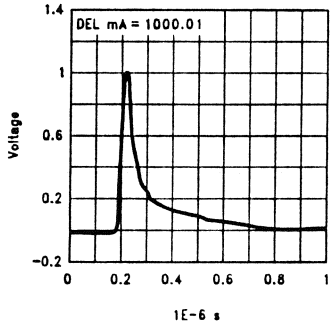
V_{CC} AC Inverted



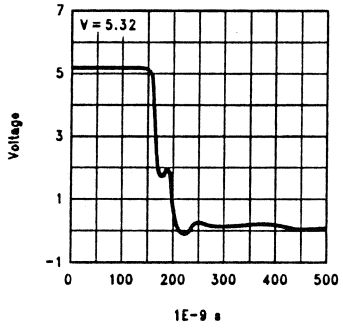
I/O 0



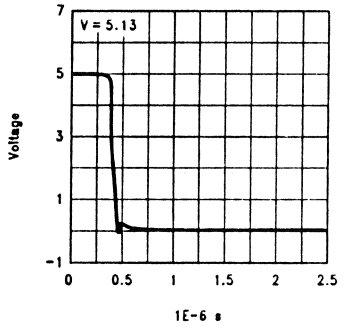
Delta I_{CC}



Q7



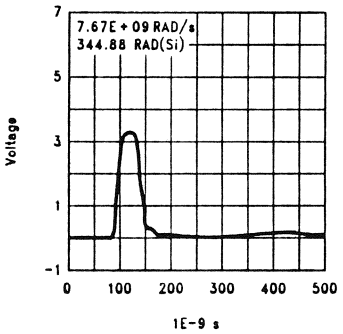
I/O 7



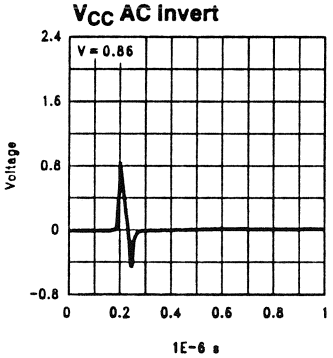
TL/F/11301–12

National 54AC299 Dose Rate Characterization
Latchup/Survivability Test at +117°C

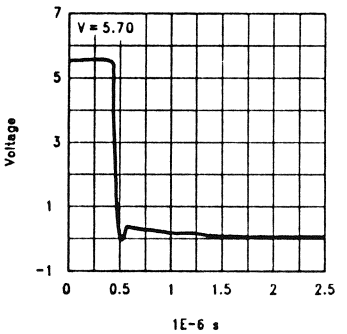
Dosimetry
File: 4608CL



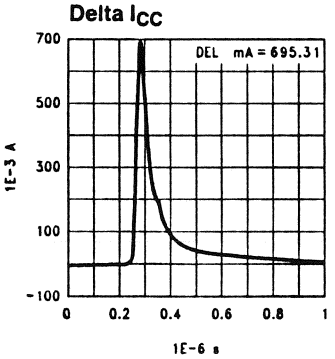
V_{CC} AC invert



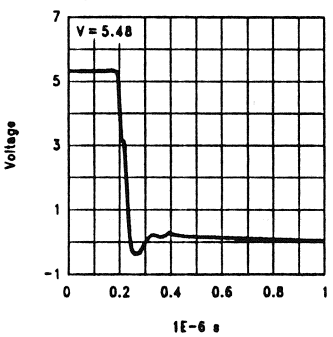
I/O 0



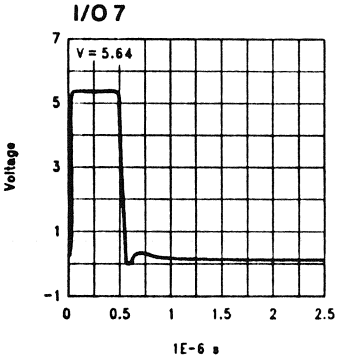
Delta I_{CC}



Q7



I/O 7



TL/F/11301–13

SINGLE EVENT PHENOMENA (SEP) TEST RESULTS

Space system designers require single event radiation test data. Independently performed single event radiation of FACT and other manufacturers' products was completed at the Lawrence Berkeley Laboratory's 88-inch cyclotron facility. Six types of heavy ion beams were employed to test the resilience of FACT (both AC and ACT versions) and other logic devices: xeon (603 MeV), krypton (308 MeV), copper (90 MeV), argon (180 MeV), neon (90 MeV), and nitrogen (67 MeV).

FACT test results were compared with similar functions in different technologies, such as AHC, HC, ALS, and LS. Tests demonstrated that FACT logic has higher resistance in the SEP cosmic ray environment than functionally equivalent devices in other process/design technologies.

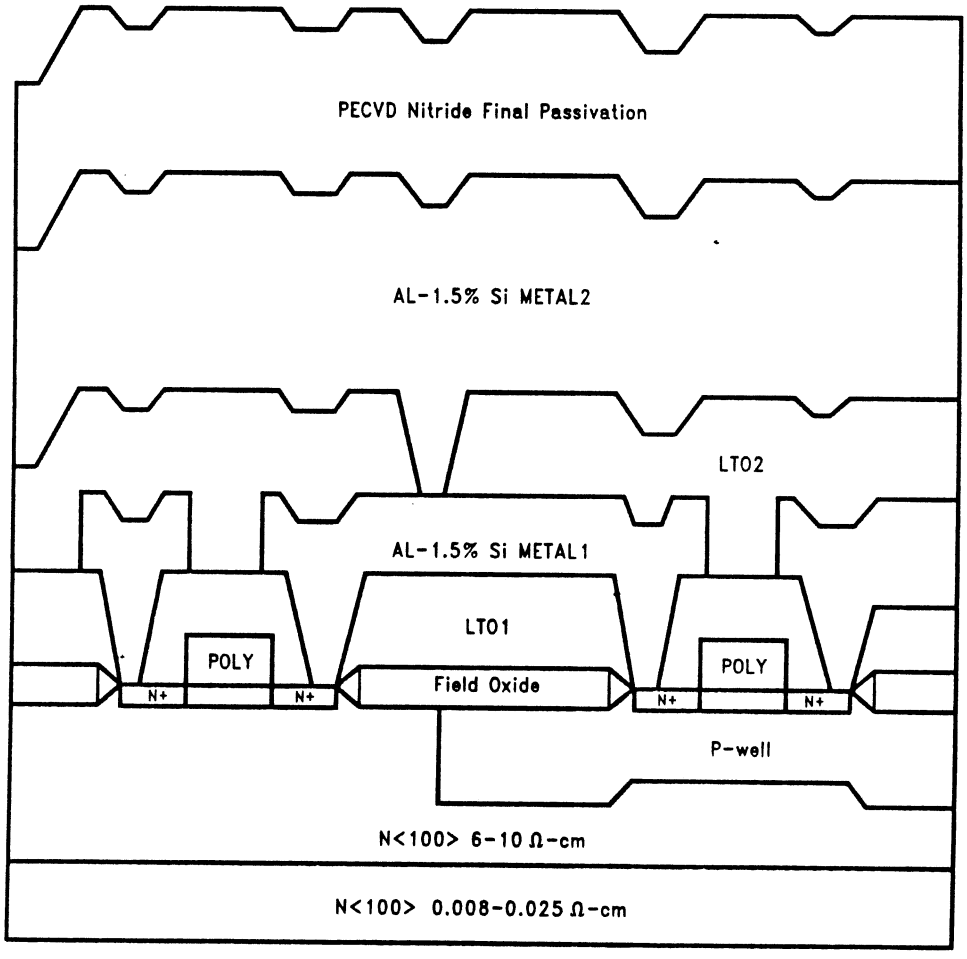
- FACT devices that were manufactured using National's JAN Class S Epi process (8 μm) did not latchup for LET (Linear Energy Transfer) values between 40 MeV to 120 MeV/((mg/cm2)^2). CMOS and other devices manufactured on thick Epi layers (greater than 10 μm) are suspect to latchup at these levels.
- Since no latchup was detected, an upper limit of the latchup cross-section was assigned at 10^{-9} cm^2/device for LET = 120 MeV/((mg/cm^2)^2). Latchup was detected in non-Epi processes.
- Testing demonstrated that FACT logic possesses large SEU LET threshold values in a range of 40–60 [MeV/mg/cm^2)].

Summary of SEU Susceptibilities for FACT Logic

Device	Data Code	LET Threshold [MeV/((mg/cm^2)^2)]	Saturation Cross-Section (cm^2/device)
54AC163	8909	40	2×10^{-5}
54AC174	8922	55	3×10^{-5}
54AC299	8922	48	3×10^{-5}
54AC374	8840	50	2×10^{-6}
54ACT174	8920	60	9×10^{-5}
54ACT373	8948	40	2×10^{-4}

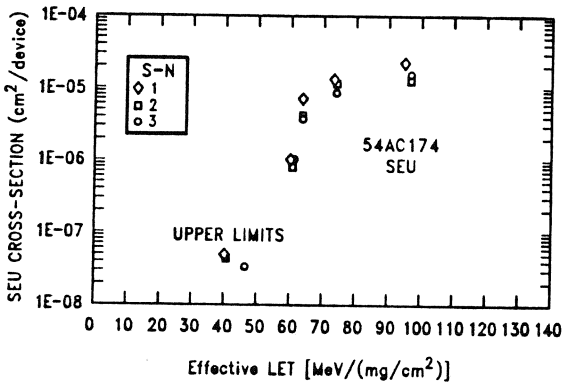
FACT logic's high SEU LET threshold is much higher than most space-orbital flights will encounter. This means a reduction or elimination of circumvention circuits or EDAC methods for those systems that employ FACT product. This provides system designers with a solution that is cost effective and increases the level of SEP resistance.

FACT Inverter Cross Section



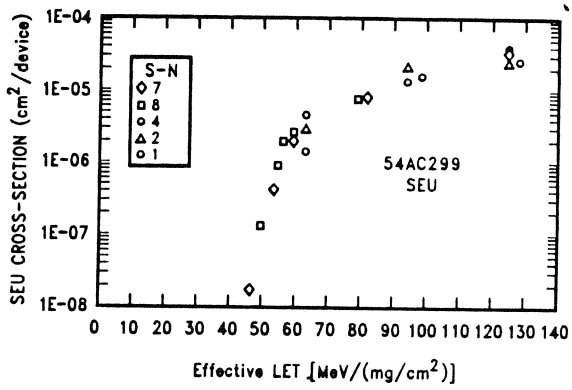
TL/F/11301–14

SEU Test Results for 54AC174



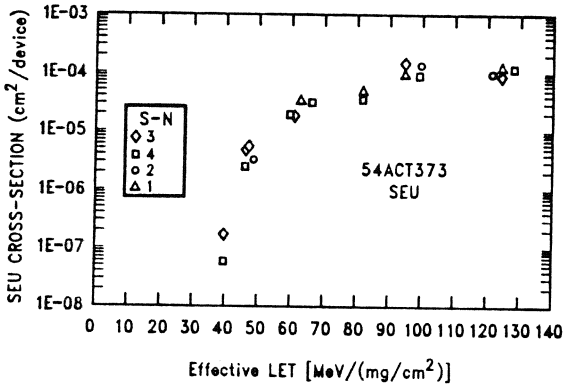
TL/F/11301-15

SEU Test Results for 54AC299



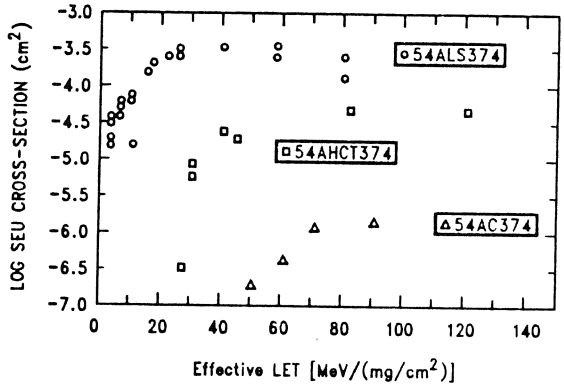
TL/F/11301-27

SEU Test Results for 54ACT373



TL/F/11301-28

SEU Test Results for 54AC374, 54AHCT374, and 54ALS374



TL/F/11301-29

FACT Quiet Series Logic

Offering the lowest in high-frequency emissions for high-speed technologies, this family should be considered in any space system.

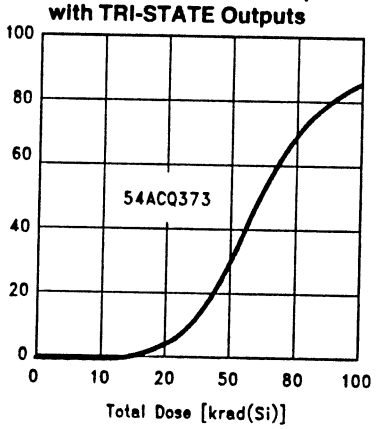
- Ideal ACMOS solution for noise-sensitive applications and asynchronous octal sockets. FACT Quiet Series (QS) reduces EMI, ground bounce, undershoot, and other noise issues as well as increases dynamic threshold. This same circuitry is also incorporated in FACT FCT products.
- FACT QS circuitry retains standard pinout.
- 15% greater speed than standard FACT logic, without increased power consumption.
- Design improvements greatly enhance performance and reliability, including output pin-to-pin propagation delay skew, higher electrostatic discharge (ESD) immunity, and higher latchup immunity. For clock distribution or for skew to similar output edges, the output skew is typically less than 500 ps; worst case, 1 ns. For bus applications or for skew to any output edge, skew is less than 800 ps. For clock drivers where duty cycle is important, $t_{PLH}-t_{PHL}$ is within ±500 ps.
- MIL Class 3 (4,000V and greater) ESD immunity is guaranteed on most functions. Typical ESD immunity is 6,000V.
- Propagation delays as well as setup and hold times are specified identically to or faster than standard FACT.
- Epitaxial silicon essentially eliminates latchup possibility. FACT QS latchup immunity is tested to 300 mA on the inputs and up to 1A on the outputs. Latchup immunity is specified at 300 mA minimum at +125°C.

National will be submitting its FACT Quiet Series devices for qualification to RHA (Radiation Hardness Assurance) standards. At that time, FACT QS ACQ and ACTQ devices will bear a "D" designation, signifying RHA certification to 10 krad(Si).

Typical Performance Characteristics

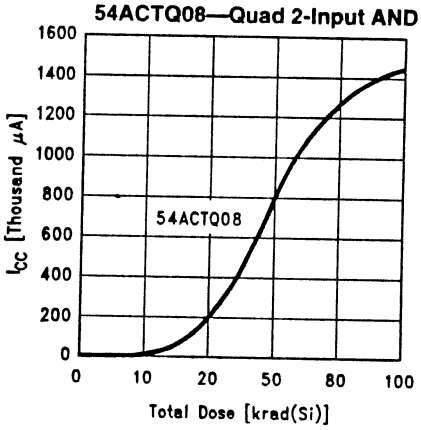
I_{CC} (Standby) vs Total Dose

54ACQ373—Octal Transparent Latch with TRI-STATE Outputs



Dose Rate = 128 rad(Si)/sec, Temp: +25°C
Radiation Input Bias = High

54ACTQ08—Quad 2-Input AND Gate



TL/F/11301–16

Dose Rate = 133 rad(Si)/sec, Temp: +25°C
Radiation Input Bias = High

FACT FCT Logic

Dual-marked as MIL-STD-883C and SMD, FACT FCT logic devices help military and aerospace designers get the most out of their high-performance systems. For high-speed VME bus applications at low CMOS power consumption levels, this is the family of choice.

- Enhanced noise immunity for improved undershoot (typically less than 0.5V) and ringing characteristics—lower than competitive FCT products. By reducing voltage swing for less device-generated noise, this minimized undershoot also protects the inputs of RAMs, PLDs, and interface devices.
- The split ground bus isolates input ground from output ground for improved dynamic threshold.
- Guaranteed current latchup immunity of 100 mA at +125°C; typical, 1A.
- Guaranteed MIL Class 2 (2,000V to 3,999V) ESD tolerance. Typical FACT FCT ESD tolerance is 6,000V.
- Fabricated using the same process technology as the FACT family.
- Pin-compatible replacement for competitive FCT devices. SCDs may include processing to Level S and radiation-resistant specifications.

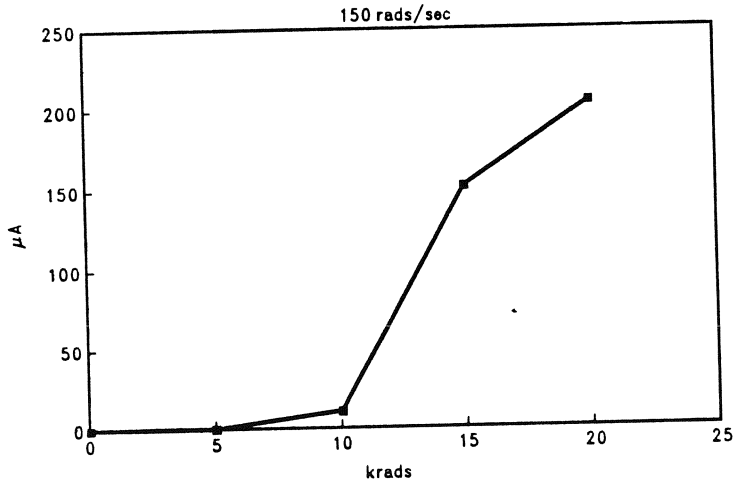
National will be submitting its FACT FCT devices for qualification to RHA (Radiation Hardness Assurance) standards. At that time, FACT FCT devices will bear a "D" designation as part of the SMD (Standard Military Drawing) number, signifying RHA certification to 10 krad(Si).

FACT FCT Dose Rate Response

Dose Rates rad(Si)/sec	'FCT244	'FCT245
1.1E8 3.1E8 4.7E8 1.1E9 5.6E9	No Latchup or Burn Out	
'FCT244 Upset at 1.1E9 rad(Si)/sec 'FCT245 Upset at 4.7E8 rad(Si)/sec		

Data courtesy of Raytheon Corporation.

54FCT273 Total Dose Data



TL/F/11301–17

F100K 300 Series ECL Logic

- The lowest power, easiest-to-use ECL logic to be fully compliant to MIL-STD-883C and available as an SMD
- Specified parametric testing across the entire military temperature range
- AC and DC performance specified over the entire −4.2V to −5.7V voltage range for easy interface with 100K ECL I/O devices and upgrades for systems employing 10K and 10KH logic
- ESD protection is guaranteed at MIL Class 2 (2,000V to 3,999V); typical immunity is 4000V
- Devices typically consume 30% to 50% less power per gate than functionally equivalent F100K 100 Series devices
- Full voltage and temperature compensation is guaranteed

Performing clock speeds of up to 400 MHz, the F100K 300 Series' 750 ps (typical) switching speeds allow mil/aero designers to eliminate speed bottlenecks in systems such as satellite communications, digital signal processing, radar, avionics, navigation, telecommunications, and portable instrumentation. All F100K 300 Series devices are plug-in compatible replacements for existing 100 Series sockets and easily interface with all ECL I/O devices (ASICs, PAL®s, and SRAMs).

The FAST-LSI process is used for our F100K 300 Series products. Similar to the FAST-Z process used with National's F100K 100 Series, it has many advantages that helped achieve the lower power consumption, higher ESD tolerance, and wider voltage range of the 300 Series. These improved ECL features make F100K 300 Series ECL devices attractive candidates for space projects.

PRODUCT TESTING

National's F100K 300 Series ECL has undergone preliminary investigation to determine its minimum radiation hardness level. Total dose irradiation tests have been performed on the:

- F100355 Low Power Quad Multiplexer/Latch. The F100355 contains four transparent latches, each of which can accept and store data from two sources. This device was chosen to represent the pure F100K 300 Series ECL circuitry, i.e., ECL input to ECL output.
- F100325 Low Power Hex ECL-to-TTL Translator. This device was chosen to represent mixed ECL/TTL circuitry, in this case converting ECL F100K logic levels to TTL logic levels.

Preliminary radiation test results for both devices show neither functional failures nor parametric (AC and DC) failures up to the 1 Mrad(Si) level. All parametric results are within National's published Table 1 limits with minimal deltas.

All total dose testing on these representative F100K 300 Series products was performed using step-stressing methodology at National's South Portland REL using the AECL Gammacell 220 (Cobalt-60 source). Post-irradiation parametric limit testing was done within five minutes from removal from the Gammacell 220. MIL-STD-883C, Method 1019.4 was employed.

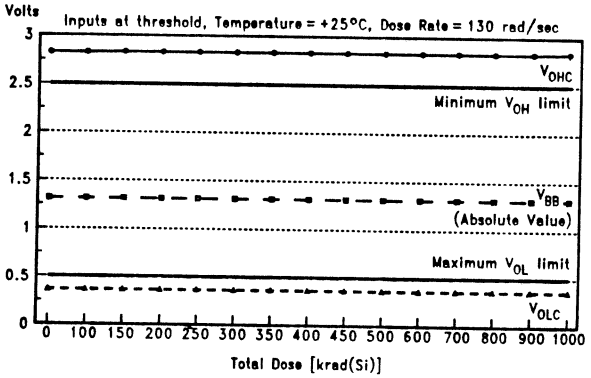
Since ECL is such high current, there is no "leakage" parameter which can be used to monitor radiation response (i.e., CMOS uses I_{CC}). Therefore, we must consider the input threshold (or internal reference voltage) to be the most sensitive parameter to observe for radiation effects.

The graphs below represent plots of V_{OLC} and V_{OHC} versus total dose radiation exposure. V_{OLC} and V_{OHC} are the "corner point" output level tests, performed using threshold value inputs such as V_{IH} (minimum) and V_{IL} (maximum). For both devices, there is essentially no shift in the output levels from the radiation exposure.

Note: The 100325 is unique as it has positive TTL-level outputs as well as an external ECL-level V_{BB} (the reference voltage) output. To plot V_{BB}, the absolute value was used.

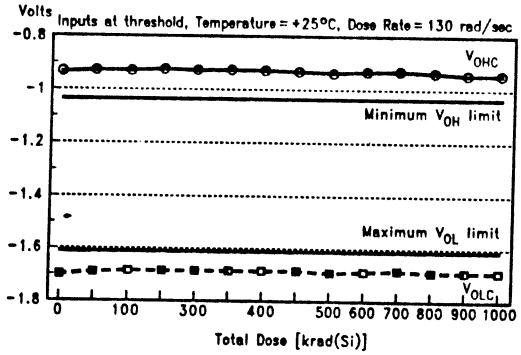
Please note that these results are preliminary and based on limited testing of two device functions. We strongly recommend that total dose radiation-hardened-assured F1003xx ECL product be purchased only on a wafer-by-wafer basis.

100325 Radiation Response



TL/F/11301–18

100355 Radiation Response



TL/F/11301–19

CMOS Custom Products

National's Mil/Areo Logic group offers CMOS custom products that are based on FACT process technology. The hardness level of this technology is product specific and typically retains parametric integrity up to 100 krad(Si).

If your custom logic requirements exhibit any combination of these characteristics, please contact your local National sales representative. We'll give you a timely response regarding our capabilities.

- Gate count (±5,000 gates)
- Pin count (up to 56 pins)
- Radiation tolerant (≥ 100 krad)
- JTAG circuitry (IEEE 1149.1)
- High drive (up to 64 mA)
- Tighter-than-usual timing requirements
- High temperatures (+200°C)
- TTL I/O or CMOS I/O

National Semiconductor

Linear Radiation Testing

As each new generation of Military/Aerospace systems evolve, manufacturers of Linear product must meet the challenge of new radiation requirements. Over the years, National Semiconductor has provided circuit and system designers with the needed radiation-resistant Linear integrated circuits for their designs.

National's Linear product meets the requirements for JAN S as well as Lockheed Monitor Line. Radiation testing is performed in full accordance with MIL-STD-883D, Method 1017 (Neutron) and Method 1019 (Total Ionizing Dose).

RADIATION TEST METHODOLOGY

- A wafer is selected from a wafer lot.
- Die are selected from the wafer and packaged according to DESC requirements.
- Following the Radiation Sample Flow, the samples are tested in accordance with Group A electrical parameter tests.
- The radiation samples are then irradiated to the specified radiation levels.
- After radiation, the irradiated parts are tested per Group A Post Irradiation Parametric Limits to establish to RHA capability.

POST-IRRADIATION ANNEAL

Should a post-irradiation anneal be required, National Semiconductor will perform the anneal in accordance with the customer's specification. An example is shown in the LM108 Radiation Test Data Section.

TOTAL DOSE TEST RESULTS—LM108A

LM108—GENERAL DESCRIPTION

The LM108 series are precision operational amplifiers. Specifications are a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range.

These functions operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

LM108 series features include:

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

LM108A RADIATION TEST RESULTS

Total dose testing of the LM108 Operation Amplifier yields the radiation responses discussed below. Anneal responses are also provided.

The Input Offset Voltage (*Figure 1*) depicts minimal amount degradation up to 100 krad(Si) level. After a 240-hour anneal, the Input Offset Voltage recovered almost to its initial value.

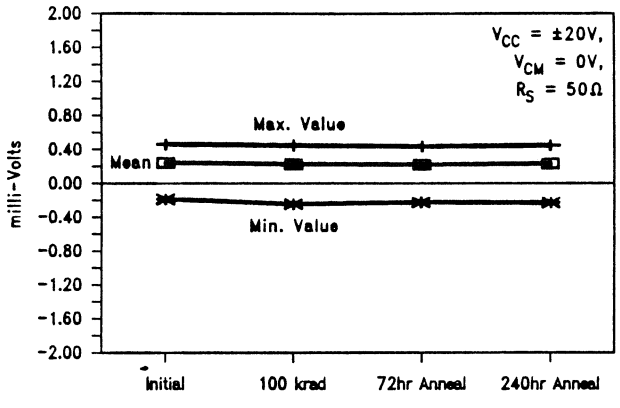
The radiation response of the Input Offset Current (*Figure 2*) shows this current to increase minimally at 100 krad(Si).

The Input Bias Current (*Figures 3* and *4*) indicates the radiation response for this parameter to be 100 krad(Si). These figures also show this parameter *recovers minimally* with a 240-hour anneal under bias and at room temperature.

Open-Loop Voltage Gain radiation response is depicted in *Figures 5* and *6*. This parameter degrades with *minimal recovery* after 240-hour anneal at room temperature and under bias.

The Power Supply Current and Common Mode Rejection Ratio (CMRR) radiation responses are shown in *Figures 7* and *8*, respectively. Both radiation responses indicate minimum degradation and full recovery after a 240-hour anneal at room temperature bias.

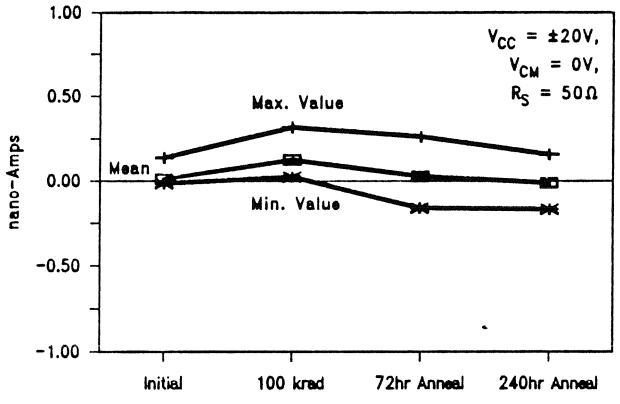
Input Offset Voltage (V_{IO})



TL/H/11385-1

FIGURE 1

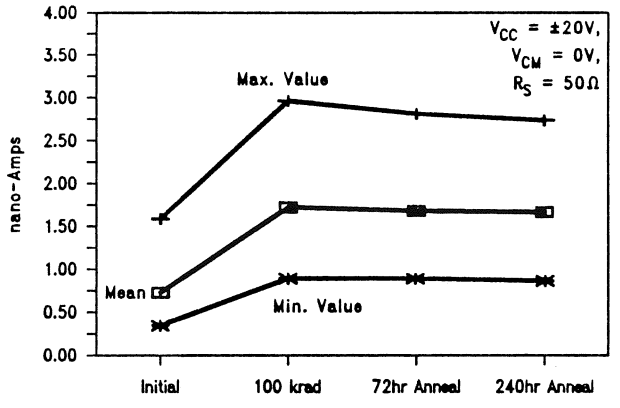
Input Offset Current (I_{IO})



TL/H/11385-2

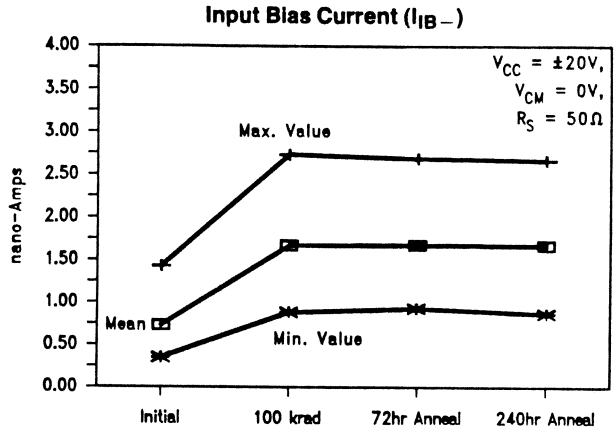
FIGURE 2

Input Bias Current (I_{IB+})



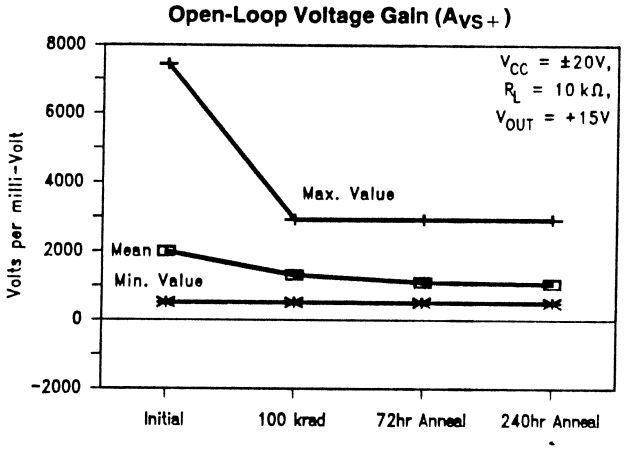
TL/H/11385-3

FIGURE 3



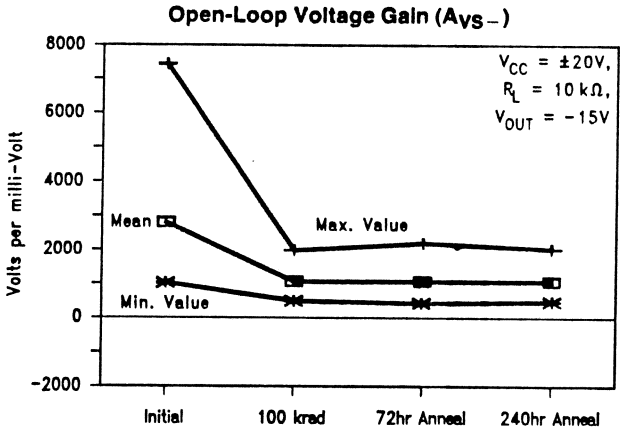
TL/H/11385–4

FIGURE 4



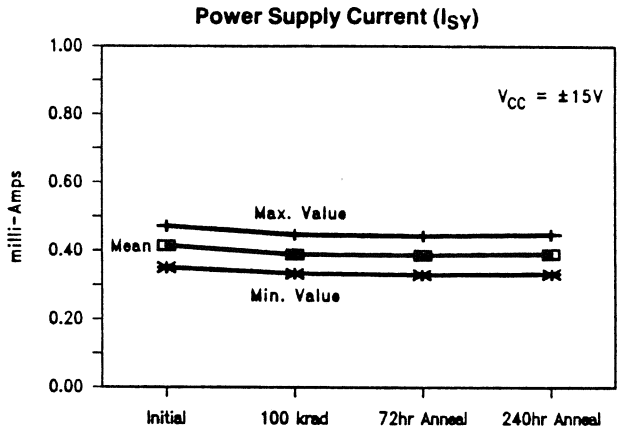
TL/H/11385–5

FIGURE 5



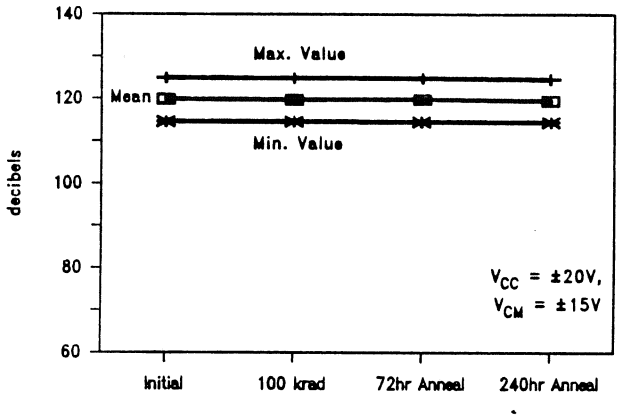
TL/H/11385–6

FIGURE 6



TL/H/11385-7

FIGURE 7



TL/H/11385-8

FIGURE 8

National Semiconductor

National Military/Aerospace Processing Capabilities

JAN CLASS S

QPL products processed to MIL-M-38510 Level S for space-level applications. The JAN S process flow assures long-term device reliability through a series of 100% screening tests over and above those specified for JAN Class B devices.

MIL S

Non-JAN products processed to Level S to negotiated electrical specifications for space level applications.

SCD (SOURCE CONTROL DRAWING)—LEVEL S

SCDs can be used to specify radiation testing to a Level S process flow. SCDs can also be used to define tighter radiation-assurance specifications than are available via the RHA's broader categories.

JAN CLASS B

QPL products processed to MIL-M-38510 Level B for military applications. JAN Class B devices are preferred, where available, for most aircraft, naval, and ground applications.

SCD (SOURCE CONTROL DRAWING)—LEVEL B

SCDs can also be used to specify radiation testing to a Level B process flow. Tighter radiation-assurance specifications than are available via the RHA's broader categories may be defined in an SCD.

SMD (STANDARD MILITARY DRAWING)

SMD products are processed to Level B with Table 1 electricals controlled by DESC.

MIL-STD-883C

This is the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Electrical test parameters, test conditions, test limits, and test temperatures for each NSC MIL-STD-883 compliant device are listed in Table 1 or RETS documents, controlled by National Semiconductor's Quality Assurance Department.

-MIL

The -MIL suffix refers to products produced on a flow similar to, but not fully compliant with, MIL-STD-883. Specific reasons for non-compliancy are clearly defined in the Certificate of Conformance shipped with the product.

DM

The DM suffix designates Logic products packaged in a ceramic DIP and tested over the −55°C to +125°C temperature range. DM devices are processed according to the standard commercial process flow.

JAN Class S (MIL-M-38510) Process Flow

Process Step	Method	Condition	Requirement
Wafer Lot Acceptance	5007		All lots
Non-Destructive Bond Pull	2023		100%
Internal Visual	2010	A	100%
Stabilization Bake	1008	C	100%
Temperature Cycling	1010	C	100%
Constant Acceleration	2001	E	100%
Mark		JAN format	100%
Serialization			100%
Radiographic	2012		100%
Pre-Burn-In Electricals	5004	Slash Sheet	100%
PIND Testing	2020	A	100%
Burn-In	1015	D, 240 Hrs./ + 125°C Min.	100%
PDA		3% Func. or 5% DC Max.	100%
Final Electricals	**Method**	**Condition**	**Requirement**
DC + 25°C*	5004	Slash Sheet	100%
DC + 125°C*	5004	Slash Sheet	100%
Solder Lead Finish			
DC − 55°C*	5004	Slash Sheet	100%
AC + 25°C	5004	Slash Sheet	100%
AC + 125°C (if required)	5004	Slash Sheet	100%
AC − 55°C (if required)	5004	Slash Sheet	100%
Group A	**Method**	**Condition**	**Requirement**
DC + 25°C*	5005	Slash Sheet	100%
DC + 125°C*	5005	Slash Sheet	100%
DC − 55°C*	5005	Slash Sheet	100%
AC + 25°C	5005	Slash Sheet	100%
AC + 125°C	5005	Slash Sheet	100%
AC − 55°C	5005	Slash Sheet	100%
Fine Leak	1014	B	100%
Gross Leak	1014	C	100%
External Visual	2009		100%
Groups B and D	5005	JAN Data	Sampled
Group E	5005	JAN Data	Sampled

*includes Functional Testing

JAN Class B (MIL-M-38510) Process Flow

Process Step	Method	Condition	Requirement
Internal Visual	2010	B	100%
Stabilization Bake	1008	C	100%
Temperature Cycling	1010	C	100%
Constant Acceleration	2001	E	100%
Solder Lead Finish			100%
Fine Leak	1014	B	100%
Gross Leak	1014	C	100%
Mark		JAN format	
Pre-Burn-In Electricals	5004	Slash Sheet	100%
Burn-In	1015	D, +125°C Min.	100%
PDA		DC, +25°C, 5% Max.	
Final Electricals	**Method**	**Condition**	**Requirement**
DC +25°C*	5004	Slash Sheet	100%
DC +125°C*	5004	Slash Sheet	100%
Solder Lead Finish			100%
Fine Leak	1014	B	100%
Gross Leak	1014	C	100%
DC −55°C*	5004	Slash Sheet	100%
AC +25°C	5004	Slash Sheet	100%
Group A	**Method**	**Condition**	**Requirement**
DC +25°C*	5005	Slash Sheet	2% LTPD
DC +125°C*	5005	Slash Sheet	3% LTPD
DC −55°C*	5005	Slash Sheet	5% LTPD
AC +25°C	5005	Slash Sheet	2% LTPD
AC +125°C (if required)	5005	Slash Sheet	3% LTPD
AC −55°C (if required)	5005	Slash Sheet	5% LTPD
Fine Leak	1014	B	5% LTPD
Gross Leak	1014	C	5% LTPD
External Visual	2009	B	100%
Groups B, C, D, E	5005	JAN Data	Sampled

*includes Functional Testing

MIL-STD-883 Process Flow

Process Step	Method	Condition	Requirement
Internal Visual	2010	B	100%
Stabilization Bake	1008	C	100%
Temperature Cycling	1010	C	100%
Constant Acceleration	2001	E	100%
Solder			100%
Fine Leak	1014	B	100%
Gross Leak	1014	C	100%
Mark		QB format	
Interim Electricals	5004	National Table 1	100%
Burn-In	1015	C, +125°C Min.	100%
PDA		DC, +25°C, 5% Max.	
Final Electricals	**Method**	**Condition**	**Requirement**
DC +25°C*	5004	National Table 1	100%
DC +125°C*	5004	National Table 1	100%
Solder			100%
Fine Leak	1014	B	100%
Gross Leak	1014	C	100%
DC −55°C*	5004	National Table 1	100%
AC +25°C*	5004	National Table 1	100%
Group A	**Method**	**Condition**	**Requirement**
DC +25°C*	5005	National Table 1	2% LTPD
DC +125°C*	5005	National Table 1	3% LTPD
DC −55°C*	5005	National Table 1	5% LTPD
AC +25°C	5005	National Table 1	2% LTPD
AC +125°C (if required)	5005	National Table 1	3% LTPD
AC −55°C (if required)	5005	National Table 1	5% LTPD
Fine Leak	1014	B	5% LTPD
Gross Leak	1014	C	5% LTPD
External Visual	2009		100%
Groups B, C, D	5005	Generic Data	Sampled

*includes Functional Testing

National Semiconductor

Glossary of Terms

Attribute Testing: Quantitative testing indicating the total number of devices subjected to various screening steps in a test sequence, as well as the total number of devices passing or failing these steps; also known as lot testing.

Dose Rate (Transient Radiation): The amount of ionizing radiation to which an object would receive per unit of time.

- **High Dose Rate:**

  Example: greater than $\frac{10 \text{ rad(Si)}}{\text{sec}}$

- **Low Dose Rate:**

  Example: greater than $\frac{0.055 \text{ rad(Si)}}{\text{sec}}$

EMI: Any electrical phenomenon where electric and magnetic field energies combine to create noise or interference on electrical signals, i.e., electromagnetic interference.

ESD: The amount of voltage a device can withstand without sustaining damage, i.e., electrostatic discharge.

F100K 300 Series ECL: Having F100K ECL speed and performance, National's F100K 300 Series consumes up to 50% less operating power, guarantees MIL Class 2 (2,000V–3,999V) ESD protection, tests output skew specification, and has a stable I/O over a wide range of voltages and temperature.

FACT: FACT (Fairchild Advanced CMOS Technology). Manufactured on a thin Epi-CMOS process. Offers high performance at zero standby power.

- **54ACxxxx:** CMOS inputs and outputs; offers post-irradiation parametric limits to 100 krad(Si).
- **54ACTxxxx:** TTL inputs and CMOS outputs; offers post-irradiation parametric limits to 100 krad(Si).

FACT FCT: Extension of FACT logic for high-performance systems. Features include enhanced noise immunity, improved dynamic threshold, dynamic output drive capable of driving 75Ω transmission lines, latchup immunity, and MIL Class 2 ESD tolerance (2,000V–3,999V).

- **54FCTxxxx:** TTL inputs and CMOS outputs; offers post-irradiation parametric limits to 30 krad(Si).

FACT Quiet Series (QS): Extension of FACT logic for noise-sensitive applications. Features include reduced ground bounce, improved dynamic threshold, elimination of undershoot, very tight output skew, elimination of latchup, and guaranteed MIL Class 2 ESD tolerance (2,000V–3,999V).

- **54ACQxxxx:** CMOS inputs and outputs; offers post-irradiation parametric limits to 30 krad(Si).
- **54ACTQxxxx:** TTL inputs and CMOS outputs; offers post-irradiation parametric limits to 30 krad(Si).

Functional Failure: The point at which the device is no longer capable of operating.

GTO™: Graduated turn-on output; the proprietary circuitry added to FACT QS and FACT FCT products that controls edge rates, i.e., waveshaping.

Latchup: A condition where the output of a circuit has become fixed near one of the two voltage extremes and will no longer react to changes in the input signal. Latchup may be radiation induced, but can also result from voltage overstresses and other causes.

Military Process Flow

- **JAN Class S:** QPL (Qualified Products List) products processed to MIL-M-38510 Level S for space level applications.
- **MIL S:** Non-QPL products processed to Level S to negotiated electrical specifications for space level applications.
- **JAN Class B:** QPL products processed to MIL-M-38510 Level B for military applications.
- **SMD (Standard Military Drawing):** SMDs are processed to Level B with Table 1 electricals controlled by DESC (Defense Electronics Supply Center).
- **MIL-STD-883C:** The general specification for non-JAN military product. Revision C defines the minimum requirements for a device to be marked as 883-compliant. Electrical test parameters, test conditions, test limits and test temperatures for each NSC MIL-STD-883 compliant device are listed in Table 1 documents, controlled by NSC's Quality Assurance Department.
- **DM:** The DM suffix designates National's Logic products that are packaged in a ceramic DIP and tested over the −55°C to +125°C temperature range. DM devices are processed according to the standard commercial flow. Also available are FM (flatpak) and LM (LCC) products.
- **-MIL:** This suffix refers to products produced on a flow similar to, but not fully compliant with, MIL-STD-883. Specific reasons for non-compliancy are defined in the Certificate of Conformance shipped with the product.

Parametric Failure: The point at which the device goes out of defined specification limits.

Parametric Testing: This tests individual variables or parameters. Values are recorded and are traceable to individual devices. Parametric testing is the opposite of attribute or lot testing.

Rad: The basic unit of absorbed dose for ionized radiation. The rad represents the absorption of 100 ergs of energy per gram of targeted material specified. In the case of integrated circuits, the specified material is silicon (Si).

Radiation: Energetic emitted radiant energy in the form of rays or particles; the combined processes of emission, transmission, and absorption of radiant energy.

RHA (Radiation Hardness Assurance) Categories

- **M** = Guaranteed limits up to 3 krad(Si)
- **D** = Guaranteed limits up to 10 krad(Si)
- **R** = Guaranteed limits up to 100 krad(Si)
- **H** = Guaranteed limits up to 1 Mrad(Si)

Single Event Phenomena (SEP): The effects caused by the passage of an alpha particle, proton, or cosmic ray (heavy ion). These effects include upset, latchup, funnel effect, and ion shunting.

Single Event Upset (SEU): A "soft error", a change of logic state, a bit flip, usually temporary. SEU is caused by alpha particles or cosmic rays as they pass through a device.

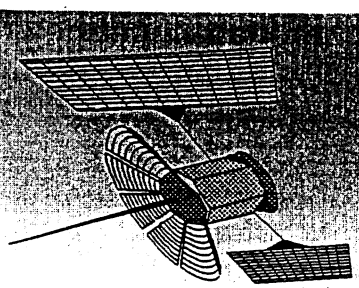
Skew: The difference in propagation delay as measured on similar outputs of one device.

Source Control Drawing (SCD): SCDs can be used to specify radiation testing to either a Level S or a Level B process flow. SCDs are also used to define tighter radiation-assurance specifications than are available via the RHA's broader categories.

Total Dose: The total accumulated amount of absorbed ionizing radiation specified at a particular dose rate exposure at +25°C.

USC™: Undershoot corrector; the proprietary circuitry added to FACT QS and FACT FCT to control signal excursion below ground.

Variable Testing: See Parametric Testing.



SPACE PRODUCTS OPERATION

September 1993

To our valued reader,

Harris Semiconductor's Space Products Operation would like to take this opportunity to reaffirm our allegiance to you and the space marketplace. As the first six editions of SPACE PRODUCTS NEWS have highlighted, we are focused upon total quality in every aspect of our business. We have addressed and continue to monitor several key areas in which we felt we could provide increased customer satisfaction, including on-time delivery, customer specification (SCD) reviews, delivery leadtimes, and new products to meet your system needs. We have listened to and acted upon what you, our customers, want and expect from the #1 supplier. As a result, we have instituted enhancements on both the service and product fronts. Below are just a few examples of these enhancements as highlighted in our previous newsletters.

- On the product front, we are continually developing and bringing to market the product you tell us you want. The RS-422 interface circuits (HS-26C/T31 and HS-26C/T32), denser memory circuits (256K SRAM and 64K CMOS PROM), advanced logic devices (ACS/ACTS), and radiation hardened field programmable gate arrays (HS-XC3020 and HS-XC3090) are just a few examples.

- On the service front, we have provided new (or enhanced the service of existing) resources to meet your needs.

  Two fully stocking North American Distributors (Hamilton/Hall-Mark and ZEUS, an Arrow Company) provide North American customers with reduced purchase quantities, off-the-shelf availability of our standard product offering, and a sales and applications engineering support team.

  Internationally, we have provided enhanced service through Jepico, our authorized Japanese distributor. Jepico, dedicated to the high reliability distribution industry, services over 70 Japanese customers.

  We have assembled a first class, service-oriented program management team located in Palm Bay, FL, who works closely with the Harris sales force in their activities to assure you 100% customer satisfaction.

  A Customer Engineering organization dedicated to the Military and Aerospace Division (M&AD) has been chartered to provide quick, user-friendly, quality SCD reviews. This organization, comprised of experienced Spec Reviewers and Writers, utilizes the expertise of dedicated functional area Quality, Assembly, and Test Engineers to quickly and accurately translate your requirements into instructions to our factory.

The above are just a few examples of our targeted improvement areas. We will continue to strive for excellence – to enhance our service provided and increase your satisfaction level.

HARRIS SEMICONDUCTOR P.O.BOX 883 MELBOURNE, FL 32902-0883

Your inputs and continual feedback are very important to us. In the 5th edition of SPACE PRODUCTS NEWS (January-March 1993), we included a response card requesting your inputs on the effectiveness of our newsletter and your opinion of Harris Space Products as your supplier. We appreciate the time each respondent spent to reply to our inquiry. While we have individually responded to and addressed specific comments with each respondent, we would like to share the below summary of inputs received.

1) On average, 92% of each newsletter is read, which frankly, is a staggering number when compared to usual marketing research statistics. However, many inputs received requested that we include more technical information. We are pleased to acknowledge your request with the publication of the accompanying Special Edition SPACE PRODUCTS NEWSletter: Integrated Circuits for the Space Environment. This special edition provides technical overviews of the space radiation environment and its effects on integrated circuits. Future editions of SPACE PRODUCTS NEWS will also be focused upon more technically and application oriented topics.

2) 83% of those respondents who have requested literature via our newsletter bingo cards rated our response to be good or better. While 83% is good, we will continue to strive for 100% satisfaction! Literature is available from any Space Products Operation team member directly, from our local sales and authorized representative locations, and from our two authorized distributors (ZEUS, an Arrow Company and Hamilton/Hall-Mark).

3) 81% of respondents currently use Harris space products in their systems with almost 9 out of 10 considering Harris Space Products their Supplier of Choice. Thank you! But, we will not be satisfied until that number is 100% year in and year out. We offer the most comprehensive line of space-qualified, radiation hardened ICs to support the commercial, scientific, and military satellite industries. Our logic, memory, microprocessor and peripheral, signal processing, and ASIC devices can provide you with a cost-effective means to implement all of your systems solutions.

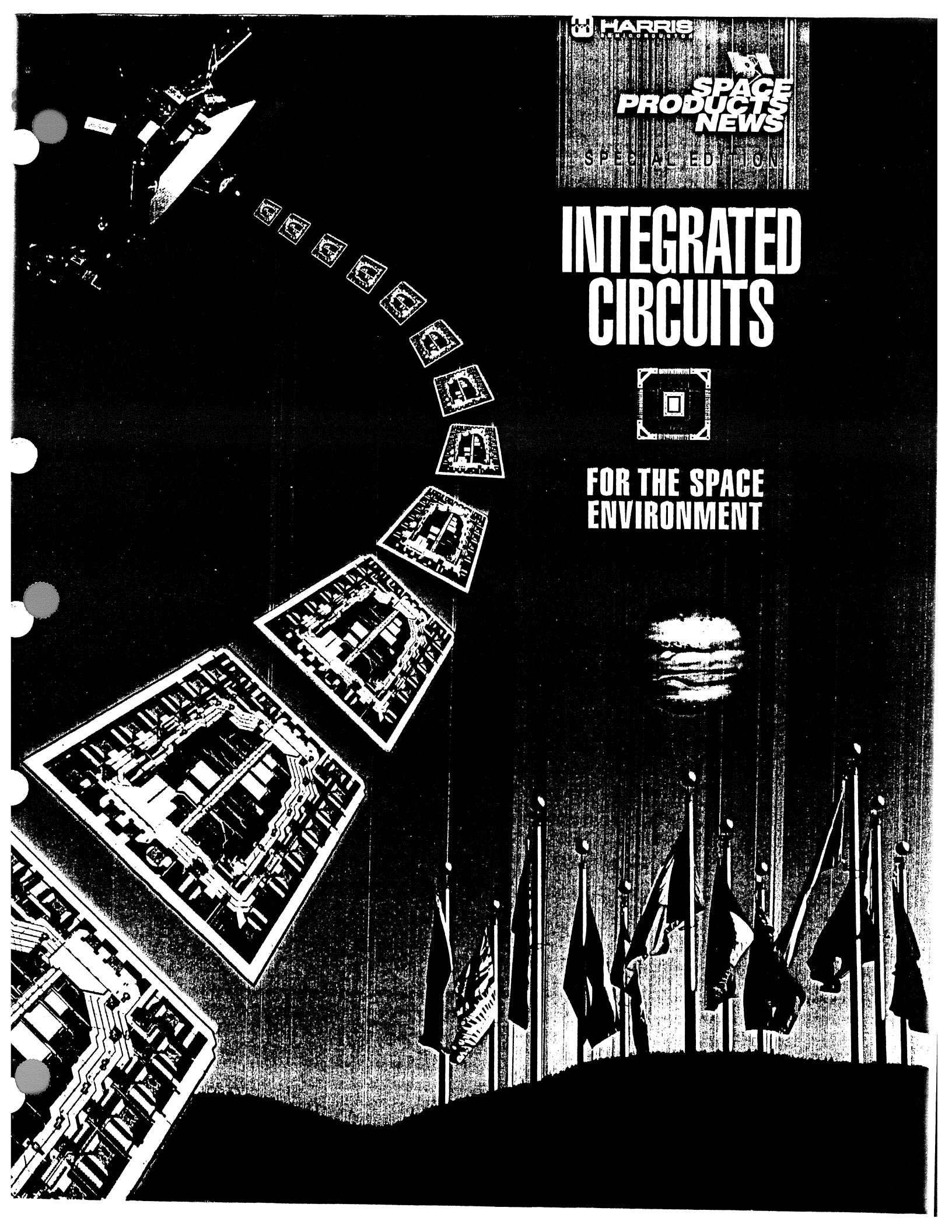
Please feel free to continue providing your inputs to us. You need not wait for us to publish another survey – we are happy to hear from you anytime! To accommodate you doing just that, we have published in the back cover of this special edition the phone numbers of each author and of each Editorial Board member of the newsletter. Feel free to use these phone numbers at your will.

We hope that you find this special edition informative and worth keeping for future reference. A future there will be, for we are in this market to stay. With over 30 years of rad hard experience behind us and the resources to guarantee our place in the future, we will continue to be here to fill all of your space system integrated circuit needs.

Regards,

Linda J. Whelan
SPACE PRODUCTS NEWS Editor

HARRIS SEMICONDUCTOR P.O.BOX 883 MELBOURNE, FL 32902-0883


HARRIS
SEMICONDUCTOR
SPACE
PRODUCTS
NEWS
SPECIAL EDITION
INTEGRATED
CIRCUITS
FOR THE SPACE
ENVIRONMENT

HARRIS SEMICONDUCTOR

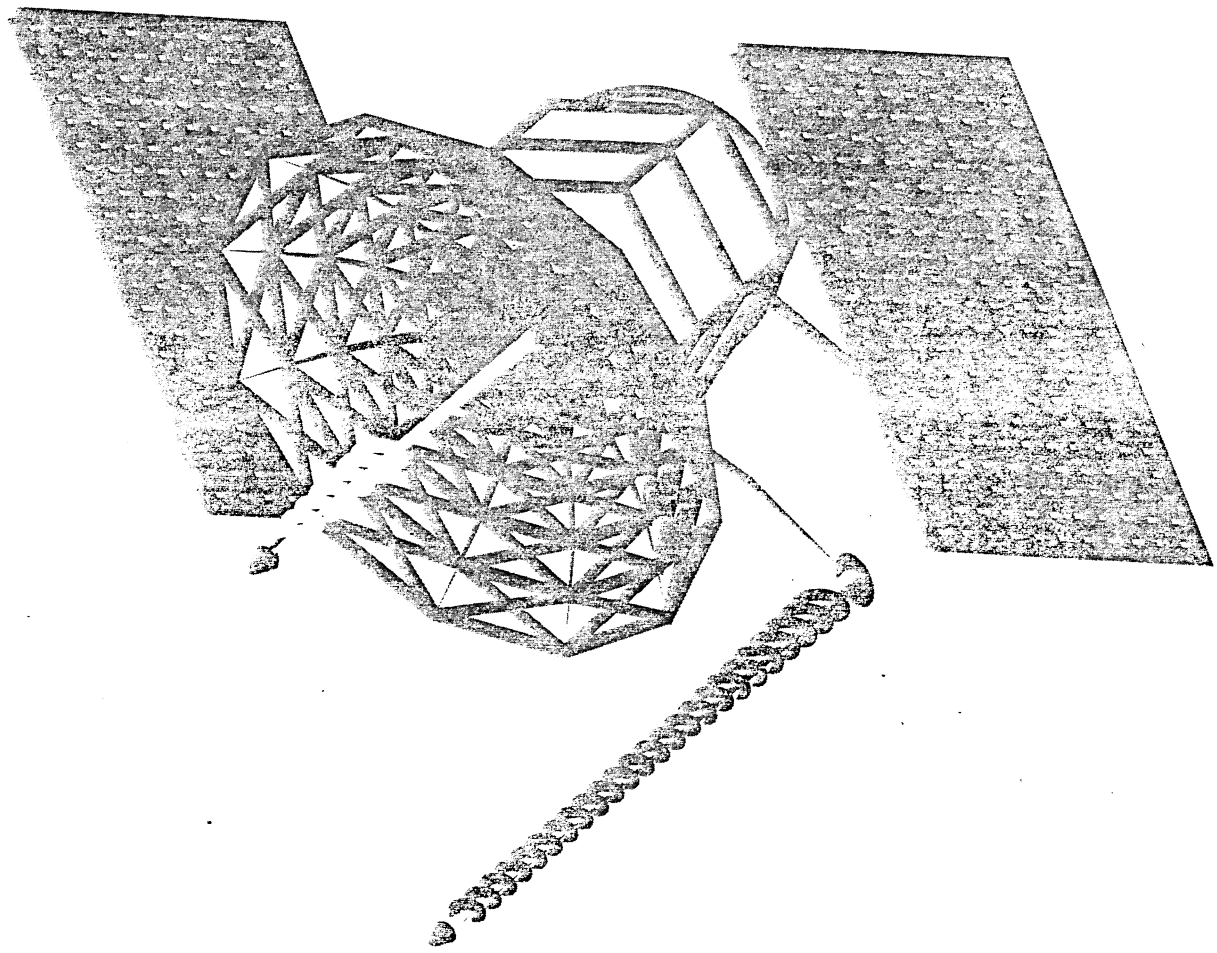
Harris Semiconductor has been an industry leader for more than two decades in radiation hardened circuits which provide high performance and high reliability in severe operating environments. The Harris radiation hardened product portfolio includes CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers and switches, data converters, the 80C85/80C86 microprocessor family, gate arrays, standard cells and custom devices which provide the system designer with a full complement of products for radiation hardened systems.

HARRIS SEMICONDUCTOR

SPECIAL EDITION
INTEGRATED CIRCUITS FOR
THE SPACE ENVIRONMENT

SPACE PRODUCTS NEWS

TABLE OF CONTENTS



Radiation in Space ... An Inescapable Threat

By Scott Moody

Radiation ... no matter the type of satellite, or orbit, or purpose, any craft launched into space must be designed considering the radiation environment it will be subjected to over its lifetime. With this in mind, Space Products Operation is pleased to bring you this special edition of SPACE PRODUCTS NEWS which focuses on the very real issue of radiation and its effects on integrated circuits.

This special edition is segmented into two sections. In reading it, you will find it to be technically oriented; however, even the non-technical, casual reader will obtain a good overall understanding of the issues involved. A glossary is provided at the back of the newsletter should you come across any terms with which you may be unfamiliar.

Below is a brief synopsis of each Section.

SECTION 2: THE SPACE RADIATION ENVIRONMENT

The space environment is discussed in this Section - our current knowledge of the environment and the effects of radiation on ICs. The authors highlight and provide specific examples of the effects of ionizing radiation, including catastrophic circuit failure, gradual degradation, and corruption of data. Also discussed are the critical issues which a designer must consider when making a choice between radiation hardened and non-radiation hardened parts.

Section 2.1, "A Historical Perspective": Fifty years of experiments and analyses which form the foundation of the current understanding of the space radiation environment are discussed.

Section 2.2, "Space Radiation Environments": Understanding the space radiation environment is the first step in creating systems that can operate effectively in it. Discussed are the radiation threats to space vehicles and the electronic and electrical systems controlling these vehicles.

Section 2.3, "Radiation Effects on Integrated Circuits": An understanding of the effects of radiation threats to spacecraft and the nature of the interaction of these radiation threats with electronic and electrical spacecraft systems is critical. Specifically discussed are the effects of ionizing radiation, including single event effects.

Section 2.4, "Performance Tradeoffs: General Characteristics of Rad Hard versus Commercial and Rad Tolerant ICs": Using circuits specifically designed for the space environment provides significant system design advantages. Discussed in this Section are "typical" performance parameters and general characteristics of radiation hardened (i.e., guaranteed), radiation tolerant, and commercial ICs, and critical considerations and design and process approaches to minimize radiation effects.

Section 2.5, "Rad Hard Microcircuits in Satellite Applications: The Real Costs": There are "hidden" design costs associated with using components not specifically designed for the space radiation environment. This Section explores the cost-of-ownership in using industrial grade non-radiation hardened ICs.

SECTION 3: MANUFACTURING ICs FOR THE SPACE ENVIRONMENT

Section 3 discusses the three factors that are essential for the production of radiation hardened integrated circuits: process design and control, circuit design, and hardness assurance. The authors show how these three factors enable Harris to provide you with radiation hardened ICs capable of withstanding the rigors of the space environment.

Section 3.1, "Circuit Design Techniques for Radiation Hardness": Designing ICs to withstand the rigors of space applications requires the intimate matching of circuit design to process parameters. The processes used to fabricate hardened ICs are designed to minimize the effects of radiation on device, and therefore circuit, operation. Conversely, circuit designs are optimized to provide the maximum tolerance to device level effects.

Section 3.2, "Radiation Hardened Technology at Harris": Harris has developed several different process technologies to provide the levels of hardness necessary for the harsh environments in which modern electronic systems operate. These processes are specifically tailored for the types of circuits involved. With over 325 radiation hardened circuit types available, Harris has developed a very broad portfolio of radiation hardened processes, including Bulk CMOS, SOS, DI Bipolar/CMOS, SOI, bonded wafers and others. Many of these are discussed in this Section.

Section 3.3, "Quality Assurance in Product Development": A hardness assurance program must be in place to ensure the processes used are in control. Hardness assurance at Harris takes place primarily by SPC (statistical process control) of the wafer fabrication, assembly, and test processes.

We certainly hope that you enjoy this special edition and can use it for future reference. In the inside back cover are listed the phone numbers of all the authors and SPACE PRODUCTS NEWS Editorial Board Members; should you have any questions, please feel free to call. All of us at Harris Semiconductor are only here to serve you. Use these numbers freely.

At Harris Semiconductor, we continue to be dedicated to the global space market. With over $100,000,000 in rad hard product sales and an aggressive new product program, we plan to continue servicing your needs with the highest value added radiation circuits for as long as mankind continues to explore and take advantage of the many opportunities that space can provide.

Scott Moody is the Vice President of Space Products Operation. In his position, he is responsible for the overall activities of space qualified radiation hardened standard and ASIC products. Moody has been employed by Harris Semiconductor in a variety of positions over the past 13 years. He holds a BSIE from North Carolina State University and an Executive MBA from the University of Florida.

A Historical Perspective

By Chuck Tabbert

Approximately 50 years of research have gone into the present knowledge base concerning the space environment, with a multitude of experiments and observations each providing another piece of the puzzle. This Section will briefly discuss the origins of this knowledge.

By most accounts, the space age began in 1946 with scientists using rockets left over from World War II to take physical measurements in the upper atmosphere. In 1946 it was written, "A satellite vehicle with appropriate instrumentation can be expected to be one of the most potent scientific tools of the Twentieth Century. The achievement of a satellite craft would inflame the imagination of mankind and would probably produce repercussions in the world comparable to the explosion of the atomic bomb ..."[1]

Prior to the space age:

- the Earth's atmosphere was thought to extend upward a few hundred miles and then essentially end
- the Earth's magnetic field was thought to be quite like the field of a bar magnet, extending into space and gradually getting weaker and weaker
- the Sun was thought to emit little but visible light
- it was understood that a magnetic storm frequently occurred at the Earth shortly after a solar flare

In trying to interpret the magnetic storm process prior to the advent of actual space measurement, Chapman and Ferraro [2] provided an important clue to the Earth's exoatmospheric environment. They suggested that when a solar flare occurred, the Sun emitted a plasma cloud which traveled at such a velocity that it reached Earth approximately one day later. They theorized that the plasma would compress the Earth's magnetic field and therefore increase the magnetic field at the Earth's surface, as observed. This model is now known to be correct; we now know that a solar wind flows continuously from the Sun and is strengthened at the time of flares. In trying to explain solar magnetic storms, Singer [3] suggested that the main phase of a storm was due to drifting particles trapped in the Earth's magnetic field. This idea contained some of the ingredients necessary to describe what are presently regarded as radiation belts.

The "Space Race" began on July 29, 1955, when the White House announced that the U.S. would launch "small unmanned Earth-circling satellites as part of a U.S. participation in International Geophysical Year (IGY) 1957-1958". Two days later, Soviet academician Leonid I. Sedov called a press conference and stated that in the late summer or early autumn of 1957 Soviet scientists would launch a satellite of greater size than the 21 pound satellite the U.S. proposed [4]. The U.S.S.R.'s Sputnik was launched October 4, 1957; the U.S.' Explorer I was launched on January 31, 1958, and the race was on!

In 1958, Van Allen [5] was credited with the discovery of the radiation belts that now bear his name. Explorer I was launched with a Geiger counter aboard (supplied by Van Allen's Iowa University group). Without a tape recorder, the only data recovered was from passes over receiving stations. Post-flight data revealed "gaps" in cosmic rays at high altitudes over South America. Explorer III (II went into the ocean), launched successfully on March 26, 1958, was outfitted with a Geiger counter and flight data recorder, and again revealed "gaps". The only reasonable explanation, put forth by Carl McIlwain [7] of the Iowa group, was that the counter had entered a region of very large particle fluxes which caused the counter pulses to overlap in such a way as to not trigger the electronics, thus stopping the count rate. Van Allen suggested in his first public lecture on satellite results [5] that cosmic rays did not cause this peculiar radiation, but rather a large flux of particles trapped in the Earth's magnetic fields.

It is interesting to note that the Soviet satellite, Sputnik II, launched on November 3, 1957, was

equipped with Geiger counters (but no recorders) and might have discovered the radiation belts, but its closest flight path to Earth was in the north so that it was underneath most of the radiation belts when it was monitored in the U.S.S.R. (Remember, with no flight recorders, satellite data could only be gathered when the satellite was in range of a ground station.)

On December 5, 1958, the Pioneer III spacecraft was sent to a distance of 107,400 kilometers from the Earth. It was intended as a lunar probe but apparently could not break completely free of the Earth's gravitational pull. It carried two Geiger counters and measured the spatial extent of the trapped radiation discovered by Explorer I. Combining results from this mission with the data from Explorer IV led to the first complete map of trapped radiation and to the concept of inner zones and outer zones as we understand them today. Data obtained from Pioneer IV showed the outer zones' particle density varied in time whereas the inner zone was very stable in time.

Prior to the discovery of the Van Allen belts, the U.S. and U.S.S.R. were apparently preparing to conduct trapped particle radiation belt experiments by detonating high-altitude nuclear devices. The Argus tests of 1958 proposed by Christofolis [6] were to see how well the Earth's magnetic field would hold electrons injected by such explosions. (Table 1 below lists tests to date.) Trapped particles resulting from the Argus explosions were observed by Explorer IV, and thus the ability of the geomagnetic field to trap charged particles was directly experimentally verified by Argus [7], which reinforced the theories of particle belts. Also demonstrated was that a shell of particles (approximately 100 km thick) put into the magnetosphere was stable for several weeks; the shells did not drift or broaden appreciably.

These nuclear activities produced sufficient electronic pumping of the Van Allen belts to cause failure in the communications satellite, Telstar I. Not long after the Telstar failure, Nikita Khruschchev, Premier of the U.S.S.R., announced that such radiation vulnerability would be considered a possible means to destroy future U.S. military space systems. This vulnerability heightened the United States' research efforts into protecting satellite assets and contributed greatly to furthering the understanding of the space environment and how satellite systems react to radiation.

Even though the perceived man-made threat against satellite assets has apparently diminished, satellites continue to be vulnerable to the effects of the natural space radiation environment. This vulnerability is heightened in today's technological thrusts. In fact, a disabling event may be even more likely to occur now because presently used commercial VLSI circuits, like dynamic RAMs, are more radiation sensitive than the circuits that were part of the 1962 Telstar satellite. The advent of the use of smaller and smaller geometry integrated circuits combined with increasing mission requirements has led to present concerns over phenomena known as single event upsets. These anomalies have been observed in both the labora-

EXPLOSION	LOCALE	DATE	YIELD	ALTITUDE (APPROX IN kms)
Argus I	South Atlantic	8/27/58	1kt	200
Argus II	South Atlantic	8/30/58	1kt	250
Argus III	South Atlantic	9/6/58	1kt	500
Starfish	Johnson Island, Pacific Ocean	7/9/62	1.4Mt	400
U.S.S.R.	Siberia	10/22/62	Several Hundred kt	Unknown
U.S.S.R.	Siberia	10/28/62	Submegaton	Unknown
U.S.S.R.	Siberia	11/1/62	Megaton	Unknown

Table 1
Exoatmospheric nuclear tests to date [8]

tory and in spacecraft since the early to mid 1970's. Their effect on integrated circuits, as well as methods to mitigate those effects, will be discussed in later Sections.

Our society has become dependent on satellites for routine navigation (GPS), meteorology (DMSP and NOAA), communication (INMARSAT et. al.), as well as for surveillance (DSP) and command and control operations needed for national security purposes (MILSTAR). The booming commercial satellite industry, with its emphasis on "lighter, cheaper and faster", can benefit from the knowledge gained concerning the space radiation environment and the technologies that have been incorporated to mitigate these effects. A wise man once said, "those who do not understand the past are doomed to repeat it!"

REFERENCES

[1] "Preliminary Design of an Experimental World-Circling Spaceship", May 1946. Project RAND.

[2] W. Chapman and V.C. Ferraro, "A New Theory of Magnetic Storms", *Terrestrial Magnetism and Atmospheric Electricity*, 36, 77-97, 171-186 (1931).

[3] S.F. Singer, "A New Model of Magnetic Storms and Aurorea", *Trans Am Geophys.*, Union, 38 175 (1957).

[4] E.M. Emme, "Aeronautics and Astronautics", 1915-1960, GPO (1961).

[5] J.A. Van Allen, "The First Public Lecture on the Discovery of the Geomagnetically Trapped Radiation", *State University of Iowa Report*, 60-13, (1960).

[6] N.C. Christofolis, "The Argus Experiment," *J. Geophy. Res.*, 869 (1959).

[7] J.A. Van Allen, C.E. McIlwain, and G.H. Ludwig, "Satellite Observations of Electrons Artificially Injected into the Geomagnetic Field", *J. Geophy. Res.*, 64, 877 (1959).

[8] W.N. Hess, *The Radiation Belt and Magnetosphere*, Blaisdell Publishing Company, 1968.

The following sources are available for additional information regarding the history of our knowledge of the space radiation environment.

1) "Scientific Uses of Earth Satellites" by James A. Van Allen, copyright 1956 by The University of Michigan Press.

2) "Satellite Environment Handbook" by Francis S. Johnson, copyright 1961 by Lockheed Aircraft Corporation.

3) "Physics and Chemistry in Space" by J.G. Roederer, copyright 1970 by Springer-Verlag.

Chuck Tabbert is manager of Customer Engineering in the Harris Semiconductor Military and Aerospace Division (M&AD). A former Air Force officer, Tabbert was the chief of Satellite Survivability for the Navstar Global Positioning System program office. He holds a BSEE from the University of Florida and an MBA from Northrop University (Inglewood, Calif.).

Space Radiation Environments

By Steve Rivet

As Section 2.1 highlighted, our knowledge of space and its radiation environment has exploded over the last 30 years. Today, satellites that affect our everyday lives must operate in these extremely harsh environments. Without a solid understanding of the environment in which these satellites operate, our ability to communicate, navigate, forecast weather, map environments and explore outside our own planetary system would all be significantly impaired. Even high altitude commercial airliners flying polar routes [1] have shown documented cases of avionics malfunctions due to radiation events. Particles responsible for these effects come from a variety of sources both within and beyond our solar system and can cause degradation and failures of the electronic and electrical systems controlling these vehicles. Particle spectra and secondary radiation caused by the interaction of these particles with spacecraft materials are collectively referred to as the space radiation environment. Understanding of this environment is the first step in creating systems that can operate reliably in it.

The INTELSAT satellite required immediate ground intervention to prevent loss of attitude control. The potential loss is estimated to be $85-100M per satellite plus $300M in lost revenue.

As indicated earlier, the nuclear fusion in the interior of the Sun creates a stream of electrons and protons (and a small percentage of helium and other, heavier nuclei) known as the solar wind. The solar wind radiates out from the Sun in all directions; its intensity varies with the level of solar flare and sunspot activity. A fairly steady background of much lower numbers of protons and electrons from other stars and heavy ions from sources such as novas and supernovas is also present. In interplanetary space, away from the influence of planetary magnetic fields, these particle streams constitute the entirety of the radiation threat. In the vicinity of planets and stars with significant magnetic fields, some particles are trapped and concentrated in radiation belts, while others are deflected away from low altitudes. The composition and intensity of the radiation threat therefore varies significantly with the path of a vehicle through space. Thus, the designer must not only be cognizant of the space radiation effects, but also must concern himself with the vehicle's flight path.

During a large geomagnetic disturbance (July, 1992), NOAA-11 experienced loss of automatic attitude control.

The motion of charges within a planet's core and residual magnetism in frozen ferrous elements in its crust are responsible for that planet's magnetic field. The Earth's magnetic lines of force extend out into space for many thousands of miles. The region of influence of this magnetic field is known as the magnetosphere and the outer edge of this area of influence is the magnetopause (see Figure 1).

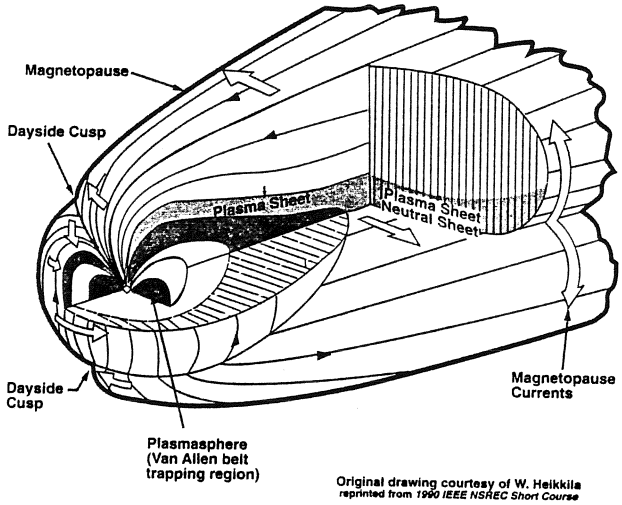


Figure 1
The Earth's magnetosphere

The actual shape of this field is altered by the pressure of the solar wind. The magnetosphere is compressed on the daylit side of the Earth and stretched out on the night side. Charged particles from the Sun or extragalactic sources will be deflected from their paths by the field and tend to follow the lines of force. Particles below a critical energy will become trapped and spiral around these lines of force reflecting back and forth between reflection points [2]. These protons and low energy electrons that become trapped in the near Earth particle environment, or plasmasphere, are known collectively as the Van Allen belts. Higher energy particles are not deflected enough to become trapped, but are effectively shielded from the lower altitudes at the equator.

The dependence of particle concentrations upon both altitude and latitude can be described by the McIlwain L parameter [3]. The L parameter description is a quantitative model for describing the shielding of low latitude/low altitude regions from particles of differing charges and energies. Particles encountering the magnetosphere are deflected along magnetic lines of force; particles striking the magnetosphere at low latitudes (near a plane perpendicular to the Earth's equator) encounter the greatest deflection, and are therefore shielded from low altitudes; only extremely energetic particles make it to the lower altitudes at low latitudes. At high latitudes (on line with the magnetic poles), particles are already traveling along the lines of force and are not significantly deflected. Even relatively low energy particles penetrate to very low altitudes at high latitudes. Figure 2 shows the near-Earth magnetosphere in more detail than Figure 1 and highlights the approximate location of the Van Allen belts. At very low altitudes, the atmosphere shields the surface of the planet from all but the most energetic cosmic rays.

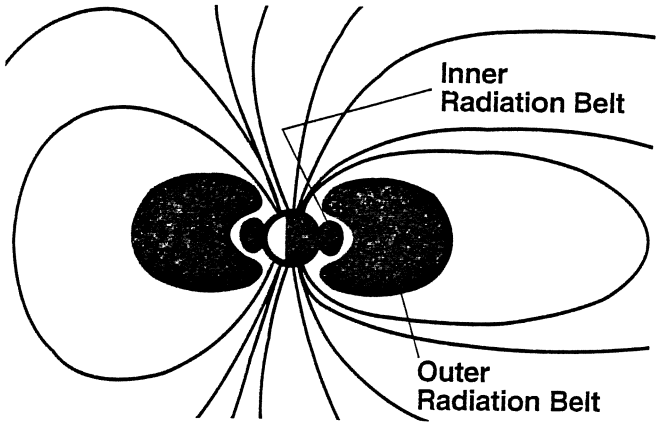


Figure 2
Near Earth magnetosphere and Van Allen belts

The Van Allen belts have been mapped by many scientific spacecraft since their discovery by experiments on board Explorer I. Dosimetry data from these spacecraft have been collated into NASA AE8 (electrons) and AP8 (protons) models; these models describe the time averaged distributions of particles in the Earth's magnetosphere. Figure 3 (next page), reprinted from the *1990 IEEE NSREC Short Course,* illustrates the dependence of electron concentrations versus latitude and longitude at a 500 km altitude. Proton concentration maps are similar.

Notice the higher electron concentrations (expressed here as micro RADS/sec behind an aluminum shield) between 45° and 85° latitude in both the northern and southern hemispheres. This indicates that the belts descend to a lower altitude in these regions. It can be seen that low inclination orbits (less than about 30°) encounter the lowest electron concentrations. This figure also shows the presence of a high electron concentration over the south Atlantic. This high particle concentration area is known as the South Atlantic Anomaly, or SAA. The SAA is caused by the misalignment of the Earth's magnetic north and south poles with its axis of rotation [2]; the magnetic field is weakened and the Van Allen belts reach down to lower altitudes over the south Atlantic. The opposite effect (higher magnetic fields and higher altitude Van

Allen belts) is observed in the Southeast Asian Anomaly. In low altitude low inclination orbits, the SAA dominates the total dose a spacecraft receives.

TOPEX: Altimeter electronics gate arrays are experiencing single event upsets (SEU) in the South Atlantic Anomaly. Star Tracker's Analog-to-Digital converter experienced "hard" SEU.

While AE8 and AP8 are good representations of averaged particle distributions, the cyclical and probabilistic nature of particle emissions from the Sun causes the trapped particle distribution to ebb and flow in response. The March 1991 solar storms, for instance, significantly increased the particle distributions in the two previously mapped belts, and even created a third belt [4]. (It is important that environmental models reflect known variations or that the limitations of static models be accounted for when calculating system dose.)

Charged particles themselves are not the only radiation threat encountered by space vehicles. The electrons, protons, and heavy ions in space penetrate the spacecraft and cause direct damage to the electronic components. Additionally, charged particles losing energy as they penetrate the spacecraft's skin and other structures generate X-rays; these X-rays are known as Bremsstrahlung radiation and can be a significant percentage of the total component level radiation threat. [Refer to the following Section for further detail.]

Figure 4 provides a rough estimate of the radia-

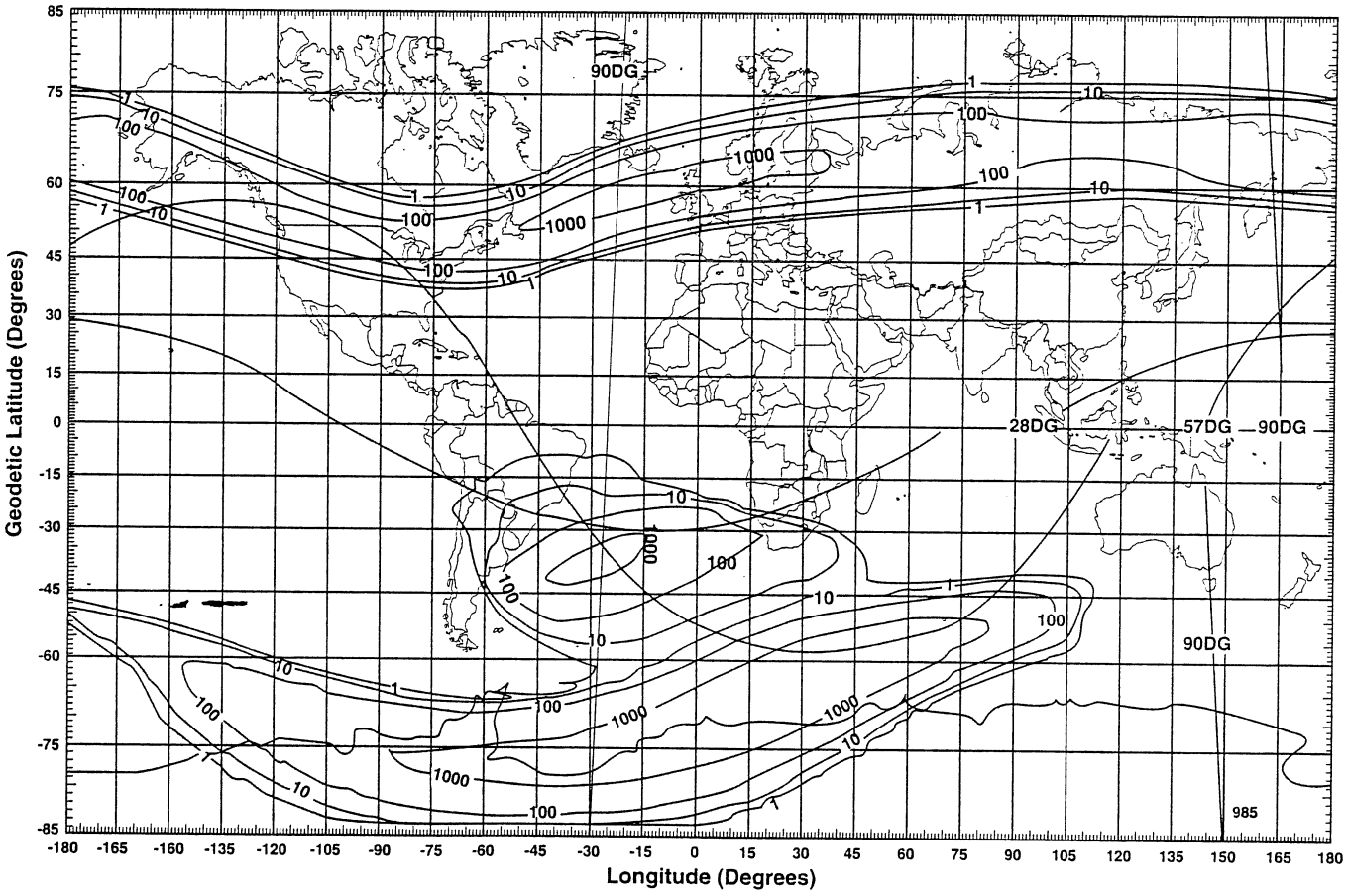


Figure 3
Electron dose at 500 km altitude: AE8-MIN (Epoch of B&L: 1964)
Spherical aluminum shield: 0.2 GM/cm² (Units: RADS/sec x 10^{-6})

tion exposure rates encountered by spacecraft. (For more precise calculations of expected exposure rates, software packages that allow the user to enter the specifics of the orbit and generate the expected dose in that orbit are available.)

- The most benign environment is encountered by satellites in low inclination (< 28°) Low Earth Orbit (LEO, < 500 km). (Refer to Area 1, Figure 4.) Typical dose rates due to trapped Van Allen electrons and protons in this orbit are 100 - 1000 rad(Si)/year. Only a few very energetic heavy ions penetrate to this orbit. However, low earth orbit in a higher polar inclination encounters a significantly increased dose due to the Van Allen belts dipping to low altitudes and a much higher heavy ion flux due to the lack of magnetic deflection of the ions at the poles.
- In the densest regions of the Van Allen belts (Area 3, Figure 4), the dose from trapped particles can rise to 100 krad - 1 Mrad(Si)/year; heavy ions are deflected by the magnetosphere, but penetrate at much higher levels than at equatorial LEO.
- In geosynchronous orbit (GEO) (0° inclination, 36,000 km altitude), spacecraft are outside of most of the Earth's trapped radiation, and subsequently encounter a total dose rate of only about 5 krad(Si)/year. Geomagnetic shielding is fairly weak at these altitudes, which results in a high heavy ion flux. (Area 4, Figure 4, not to scale)
- In interplanetary space, away from planetary magnetic fields, there are no trapped particles; the solar wind dominates the particle spectrum. In these regions there is no geomagnetic shielding, so heavy ion flux is the highest of any environment.

As discussed previously, even the relatively low altitudes where commercial jet aircraft operate are not totally free of particle radiation that can affect the electronics on board. A recent paper by

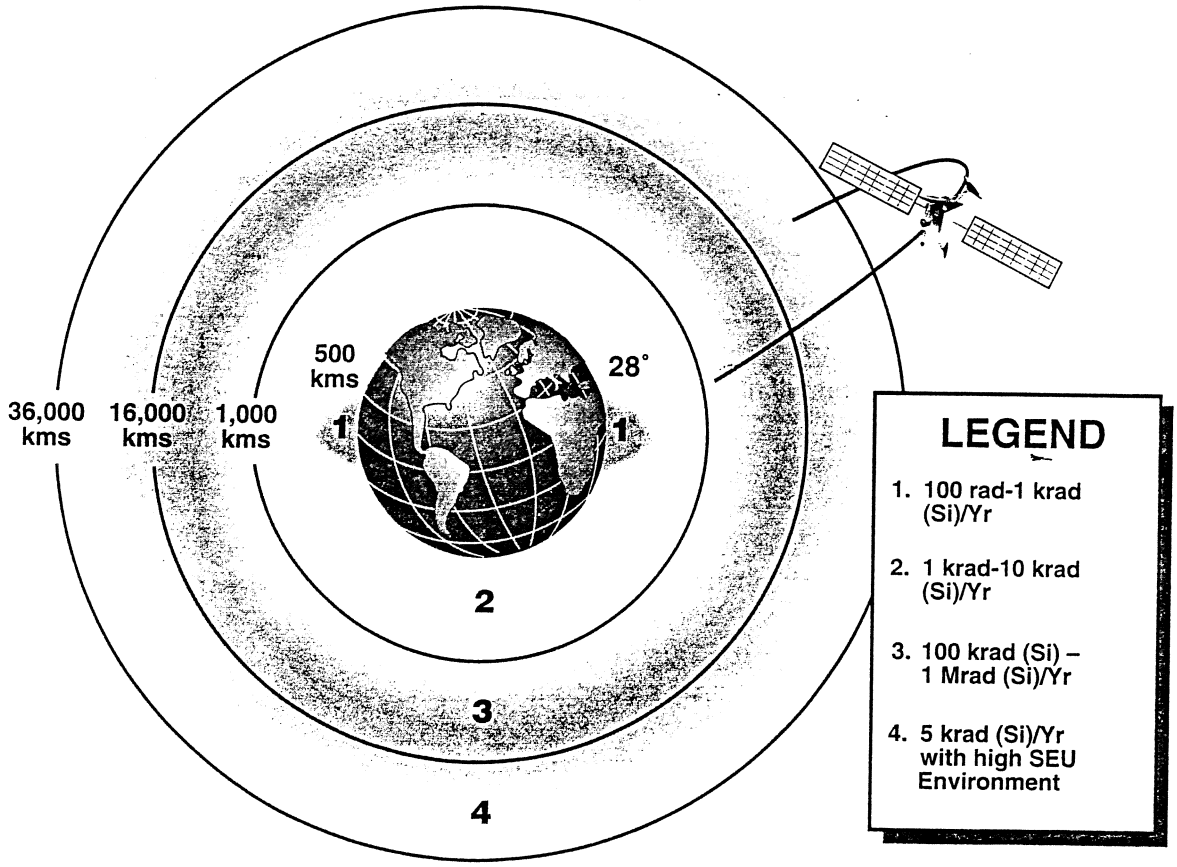


Figure 4
Spacecraft radiation environment

J. Olsen, et al. reports memory upsets aboard commercial airliners flying 10 km altitude polar routes [1]. High energy cosmic rays penetrate to low altitudes in polar regions and interact with nitrogen and oxygen in the upper atmosphere; neutrons from these reactions penetrate aircraft and their electronic components. (Refer to the following Section, "Radiation Effects on Integrated Circuits", for a description of neutron induced single event upsets.)

Current knowlege of radiation threats in environments requires designers to take a variety of measures to counter those threats. Two of these measures include altered flight paths and shielding, both of which may be impossible or prohibitively expensive. The best way to protect against the known environment and provide insurance against the unknown is to use electronics specifically designed for the environment.

REFERENCES

[1] J. Olsen, et al., "Neutron-Induced Single Event Upsets in Static RAMs Observed at 10 km Flight Altitude", *IEEE Transactions on Nuclear Science*, April 1993.

[2] E. G. Stassinopoulos, "Radiation Environment of Space", *IEEE NSREC Short Course*, July 1990.

[3] C. E. McIlwain, "Coordinates for Mapping the Distribution of Magnetically Trapped Particles", *Journal of Geophysics Res*, vol. 66, No. 11, 1961.

[4] J. B. Blake, et al., "Identification of an Unexpected Space Radiation Hazard", *IEEE Transactions on Nuclear Science*, December 1992.

Steve Rivet is the Advanced Digital Product Marketing Manager in Harris Semiconductor's Space Products Operation. He has been employed by Harris since 1983, holding several engineering and management positions. Rivet holds a BSEE from the University of Michigan and an MBA from the Florida Institute of Technology. His publications include contributions to IEEE Transactions on Nuclear Science and several Harris publications, including SPACE PRODUCTS NEWS.

Radiation Effects on Integrated Circuits

By Jack Clark and Steve Rivet

Over the last few decades we have seen an explosion in the advancement of electronics technology. The cornerstones of this explosion were the development of the transistor and eventually, integrated circuits (ICs). Today, electronics that two decades ago took up a room and ten years ago filled a desk, can now be fitted on one integrated circuit smaller than a fingernail. While this explosion in technology has allowed us untold opportunities in space, it is not entirely without some sacrifices. Semiconductors, including ICs, can be particularly sensitive to space radiation threats. This Section summarizes the effects of radiation on integrated circuits.

There are two types of radiation threat to semiconductors in space: the direct effect of charged particles in the environment that penetrate the spacecraft and the components within and secondary photon radiation known as Bremsstrahlung

RADIATION TYPE	NATURE OF INTERACTION WITH MATERIAL
1. PHOTONS (X-Rays, γ-rays, etc.)	a. PHOTOELECTRIC EFFECT- incident photon is completely absorbed by a target atom, which then expels an electron; predominates for low energy photons (< 50 keV) b. COMPTON SCATTERING-incident photon is scattered, giving up portions of its energy to several atoms, which then emit electrons; this mechanism dominates for photons of approximately 50 keV to 20 MeV c. PAIR PRODUCTION-incident photon is completely absorbed by a target atom which emits an electron-positron pair; occurs only for very high energy (> 20 MeV) photons striking high atomic number targets
2. CHARGED PARTICLES (electrons, protons, heavy ions)	a. COULOMBIC SCATTERING-incident charged particle is scattered in the target material giving up energy to target atoms in multiple collisions; the target atoms then emit an electron or electrons b. NUCLEAR INTERACTIONS-incident particle is completely absorbed by a target atom's nucleus, which then usually decays into two or more fission fragments c. ATOMIC DISPLACEMENT-the incident particle knocks the target atom out of its place in the crystal structure; electrons may be ejected from the displaced atom
3. NEUTRONS	a. NUCLEAR INTERACTIONS-see above b. ATOMIC DISPLACEMENT-see above

Table 1
The interaction of radiation with integrated circuits

radiation. Bremsstrahlung radiation is generated when high energy particles slow down as they pass through a target material; the kinetic energy lost by the particles is radiated out of the target material in the form of high energy photons. In a satellite in Earth orbit, electrons and protons trapped in the Van Allen belts strike the structural components (usually aluminum) and bathe the interior of the spacecraft in X-rays. These Bremsstrahlung X-rays can be the predominant radiation threat to components in the interior of the spacecraft.

The interaction of charged particles and photons with integrated circuits depends upon a number of factors such as mass, charge state, and kinetic energy of the incident particle or energy of the incident photon, and on the mass, charge (atomic number), and density of the integrated circuit material. Some examples of the specific interactions are defined in Table 1 (page 2.3-1); this Section will be limited, however, to the effects of ionizing radiation (including single events) on silicon ICs.

Electrons and Bremsstrahlung X-rays produce ionization in the IC materials, most notably in the silicon and silicon dioxide layers of the circuit. The accumulation of ionization is commonly referred to as the total dose a circuit receives. In natural environments, the rate at which this ionization is accumulated (dose rate) is very low, and the electron-hole pairs produced in the silicon layers are quickly collected at the circuit's power supply nodes with no appreciable effect on the circuit. This collection of charge manifests itself as low level leakage currents throughout the circuit. It is the ionization in the oxide layers of the circuit that is responsible for degradation and eventual functional failure of circuits exposed to electron and Bremsstrahlung radiation. Shifts in metal oxide semiconductor (MOS) transistor thresholds due to silicon/silicon dioxide (SiO_2) interface charge trapping and generation of interface states are the dominant mechanisms causing device degradation. Even in bipolar circuits, the parasitic MOS transistors dominate the circuit's response to ionizing radiation.

Figure 1 shows a schematic representation of the generation and trapping of charge in an MOS transistor [1]. For clarity of illustration, the dose is accumulated in a very short time with respect to the movement of the electron-hole pairs generated.

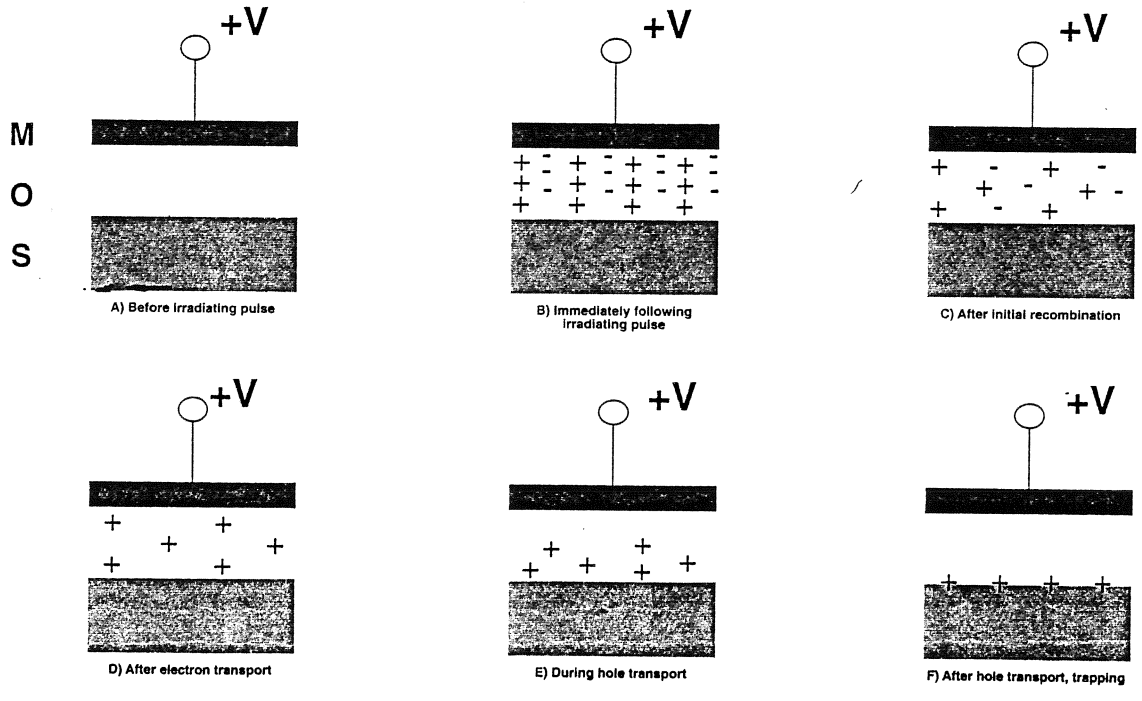


Figure 1
Generation and trapping of charge in an MOS transistor

In the natural space environment, the dose accumulation is gradual; the illustrated effects occur continuously and simultaneously. Figure 1A shows the MOS transistor in cross section before the irradiation, while Figure 1B shows the electron-hole pairs immediately after the irradiating pulse, before the carriers begin to recombine. Recombination reduces the number of electron-hole pairs, as shown in Figure 1C. If there is no bias on the transistor (no field across the oxide), almost all of the electron-hole pairs will recombine. However, with a positive gate bias, the highly mobile electrons will migrate to the positively biased metal gate within several picoseconds of irradiation, leaving the situation illustrated in Figure 1D. The holes, which are about a million times less mobile in oxide than the electrons [1], begin a much slower migration towards the negatively biased silicon channel (Figure 1E). Some percentage of these holes (depending upon interface quality, oxide purity, and several other factors) become trapped at the interface, as shown in Figure 1F. These trapped charges cause transistor thresholds to decrease; N channel enhancement mode transistors become much easier to turn on, while P channel transistors become harder to turn on (i.e., thresholds become more negative). These threshold shifts can eventually cause circuit failure.

The interface trapping sites will eventually become saturated and the transistor thresholds will not change further. Additional charges that migrate to the interface will not become trapped when these sites have been filled. Trapped charge will also anneal after the source of ionizing radiation is removed; the annealing rate depends upon the properties of the silicon/silicon dioxide interface and occurs much more quickly at high temperatures than at low temperatures.

Another mechanism that affects MOS threshold voltages is the formation of interface states. Interface states have been explained by several different physical processes (Refer to *IEEE Transactions on Nuclear Science* for the last 5-10 years for details of the evolution of theories on the physics of interface state production) and their behavior is fairly well understood. Interface state production is a much slower process than charge generation and trapping, and dominates transistor response at very high accumulated doses. Figure 2 illustrates the effects of both charge trapping and interface state generation on MOS threshold voltages for N and P channel transistors. Interface states will increase an N channel transistor's threshold, and make a P channel transistor's threshold increasingly negative. Interface states anneal much more slowly than trapped charge; at room temperature the annealing process may take many years.

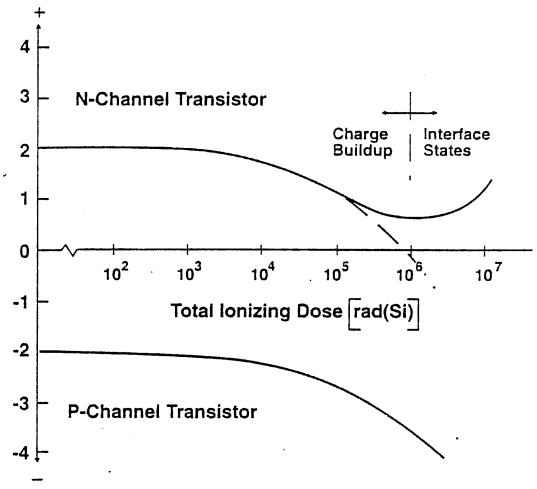


Figure 2
Charge trapping and interface state generation effects on MOS threshold voltages

Interface states also reduce the surface mobility of the MOS transistor channel, which reduces the current drive the transistor is capable of delivering. At high doses the mobility degradation may be significant and cause circuit failures.

Another class of radiation effect on ICs is known as single event effects (SEE). SEE are the responses of an IC to the passage of a single highly energetic charged particle, and include single event upset (SEU), single event latchup (SEL), and single event burnout or gate rupture (SEB or SEGR). SEGR applies only to high voltage MOS transistors. Very energetic charged particles will penetrate a spacecraft structure and can travel through the electronic components inside. As the particle travels through the silicon layers of an IC, it loses energy; this energy creates ionization or electron-hole pair generation along the path of the particle. In general, the higher the mass and charge of the impinging particle, the greater the amount of ionization produced.

UoSat-2: During the September 1988 to May 1992 time period, almost 9,000 single event upsets (SEU) were observed. The majority (75%) of the errors occurred in the South Atlantic Anomaly (SAA) region, with events at high latitudes attributed to galactic cosmic rays and solar proton events.

Single event burnout (SEGR) has been primarily observed in power MOSFETs where extremely high voltages and electric fields are present. It has also been observed in EEPROM technologies during the high voltage portion of the write cycle. These high electric fields give rise to large currents flowing through the oxide during a charged particle strike, along with localized heating; this results in the destruction of the oxide and subsequent device failure. This is generally considered the most spectacular of the single event effects associated with ionizing particle exposure of MOSFET devices. It also does not generally occur unless the incident particle is very massive. Some testing has shown that ionized elements at or below the Linear Energy Transfer (LET) of ionized argon will probably not cause an SEGR even under high bias conditions. (Note that SEGR is a permanent effect, unlike the other single event effects we will discuss later.)

Another devastating effect is the activation of a parasitic silicon controlled rectifier (SCR) contained within some CMOS process technologies, resulting in single event latchup. Latchup has the potential to destroy the device or render a portion of the circuit inoperable while in the latched condition. The device must be powered off to reset the SCR to the off state. This latchup event is triggered by the passage of the ionizing particle, resulting in current injection into the "gate" terminal of the parasitic SCR which exist in most bulk CMOS and bipolar processes. Careful device design, rigorous layout groundrules, and the use of thin epitaxial silicon layers over N++ substrates or insulated substrates such as silicon on sapphire (SOS) or silicon on insulator (SOI) can reduce or eliminate the possibility of activating the parasitic device and make such an occurrence a physical impossibility.

Once the process and layout groundrules in junction isolated CMOS are established to prevent achieving a viable SCR, latchup will not occur, regardless of the layout used. SOS, SOI and other insulated substrate technologies are designed to physically separate the junctions so that an actual SCR cannot be formed; the possibility of latchup is thus eliminated entirely. Another bonus received from using insulated substrate processes is the elimination of the capacitance associated with the reverse biased isolation junction's capacitance and the resultant increase in circuit speed.

The most common effect associated with an ionizing particle strike is the upset of circuit elements resulting in a temporary or permanent change of state for that circuit element. This is called single event upset (SEU) and is a very serious concern for memory devices whose contents are critical. While error correcting hardware and codes are available for scrubbing the memories of errors which may occur due to SEU, the ideal solution is to prevent the upsets with SEU hardened memory designs.

Polar Earth Resources Satellite -1 (ERS-1): Precision Range and Range Rate Equipment (PRARE) experienced proton induced latchup. Equipment shut off after five days. Estimated cost was $25M per experiment, with associated launch costs of $20-60K per pound.

Single event upsets occur due to charge deposition of sufficient magnitude to cause a change of state at a critical node. (See Figure 3, page 2.3-5) Figure 3a shows a cross section of a memory cell as the heavy ion passes through. Figure 3b shows the impact of the change of state of the memory element.

When a sufficiently large charge is deposited at or near a reverse biased (off) PN junction, charges drift to their respective electrodes. This results in a current injection onto that node. Figure 4 (next page) shows a six transistor cross coupled latch commonly utilized in static memories. The figure illustrates the sensitive regions of the circuit both schematically and graphically (a bulk CMOS technology is illustrated here).

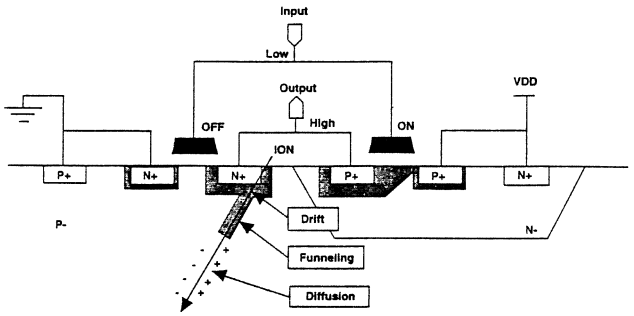


Figure 3a
Cross section of a memory cell

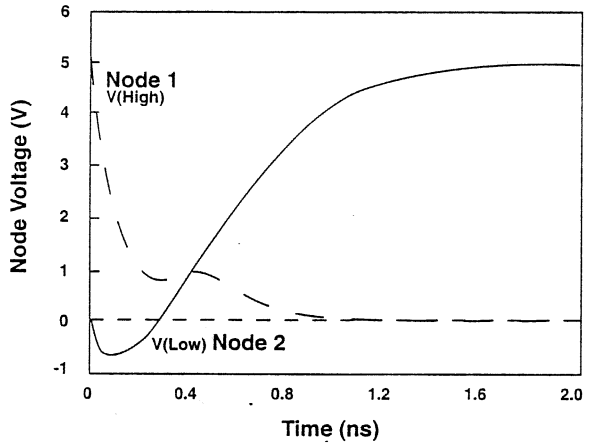


Figure 3b
Change of state of the memory element

In combinational logic circuits, single event upsets can cause momentary changes of state of the logic gates; the circuit generally recovers in less than 5 ns for actively driven circuit nodes. This pulse can propagate to a latching storage element where it is possible for it to become latched as an electrical error. The SEU induced pulse will usually be filtered out through many stages of logic; this is, of course, dependent upon the magnitude of the injected charge and the performance of the technology.

Protons and neutrons do not leave an ionized trail dense enough to cause direct single event upsets. Proton and neutron induced SEU occurs when a proton or neutron collides with a silicon nucleus and the recoiling nucleus fragments leave an ionized trail. This type of nuclear reaction is known as spallation. Spallation has been observed at both low earth orbits (due to protons) and even in avionics at very high altitudes (due to neutrons)

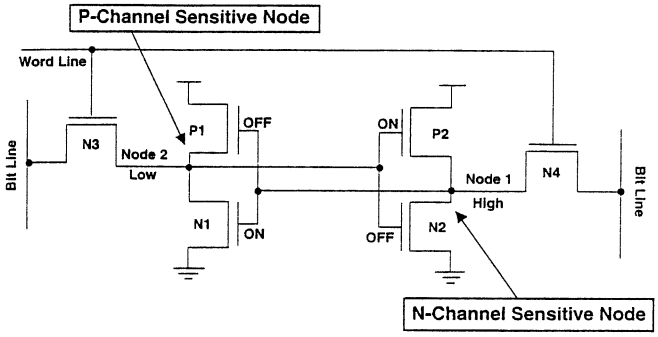


Figure 4
Six transistor cross coupled latch

[2]. Generally, the proton and neutron interactions do not induce sufficient electron-hole pair generation of the spallation products to upset a circuit node specifically designed to be rad hard; however, many commercial ICs are sensitive to such low levels of charge deposition that proton and neutron SEU can significantly contribute to system error levels.

CONCLUSION

Ionizing radiation can cause significant, instantaneous corruption of data (SEU), sudden catastrophic circuit failure (SEL and SEGR), or gradual degradation and eventual circuit failure. The techniques used to reduce or eliminate these effects and optimize the performance of space systems will be explored in the following Sections.

REFERENCES

[1] J. R. Srour, et al., "Radiation Effects On and Dose Enhancement of Electronics Materials", Noyes Publications.

[2] J. Olsen, et al., "Neutron-Induced Single Event Upsets in Static RAMs Observed at 10 km Flight Altitude", *IEEE Transactions on Nuclear Science*, April 1993.

Jack Clark is a design engineer in Harris Semiconductor's Military and Aerospace Division (M&AD). He has designed several radiation hardened SRAMs in SOI technologies, including the RHD-1 256K SOI SRAM. Prior to joining M&AD, Clark worked in the Commercial Products Division (currently called SPD) of Harris Semiconductor, where he was responsible for the design of several commercial high speed SRAMs. Clark holds a BS in Electrical Engineering from the University of South Florida and an MSEE from the Florida Institute of Technology. He holds two patents on circuit design techniques and has co-authored eight technical papers on rad hard circuit design.

Steve Rivet is the Advanced Digital Product Marketing Manager in Harris Semiconductor's Space Products Operation. He has been employed by Harris since 1983, holding several engineering and management positions. Rivet holds a BSEE from the University of Michigan and an MBA from the Florida Institute of Technology. His publications include contributions to IEEE Transactions on Nuclear Science and several Harris publications, including SPACE PRODUCTS NEWS.

Performance Tradeoffs: General Characteristics of Rad Hard versus Commercial and Rad Tolerant ICs

By Don Koch

In previous Sections we have provided a description of the space radiation environment and its effects on integrated circuits (ICs). We will now evaluate the performance tradeoffs of using radiation hardened versus commercial and rad tolerant components in this environment The key issues on this topic which will be discussed include: (1) working definitions of commercial, rad tolerant, and rad hard components as they apply to the space environment; (2) critical considerations when choosing rad hard vs. commercial components; and (3) design and process approaches that minimize radiation effects.

WORKING DEFINITIONS

When a satellite systems designer is reviewing the component options between radiation hardened and commercial devices, there is a series of fundamental issues that must be understood, including the definition of rad hard, rad tolerant, and commercial device types. Table 1 (below) identifies general characteristics of radiation hardened ICs as they compare with rad tolerant and commercial parts. While some users may have slightly different definitions for these categories, this table attempts to quantify the general characteristics of the parts.

CRITICAL CONSIDERATIONS

Systems designers must also understand the following critical considerations when choosing a device to be used in the space environment.

- It is essential that the costs of the integrated circuits be evaluated in the context of other associated cost drivers on the program. While

RAD HARD	RAD TOLERANT	COMMERCIAL
Designed for specific hardness level	Hardness offered as a by-product of the design	Hardness limited by inherent process and design; customer risk
Wafer lot rad test	Sample rad test	Customer rad test
Guaranteed to remain within data sheet limits	Usually tested to functional fail only	Customer rad test and risk
Process variables under statistical process control (SPC)	No lot radiation controls	No lot radiation controls
Total Dose: > 200 krad to >1 Mrad	20 krad to 50 krad (typical)	2 krad to 10 krad (typical)
SEU Threshold LET: 80-150 MeV/mg/cm ^{2}	20 MeV/mg/cm ^{2} (typical)	5 MeV/mg/cm ^{2} (typical)
SEU Error Rate: $10E^{-10}$ to $10E^{-12}$ errors/bit-day	$10E^{-7}$ to $10E^{-8}$ errors/bit-day	$10E^{-5}$ errors/bit-day (typical)
Latchup: Silicon on insulator (SOI) technologies: none Bulk rad hard technologies: guaranteed extremely low sensitivity	Customer evaluation and risk	Customer evaluation and risk

Table 1
General characteristics of rad hard, rad tolerant, and commercial integrated circuits

commercial ICs may reduce the initial procurement costs, cost adders may actually drive the total program costs above the total cost when radiation hardened components are used. These cost adders include (1) radiation screening performed by the systems builder, (2) additional qualification costs for commercial ICs, (3) system redesign costs to increase shielding, (4) cost of launch weight associated with shielding, (5) design and launch costs for larger power supplies, and (6) risk mitigation costs.

- It is important to realize that component costs are 3-5% of the total cost of a satellite; when evaluating the cost/risk tradeoffs associated with using commercial parts, this factor must be considered. The relatively small up-front investment of using properly designed components can pay huge benefits in the life cycle costs. Specific (and often times hidden) cost tradeoffs will be explored further in the following Section.
- Costs for Class S components are driven primarily by low volume, specialized screening flows, and large qualification costs amortized over a small quantity of parts. The difference in wafer fabrication costs between a rad hard wafer and a commercial wafer is relatively small. As a result, a commercial circuit procured to Class S specifications will cost nearly the same as a radiation hardened circuit to the same specifications. The procurement costs for ICs can be decreased by using standardized screening flows, combined procurement (to reduce qualification costs per circuit), and generic data. Using rad-soft components does not significantly reduce cost, but greatly increases risk.
- There are no components that are ideal for all parameters. Integrated circuit design involves a series of engineering tradeoffs in performance (with cost being considered a performance parameter). Commercial components tend to emphasize features that make them useful in commercial applications, such as low cost, latest (possibly immature) commodity technology, and high speed over moderate temperature and voltage ranges. These features may be achieved at the expense of features needed for long-term space applications, namely, mature, reliable processes with good performance over wide temperature and radiation environments.
- Shielding of commercial components is an approach used by some systems designers. While shielding can reduce the total dose radiation seen by the components, other radiation effects are not impacted by shielding. Effects such as single event upset (SEU) and single event latchup (SEL) can still occur. Unfortunately, these catastrophic effects are expensive to evaluate on commercial components. Circumvention techniques such as frequent rebooting of the system and current limiting power supplies to avoid latchup burnout are also expensive.
- The variety of radiation effects on materials (previously discussed in Section 2.3) can be well controlled on processes that have been designed with radiation effects in mind. The key process parameters on Harris' rad hard processes are under statistical process control (SPC). The key process parameters (from a rad effects standpoint) may not even be known on a commercial process.
- Screening commercial components to a radiation specification is a fairly high risk proposition. Total dose capability of commercial processes or of different lots or circuits on the same process can vary widely, leading to a high probability of unusable parts. Also, evaluating parts for SEU and SEL is an expensive undertaking.

PRODUCT PROCESSING AND DESIGN

In order to provide high performance parts for the space radiation environment, it is essential to evaluate both process and design considerations. (Both are discussed in subsequent Sections.) Of particular note is the superior SEU capability and latchup free operation that is inherent in silicon on sapphire (SOS) and silicon on insulator (SOI) device structures. Along with rad hard gate oxides (used at Harris for over 15 years), SOS and SOI technologies provide exceptional performance over all radiation environments. This allows for superior device stability over the entire radiation, temperature and life time of the part.

Once a rad hard process has been established, it is critical to use fundamentally sound design approaches for maximum radiation immunity. (Detailed approaches are outlined in Section 3.1.)

In order to understand the significant system performance advantages of using rad hard devices, it is useful to look at specific examples of available rad hard devices versus commercial "alternatives".

Spacecraft Memory Systems - Referring back to Table 1, the SEU error rates vary dramatically from rad hard to commercial devices. Shielding, while very expensive, is often considered in space applications. While shielding can make the total dose capability of rad tolerant devices acceptable, the SEU rates cause serious problems. If one evaluates a typical 30 Mbit memory system, simple mathematics will highlight the problems.

- Using a commercial component error rate of $1E^{-5}$ errors/bit-day, a 30 Mbit system will have over 10 errors per hour. Error correction and/or rebooting the entire system is nearly impossible with this kind of error rate, and will most certainly affect mission success. The magnitude of the problem is somewhat reduced with rad tolerant devices.
- Using a rad tolerant component error rate of $1E^{-7}$ errors/bit-day, the 30 Mbit system has an error every three days. This can still be a serious systems operation problem.
- Using a radiation hardened memory with an error rate of $1E^{-11}$ errors/bit-day, the error rate is approximately 1 error every 10 years.

Clearly, the use of rad hard memories greatly enhances the system design. One need only to review system problems encountered on Hubble, Magellan, ERS-1, and other systems to understand that SEU can cause serious operability issues.

The Hubble Space Telescope experienced SEU in the fine guidance system when passing through the South Atlantic Anomaly (SAA). TDRS-1 frequently experiences SEUs in random access memories and requires ground intervention.

Interface Circuitry - Many systems designers would like to use RS-422 driver/receiver pairs for system interfacing. Commercially available parts pose a serious system design tradeoff for a user because commercial CMOS parts are not very rad hard and have variable output impedance on the driver; commercial bipolar parts have fairly good inherent total dose capability but draw significant static I_{DD} (current supply) and are not latchup immune. Furthermore, the matching of the output

PARAMETER		Harris' HS-26CT31	Competitor's CMOS	Competitor's LS
Functional 500 krad		Yes	No	No
Functional 1 Mrad		Yes	No	No
Static IDD		0.3mA	1.5mA	67mA
IDD 10MHz Unloaded (1 channel active)		8.7mA	4.7mA	82mA
Output Impedance		5 ohms constant	10-∞ variable	5-100 variable
Max Output Drive	IOH	700mA	120mA	100mA
	IOL	500mA	150mA	200mA
Short Circuit I out		150mA	120mA	100mA
Prop Delay	TPLH	12ns	7ns	19ns
	TPHL	12ns	8ns	11ns
	Skew	1ns	0ns	1ns

Table 2
Harris' radiation hardened HS-26CT31 provides distinct performance advantages over commercially available device types

impedance for the commercial drivers is poor, which complicates source termination.

The use of source termination is common practice in satellite data bus designs because it eliminates quiescent power drain required to hold the bus voltage in shunt topologies. To obtain minimum shield current/minimum noise and maximum data rate, the driver must be very well matched to the line and its complementary outputs well matched to each other in time and impedance. Harris' radiation hardened HS-26CT31 has been specifically designed to meet these requirements. Table 2 (page 2.4-3) highlights specific advantages of Harris' device as compared to commercially available parts.

Logic Designs - Figure 1 (below) shows the supply current leakage of commercially available logic devices as compared with rad hard designs. Once again, the commercial parts force the satellite designer into a serious design tradeoff.

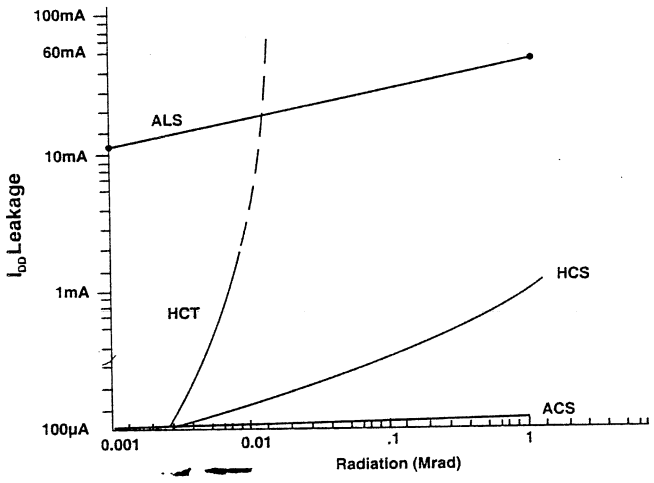


Figure 1
Comparison of radiation hardness for various logic families (I_{DD} leakage vs. rad exposure)

- Commercial HCT (High Speed CMOS with TTL inputs) devices offer low power before irradiation but are extremely leaky at about 10 krad total dose and can exhibit latchup due to cosmic rays. These parts are not designed for radiation environments.
- Commercial ALS (Advanced Low Power Schottky) devices are reasonably rad hard but draw significant current during static operation and may latchup in a cosmic ray environment. Again, these parts are not designed for radiation environments.
- Only the rad hard High Speed CMOS (HCS) and Advanced CMOS (ACS) SOS logic parts offered by Harris provide rad hard, low power latchup-free operation. In the satellite environment, low power is essential in order to minimize power supply volume and weight issues.

Field Programmable Gate Arrays (FPGAs) - The advent of FPGAs would seem to be ideal for satellite systems designers. Xilinx parts, for example, can be purchased in volume and programmed as needed for different applications. Furthermore, this volume of product can be fully qualified so that any qualification costs would be spread over many programs. In-field programmability also allows for rapid system design changes. Unfortunately, the spacecraft SEU error rate associated with the Xilinx RAM cells on the commercial FPGA is a major issue. Since the RAM cells are embedded within the FPGA design (and are the heart of the programmability feature of the part), error correction is impossible in these commercial designs. However, the Harris/Xilinx radiation hardened FPGA (Harris is a licensed Xilinx partner) combines the advantages of the Xilinx architecture with the rad hardness of the Harris insulated substrate SOI technology. The combination is ideal for the space systems designer.

CONCLUSION

In summary, the use of commercial and rad tolerant parts in space system design may occasionally be necessary; however, the utilization of circuits specifically designed for the rigors of the space environment reduces life cycle costs and provides significant system design advantages.

Don G. Koch is a design engineer of radiation hardened digital circuits (both standard product and ASICs) in the Harris Semiconductor Military and Aerospace Division. He has been involved in the characterization of the rad hard CD4000 logic family for the JPL Galileo Program, design of a 6805 microprocessor with Manchester I/O Port, design and yield enhancement of SOS gate arrays, and the development of the SOS radiation hardened family of logic functions. Prior to joining Harris, Koch worked at the Naval Weapons Support Center in Crane, Indiana, as a member of the NASA/NAVY Microcircuit Team (under MIL-M-38510). He holds a BS in Mathematics from the University of Michigan and an MS in Physics from the University of Illinois.

Rad Hard Microcircuits in Satellite Applications: The Real Costs

By Chuck Tabbert and Steve Rivet

As described in Section 2.2, vehicles such as sounding rockets, Earth satellites, and interplanetary and solar probes operate in regions of space where naturally occurring radiation can impact their operation. In Section 2.3, we discussed the radiation effects on electronic components operating in the space environment, and in Section 2.4 we discussed critical performance considerations and tradeoffs in performance of radiation hardened versus commercial and rad tolerant integrated circuits (ICs). In this Section, we will explore the associated "hidden" design costs of not using components specifically designed for the rigors of the space radiation environment.

ANALYSIS METHODOLOGY

An analysis was undertaken by Harris to understand the "hidden costs" satellite systems manufacturers are faced with when making procurement decisions of integrated circuits. Representative mission profiles (from low earth orbit to geosynchronous to deep space) were used. This analysis methodology was discussed with major satellite manufacturers and traditional subcontract component manufacturers as well as industry test laboratories. The costs discussed in this analysis are the averages incurred in the industry to date. Test methodologies varied with the manufacturer's projected missions and the amount of risk a program was willing to accept. Refer to Table 1 (next page) for surveyed average costs.

Upscreening Costs

- The unit cost differential between the space-qualified radiation hardened IC, which is guaranteed to meet all performance parameters over radiation and full space temperature range (-55°C to 125°C), and a non-rad hard IC, designed to function over an industrial temperature range (0°C to 60°C) with no guaranteed radiation performance, is averaged to a factor of 10. (line A)
- It was assumed that a lot consisting of 100 integrated circuits was being procured (line B).
- The survey showed (lines C-E) that in making a procurement decision to use industrial screened ICs, some "upscreening" would be necessary. On a lot-to-lot procurement, an average 5% unit loss occurs in upscreen testing (some loss of units at temperature extremes). The cost of this 100% testing, either internally or by independent test laboratories, was averaged along with the component engineering and the specification costs associated with the upscreening. A conservative figure of 100 man-hours at $100/man-hour was used for upscreen engineering support.

Total Dose Radiation Testing

- The test program cost generation (line F) was averaged for relatively simple ICs to some of today's most complex, small geometry ICs.
- Test fixture design costs (line G) are conservatively averaged with mostly technician costs for board manufacture.
- Included are facilities usage and computer resources associated with actually performing radiation testing (line H). Also, a conservative 8 man-hours at $100/man-hour was included in facilities usage costs.
- An average of 8 samples per lot was used for actual testing (line I). This does not include any assumptions on lots lost failing radiation testing.
- After testing is complete, analysis is performed per part type to ensure its end-of-life performance in the worst case satellite application (line J). Assumptions regarding radiation shadowing internal to spacecraft are made through radiation transport analysis. Again, a conservative 50 man-hours at $100/hour for engineering support is included in derating costs.
- Design approaches to combat predicted performance degradation (line K) varied from various forms of spot shielding through increasing the thickness of component boxes. An averaged cost of $20K/pound was used.

	PROCUREMENT COSTS		SPACE QUALIFIED RAD HARD ICs	INDUSTRIAL NON-RAD HARD ICs
A	UNIT COST (PER DEVICE)		$1,000	$100
B	UNITS PURCHASED	100 (units)	$100,000	$10,000
	BASE PROCUREMENT COST-OF-OWNERSHIP		$100,000	$10,000
	UPSCREEN TEST COST FOR SPACE APPLICATIONS			
C	UNITS LOST	5 (units)	$0	$500
D	COST OF TESTING		$0	$7,500
E	ENGINEERING SUPPORT	100 (man-hours)	$0	$10,000
	UPSCREEN TEST COST-OF-OWNERSHIP		$0	$18,000
	TOTAL DOSE RADIATION TEST COSTS FOR SPACE APPLICATIONS			
F	TEST PROGRAM GENERATION		$0	$20,000
G	TEST FIXTURE MANUFACTURE		$0	$5,000
H	FACILITIES USAGE		$0	$10,000
I	UNITS LOST	8 (units)	$0	$800
J	DERATING GUIDELINES REPORT GENERATION		$0	$10,000
K	SHIELDING COST ($20K/lb)	2 (lbs)	$0	$40,000
	TOTAL DOSE TEST COST-OF-OWNERSHIP		$0	$85,800
	SINGLE EVENT UPSET (SEU) TEST COSTS FOR SPACE APPLICATIONS			
L	SEU TEST PROGRAM		$0	$40,000
M	SEU FIXTURE MANUFACTURE		$0	$20,000
N	SEU FACILITY USAGE		$0	$30,000
O	UNITS LOST	0 (units)	$0	$0
P	EXTRA CIRCUITRY TO COMBAT SEU		$0	$10,600
Q	SEU DESIGN ENGINEERING SUPPORT	100 (man-hours)	$0	$10,000
	SINGLE EVENT UPSET COST-OF-OWNERSHIP		$0	$110,600
	SINGLE EVENT LATCHUP TEST COSTS FOR SPACE APPLICATIONS			
R	TEST PROGRAM GENERATION		$0	$20,000
S	UNITS LOST	5 (units)	$0	$500
T	FACILITIES USAGE		$0	$15,000
U	EXTRA CIRCUITRY TO COMBAT LATCHUP		$0	$2,145
V	ENGINEERING SUPPORT	100 (man-hours)	$0	$10,000
	SINGLE EVENT LATCHUP COST-OF-OWNERSHIP		$0	$47,645
	SINGLE EVENT BURN-OUT COSTS FOR SPACE APPLICATIONS			
W	EXTRA CIRCUITRY TO COMBAT SEU BURN-OUT		$0	$2,145
X	ENGINEERING SUPPORT	100 (man-hours)	$0	$10,000
	SINGLE EVENT BURN-OUT COST-OF-OWNERSHIP		$0	$12,145
	TOTAL COST-OF-OWNERSHIP AT SATELLITE LEVEL		$100,000	$284,190

Table 1
Satellite "cost of ownership" for integrated circuits

Single Event Upset Testing

- The survey showed test program generation for SEU (line L) as more expensive than total dose test programs. This was primarily due to the complexity of the test program (both AC and DC parametrics) along with the analysis cost of test results.
- No additional costs were included if additional proton tests were needed; however, parts exhibiting relatively low Linear Energy Transfer (LET) thresholds may need additional tests.
- Test fixtures for a SEU test (line M) are more expensive than total dose test fixtures because the fixtures have to functionally exercise the parts and count errors during ion bombardment.
- Actual test facility usage (line N) is more costly than total dose facility testing due to the complexity of the equipment used for testing and the technical support needed during testing.
- No actual part-lost cost (line O) was included because engineering development units are usually provided by IC vendors in return for test results.
- Many design approaches to combat SEU effects were mentioned; ping-ponging between redundant memories, master-slave microprocessor schemes and Error Detection and Correction (EDAC) circuitry additions were most common. Circuitry costs for EDAC and additional circuitry overhead for correction software (averaged 4-6 bits) were included (line P).
- Design engineering support (engineers and technicians) is conservatively estimated at 100 man-hours at $100/hour (line Q).
- Latchup test costs as well as burn-out test costs (lines R-X) followed the same general methodology. Units lost for these tests were thought not to be provided by IC vendors. Also, design engineering for burn-out would usually be covered by the latchup design engineering support.

Conclusion

The results of this analysis show the cost-of-ownership in using industrial grade, non-radiation hardened ICs to be approximately three times that of space qualified ICs! This survey was not intended to be all inclusive. Many arguments for and against the use of "industrial" ICs can and will be raised. The intent was to stimulate discussion on a topic facing spacecraft manufacturers today. Pressures to reduce cost, schedule, weight and power consumption continue to drive satellite programs as the technical complexity of satellite functions increases.

As we hinted in Section 2.4, and have quantified here, hardened ICs offer a cost-effective solution that may not be evident to the casual industry observer.

Chuck Tabbert is manager of Customer Engineering in the Harris Semiconductor Military and Aerospace Division (M&AD). A former Air Force officer, Tabbert was the chief of Satellite Survivability for the Navstar Global Positioning System program office. He holds a BSEE from the University of Florida and an MBA from Northrop University (Inglewood, Calif.).

Steve Rivet is the Advanced Digital Product Marketing Manager in Harris Semiconductor's Space Products Operation. He has been employed by Harris since 1983, holding several engineering and management positions. Rivet holds a BSEE from the University of Michigan and an MBA from the Florida Institute of Technology. His publications include contributions to IEEE Transactions on Nuclear Science and several Harris publications, including SPACE PRODUCTS NEWS.

Circuit Design Techniques for Radiation Hardness

By Jack Clark

Designers of radiation hardened integrated circuits face many challenges in the quest to develop the best possible IC design for a given technology. Given the space radiation environment, ICs which are to be flown in space must have the following general characteristics:

- Temperature Range -55° to 125°C
- Total Dose > 300 krad(Si)
- SEU Error Rate < $1X10^{-8}$ errors/bit-day
- Latchup None

Designing integrated circuits to withstand these rigorous environmental requirements (as defined in Sections 2.1 and 2.3) poses a serious challenge to the circuit designer and requires several concurrent elements to be in place to achieve these goals, including:

1) Radiation hardened processes
2) Radiation hardened design techniques
3) Best commercial design techniques

As discussed in previous Sections, the space radiation environment poses radiation threats to ICs which include total accumulated radiation dose and bombardment from highly ionizing particles, giving rise to parameter degradation and single event effects within the individual circuit elements.

RAD HARD CMOS PROCESSES

Total dose radiation changes the threshold voltages of MOS transistors and degrades their ability to conduct current. Radiation hardened processes are designed to minimize changes in transistor operating characteristics. For design purposes, the changes brought about by radiation are added to the normal processing variations in the transistor parametrics to give a worst case estimate of post radiation performance.

Process technology also contributes to the ability of a circuit design to withstand heavy ion hits to the circuit elements. This could include compact resistive and capacitive elements to permit the use of efficient SEU suppression techniques. The process could also employ SOI or SOS wafers to reduce the total amount of sensitive device volume, resulting in minimized charge collection volume and reduced collected charge when a hit occurs.

Significant differences between commercial and hardened CMOS processes are apparent when one reviews typical device parameters for each process. Table 1 (below) outlines several key areas. These factors lead to incrementally larger chip size for equivalent performance.

PARAMETER	COMMERCIAL PROCESSING	RAD HARD PROCESSING
V_{TN}	0.5-0.8V	0.8-1.5V
V_{TP}	0.5-1.0V	0.9-1.4V
$I_{DSN/\mu m}$	370μA/μm	290μA/μm
$I_{DSN/\mu m}$	180μA/μm	150μA/μm
Temp. Range	0° to 70°C, or -20° to 85°C	-55° to 125°C

Table 1
Typical device parameters for commercial and hardened CMOS process

RAD HARD BIPOLAR PROCESSES

Used mostly for continuous-time analog applications, bipolar processes have a different set of sensitivities than MOS processes. Hardened bipolar processes use dielectric isolation (DI) technology to enable the use of complementary devices. Both NPN and PNP devices in these processes are vertical structures, avoiding the lateral PNP device that limits hardness in commercial junction isolated (JI) processes.

Total dose radiation degrades the gain of bipolar devices and increases leakage. Again, these changes are well understood and modeled, and predictable post-radiation performance is assured by

circuit simulations. Bipolar devices are vulnerable to SEU effects, and should not be used for digital devices in space applications. In analog parts, SEU has not been a major issue due to the use of larger geometries, higher power, and DI technologies.

RAD HARD CMOS DESIGN TECHNIQUES

Designing ICs to withstand the rigors of space applications requires the intimate matching of the circuit design to the process parameters. This is the most crucial element in creating a rad hard IC and more often than not makes a circuit unique to its particular process and non-transportable to other processes.

Transistor Ratios

The merging of process and design has major effects on even basic circuit design. The P channel to N channel device width ratios for individual logic elements such as NAND, NOR, and Inverters will be unique to the process. As a simple example, an inverter designed for equal high-to-low and low-to-high switching time might have a P:N width ratio of between 1.5:1 and 2:1 when designed for a typical commercial process. To achieve the same type of performance on some radiation hardened processes, this ratio would increase to between 2:1 and 3:1. Minimum propagation delays are usually found at lower P:N ratios. The same holds true for other types of logic gates. These increased ratios translate into increased gate size.

Output Loading

In digital CMOS circuits, the output of a particular function usually drives the input to another logic element. This driven input is usually the gate terminal of N and P channel transistors, which is primarily capacitive in nature. Note that for an equivalent geometry, a rad hard transistor has only 75-90% of the drive per micron of transistor width (taken over all conditions), while the gate capacitance is nearly the same. Also, the capacitance of the gate terminal is nearly constant over temperature and radiation so that for an equivalently sized gate, the input capacitance seen at the previous stage would be nearly the same for either a commercial or rad hard process.

To maintain equivalent output drive in the rad hard logic element, device widths must be increased by 10 to 25%, resulting in increased die area, lower yields, and increased load at the previous stage. This increased loading requires, in turn, increased drive capability and larger device widths. The net result is an increased design area (by an actual factor of 1.1 to 1.3X) in order for the design to meet an equivalent speed requirement over all possible conditions of process, voltage, temperature, and radiation degradation.

Gate Complexity

Many commercial circuits employ clocked dynamic logic to substantially reduce transistor count, improve speed, and lower overall operating power. These benefits come at the expense of static operation (low-to-zero clock frequencies) and standby power (dynamic circuits must always be clocked). Radiation poses an additional constraint on the use of dynamic logic due to post-radiation leakage currents and heavy ion hits, both of which remove charges from the dynamic nodes and can result in possible circuit failure. Therefore, clocked dynamic logic is not suitable for radiation environments.

Multi-input logic functions, such as NAND or NOR structures, result in the stacking (series hookup) of transistors to achieve the desired function. To achieve a high level of packing density, these stacked transistors are usually placed within a common silicon island or body well to facilitate a common transistor body tie. Transistor design for good switching characteristics will have the transistor body tied to the same potential as the source terminal; this permits the greatest device drive and fastest operation.

In a stacked structure (refer to Figure 1, next page) with one side of the stack tied to a power supply, only the device connected to the supply maintains this body-source tie. The remaining transistors in the stack have their sources tied to the adjacent transistor's drain terminal.

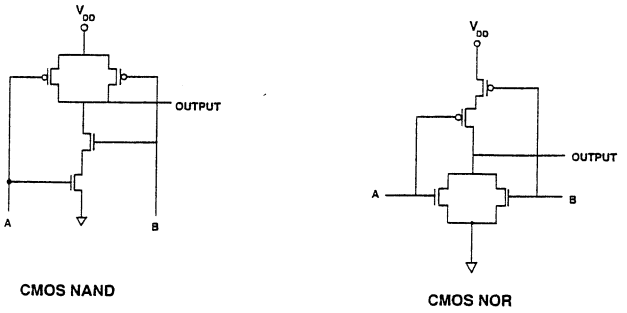


Figure 1
Stacked transistor structures

During switching of the output of this stacked structure, the devices conduct current, resulting in a momentary voltage drop across each transistor in the stack. These voltage drops add together; the transistor furthest from the supply will experience a higher than normal source voltage due to the sum of the voltage drops on the other devices in the stack. When the source voltage of a device becomes greater than the body voltage, a phenomenon known as "body effect" occurs, where the threshold of the device actually increases at the same time the gate-to-source voltage is decreasing.

This body effect is much more pronounced in most radiation hardened processes due to a variety of factors. The net effect is that a rad hard circuit designer must limit the number of transistors in a stack to between 3 and 4 while a commercial design could utilize as many as 7 to 9 devices before experiencing the same performance degradation. Thus, more stages of logic are required to yield the same function, resulting in increased chip area.

Transmission Gates

When signals must be passed from one point to the next on a common line or when signal flow is bi-directional, circuit designers often employ a transmission gate or T-gate. T-gates can be used in multiplexers, PLAs, decoders, and latches. They can be either a single transistor or a pair of complementary P and N devices plus an inverter to control the gate voltage of the second transistor. The single device can switch signals well for one transition (1 to 0, for instance) and poorly in the other. By poorly, it is meant that the device will not provide a full level logic swing of the output signal but will pull only to within a threshold voltage of the desired full logic voltage level. The full CMOS version works well for both signal transitions but has the disadvantage of increased area needed for the additional transistors.

For rad hard design, the stacking rule applies to cascaded T-gates for the same reasons as stacked transistors in logic gates. Generally, where performance matters, a full CMOS T-gate is employed to reduce propagation delays and eliminate leakage concerns from stages downstream of the signal path at the expense of increased chip area.

Special Memory Considerations

In computing applications for spacecraft, there is a need for large quantities of radiation hardened memory which can resist SEU and exposure to radiation. Radiation hardened memories must employ design techniques which are incompatible with minimization of layout area. Typical commercial SRAM designs utilize a very compact 4 transistor/2 resistor memory cell which is extremely SEU prone. To address the SEU issue, rad hard SRAM designs use a 6 transistor memory cell with additional passive components for hardening the cell to resist SEU. This generally results in a cell size which is 2 to 4X larger than the commercial equivalent. As the cell array area comprises approximately 75% of the total chip area, most radiation hardened SRAMs are at least 2X the chip area of commercial static devices.

RAD HARD ANALOG DESIGN TECHNIQUES

The design of hardened analog parts depends heavily on accurate models and good simulation fidelity. A good design cycle starts with a detailed assessment of model parameters, including pre- and post-radiation values. Device degradation by total dose leads to reduction of amplifier open loop gain and increases in critical input parameters such as offset voltage and bias current. To counteract such gain degradation, the basic circuit architecture of the op amp can be modified to include multiple gain stages and cascaded device (Darlington) output stages; a single gain stage will generally not provide sufficient current gain after irradiation. Such "multistage" approaches lead to more difficult compensation and stability considerations because the phase shifts of more transistors must be considered.

Shifts in input bias current can be minimized by the use of input current cancellation circuitry, with a moderate increase in complexity. Shifts in offset voltage, however, are not so easily handled; these are not shifts in average offset voltage, but rather a broadening of the pre-rad distribution of this parameter. By moving to a hardened analog CMOS process, input offsets can be nearly eliminated by use of autozero techniques. Harris' HS-9008RH 8-bit flash A/D converter uses this approach.

A/D conversion in a radiation environment presents its own set of challenges. In successive approximation devices, careful design of the critical comparator, DAC and voltage reference subcircuits is necessary, while in flash converters, control of post-radiation comparator offset is required.

BEST COMMERCIAL PRACTICES

In addition to many of the rad hard design considerations discussed above, many of the best design and layout techniques from the commercial world can be adapted and used for rad hard applications. Low noise output buffers to minimize system ground bounce, ESD structures to preclude damage from electrostatic charges, advanced designs for high speed static SRAMs, and general sound layout practices with regards to current density, power routing, and bussing schemes are all utilized for best results within the constraints of the specific design and layout rules for the rad hard process employed.

CONCLUSION

Following the design techniques outlined in this Section represents significant extra design effort. The end result, however, will be a radiation hardened integrated circuit which will approach the performance of the equivalent commercial part and have a layout that is between 1.7 and 4 times larger in overall die area.

Jack Clark is a design engineer in Harris Semiconductor's Military and Aerospace Division (M&AD). He has designed several radiation hardened SRAMs in SOI technologies, including the RHD-1 256K SOI SRAM. Prior to joining M&AD, Clark worked in the Commercial Products Division (currently called SPD) of Harris Semiconductor, where he was responsible for the design of several commercial high speed SRAMs. Clark holds a BS in Electrical Engineering from the University of South Florida and an MSEE from the Florida Institute of Technology. He holds two patents on circuit design techniques and has co-authored eight technical papers on rad hard circuit design.

Radiation Hardened Technology at Harris

By Nick vanVonno

In this Section we will discuss some key aspects of radiation hardened silicon process technology at Harris Semiconductor. The emphasis will be on passive isolation processes; these are a historical Harris strength and are of strong current interest to the hardened electronics community. As we will cover in more detail, the passive isolation MOS technology provides important advantages in single event upset (SEU) vulnerability reduction. Also covered will be bulk CMOS technologies, including processes optimized for cryogenic applications.

PASSIVE ISOLATION FOR SEU RESISTANCE

The understanding of radiation effects in space has evolved dramatically since the first discoveries of radiation belts and their effects on semiconductor electronics. Much early effort centered on total gamma dose and the hardening of MOS processes against these environments. This was followed by better understanding of single event upset (SEU) phenomena, first noted in the mid-seventies. The process advancements that had provided improved total dose resistance did not apply to this new threat environment, however. An early result of SEU research was the elimination of most bipolar technologies for hardened memory applications. Later, improved bulk CMOS memory design techniques were able to significantly enhance SEU hardness.

Examination of the basic mechanisms behind SEU phenomena provides guidance in technology choices. The basic effect is caused by energetic ions from cosmic rays and solar flares penetrating sensitive areas of integrated circuits. (Refer to Section 2.3 for a more complete description of single event effects.) These ions deposit significant charge in the semiconductor bulk along the ion track. This charge can upset memory cells or digital gates by changing the voltage on critical circuit nodes. The amount of charge is a function of the ion track length and also of the lifetime in the material. The first of these variables provides an important technology clue; if the MOS transistor used can be made as thin as possible, the effective ion track length and the charge deposited are both minimized. This leads to silicon on insulator (SOI) technology, or passive isolation technology in general, in which a transistor's active volume can be bounded and minimized. Figure 1 (below) compares cross sections of both bulk and SOI technologies (in this case, the silicon on sapphire [SOS] implementation) and clearly shows the reduction in device volume.

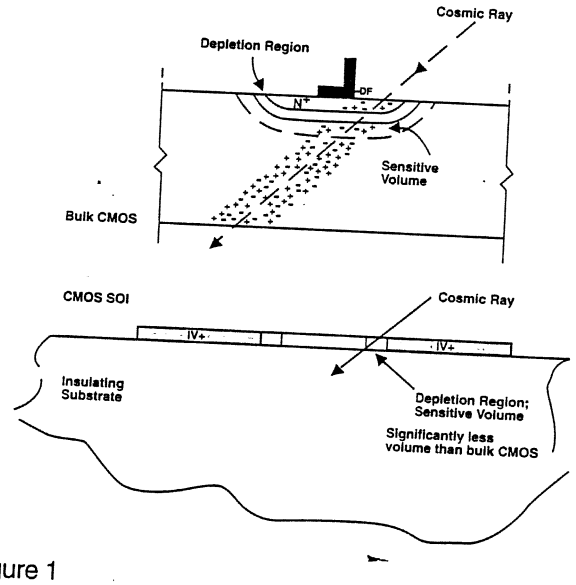


Figure 1
Sensitive volumes in bulk and SOI systems

The use of SOI technologies in itself is nothing really new. Dielectrically-isolated bipolar technology has been used in hardened applications for nearly thirty years. These processes use V-grooving and oxidation of a starting substrate followed by thick polysilicon growth on the oxide. The original substrate is then largely ground away, resulting in oxide-isolated single-crystal regions in a polysilicon matrix. This technology is well-suited to thicker devices (in the 10-20 micron range), as used in bipolar processes. It is not well suited to thinner devices, although Harris has produced photodi-

odes in single-poly DI with 5 micron island depth on a limited basis. Note that this DI bipolar technology does not improve SEU vulnerability to a great extent since the DI regions are to the order of 25-30 microns thick.

A second early SOI technology that is also still widely used is silicon on sapphire (SOS). This interesting heterostructure is formed by growing an epitaxial silicon layer on single-crystal sapphire (Al_2O_3). The sapphire is grown using edge-fed growth (EFG) technology, in which a single-crystal sapphire ribbon is pulled from a melt. The ribbon is ground and cut into wafers, which are then polished. Sapphire has a hexagonal crystal structure, hence the silicon epitaxy has a lattice mismatch of a few percent because silicon has a face-centered cubic (FCC) structure. This mismatch results in a strained Si film with a very low minority carrier lifetime, on the order of a few nanoseconds. SOS technology uses Si films of 400-600 nm which are selectively etched into individual islands for each transistor. A standard CMOS process sequence follows. The resulting MOS device is thin and has minimal lifetime, both ideal for improved SEU resistance. Harris' TSOS-4 process is in current production using 1.2 micron minimum geometries. Applications of this process center around random-access memory such as the Harris HS-65643RH 64Kx1 static RAM and logic families such as Harris' ACS device types. Figure 2 shows a cross-section of the SOS technology. Also shown in this figure are the three distinct devices created in any thin-film-on-insulator process: the top, bottom, and side transistors. Each one of these areas requires specific process and design techniques in order to produce a radiation hardened product. SOS provides the highest SEU resistance of present technologies, driven by the relatively low lifetime as compared to the SOI technologies we will discuss next.

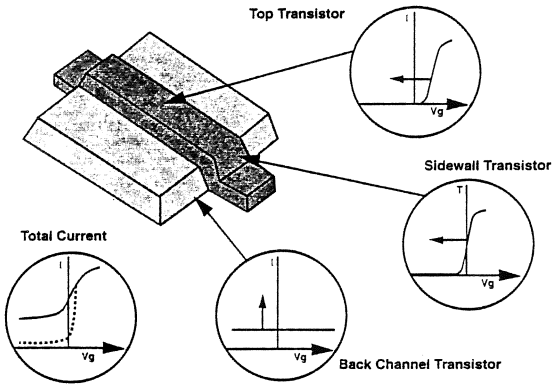


Figure 2
CMOS/SOS technology

The latest silicon on insulator (SOI) technology uses SiO_2 as the insulator and has been under intensive development since the early 1980s. The predominant materials technology is "Separation by IMplantation of OXygen", fortunately abbreviated to SIMOX. This process uses a high-energy implantation (on the order of 200 KeV) of oxygen into a starting silicon substrate. An oxygen-rich layer is thus created, usually 200-300 nm below the surface. A high-temperature anneal is then used to create a stoichiometrically correct layer of SiO_2, resulting in a single-crystal silicon layer on a nominally 300 nm oxide layer. Processing then proceeds through a local oxidation for lateral isolation or a trench/refill operation, followed by a normal CMOS processing sequence. Figure 3 shows a cross-section of this technology.

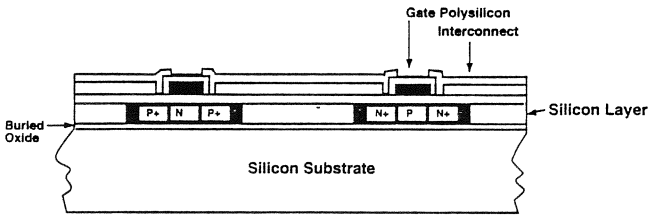


Figure 3
Silicon on insulator (SOI) technology

Applications of SOI technology using SiO_2 at Harris include the HS-65758RH 256K static random-access memory device. This part is currently in production with full qualification planned for the end of 1993. Harris has also introduced two gate arrays in SOI, with further expansion planned. The first array has 125,000 total gates (HGA6125RH), with up to 50,000 usable gates and up to 272 usable I/O's. The second member is a 197,000 gate array (the HGA6197RH), with approximately 78,000 usable gates and up to 340 I/O's. The arrays are designed for use in space and strategic applications requiring high gate count, high speed performance, and superior radiation performance. Expansion into three-layer metallization, planned for 1994, will increase usable gate counts into the 125,000 range. Finally, hardened equivalents to the Xilinx XC3020 and XC3090 field programmable gate arrays are presently in development. SOI applications at Harris use the 0.8 micron RHD-1 process, which is now in qualification.

While SIMOX is the leading technology for SOI fabrication, alternatives are under active development, driven mostly by SIMOX material costs. The alternative method of current interest at Harris uses bond/etch back technology. Two oxidized wafers are heated in an appropriate ambient, causing the oxide layers to bond together chemically. One of the wafers is then thinned by grinding and polishing, again resulting in a thin film on oxide. This method, now in production at Harris, is used to fabricate Harris' commercial UHF-1 high-frequency bipolar process. It is well adapted to low-cost processing and large wafer size, especially in bipolar technology. The use of implanted etch stops and electrochemical etching can extend the method to thin-film SOI structures suitable for CMOS processing.

As described in this brief overview, SOI processing has advanced significantly over the past decade, propelled by increased emphasis on SEU resistant digital electronics. Well-publicized SEU difficulties on Hubble, Magellan, and many other missions have resulted in stringent SEU specifications on new systems; present SOI technologies provide the semiconductor processes that can meet these specifications. Harris has participated in this area since its pioneering development of single-poly DI in 1963, and continues this participation with aggressive efforts in SOI and SOS technologies. Figure 4 shows Harris' history in SOI and SOS production, starting with early metal-gate SOS

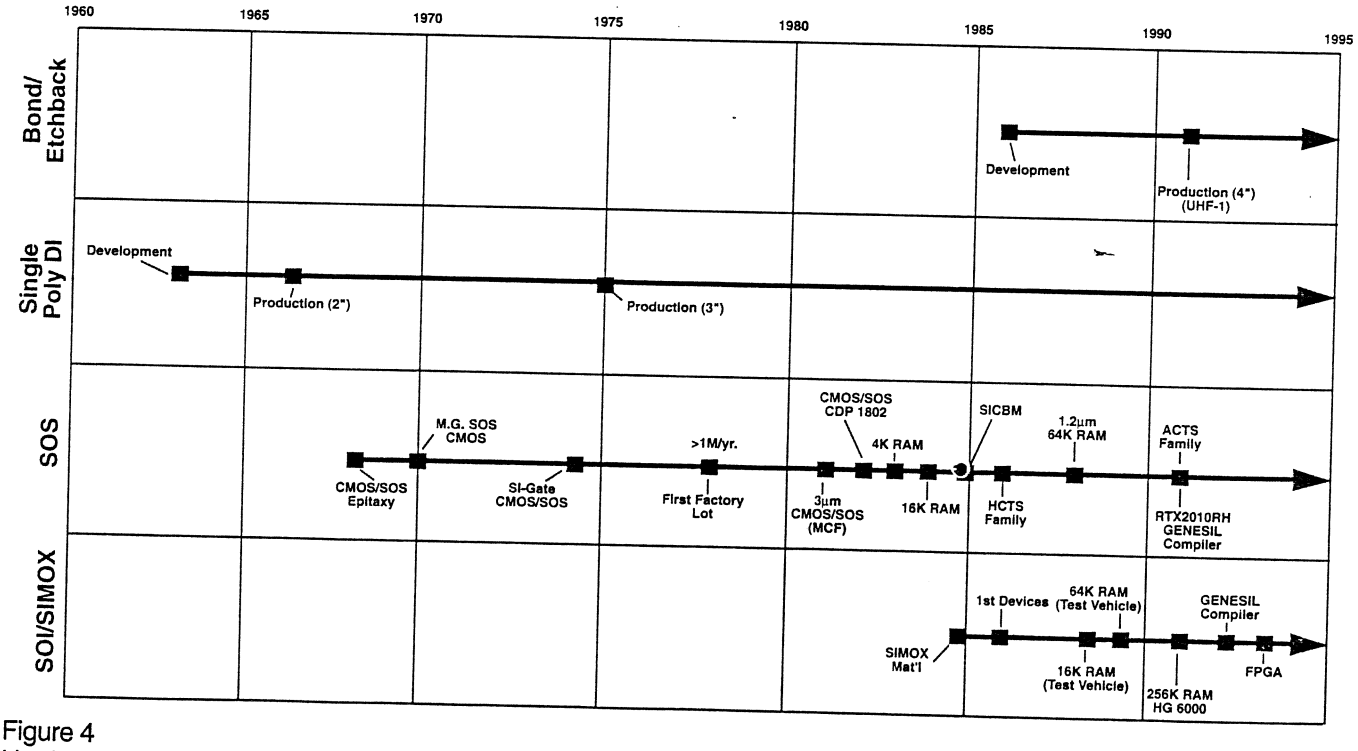


Figure 4
Harris' long history in the production of radiation hardened SOS/SOI circuits

efforts and culminating in current production in both technologies.

BULK HARDENED CMOS TECHNOLOGIES

For hardened applications that do not require very low levels of SEU vulnerability, bulk CMOS processes provide a cost-effective solution. These applications include analog and mixed-signal devices in which SEU is not as critical an effect.

The Harris AVLSI family of bulk CMOS processes is radiation hardened to high levels of total dose radiation. It uses 1.2 micron minimum design rules and features two levels of interconnect. An analog option introduces a metal/nitride/metal capacitor using molybdenum top and bottom plates; this enables the design of precision switched-capacitor functions due to the low temperature and voltage coefficients of this structure. Current Harris products include the HS-26C31/32 line driver/receiver set and the HS-9008RH 8-bit flash A/D converter.

A second radiation hardened bulk CMOS process is optimized for cryogenic signal processing applications in the 40K-77K range. The RHC-40 process is currently in development at Harris and is based on the earlier LN77 process. These processes use modified counterdope implants, low-noise hardened gate oxides or oxynitrides, and heavily doped N-channel guard rings to provide total dose hardness in the 200 krad(Si) to 1 Mrad(Si) range. Applications include on-focal plane signal processing and A/D conversion and large readout cell arrays for direct hybridization of staring focal plane arrays. Emphasis here has been on extreme low-power operation and complex mixed-signal functions.

CONCLUSION

As this Section has outlined, Harris has developed several different process technologies to provide the levels of hardness necessary for the harsh environments in which modern electronic systems operate.

Nick vanVonno presently heads a design and development organization involved in radiation hardened digital and analog circuits in Harris Semiconductor's Military and Aerospace Division. Recent interests include cryogenic CMOS process development and the application of these processes to on-focal plane signal processing. van Vonno holds a BSEE from the University of Florida. He has authored numerous papers on radiation hardened processing and design, receiving Best Paper award at the 1976 Government Microcircuit Applications Conference. He has been actively involved with the IEEE Nuclear and Space Radiation Effects Conference in capacities of session chairman, Guest Editor and Awards Chairman. vanVonno holds eight patents in the areas of high speed logic, laser trimming techniques and packaging technology.

Quality Assurance in Product Development

By Bill Schultz

Reliability is a critical and often limiting factor in both manned and unmanned space systems. It is a major factor that has distinguished Harris Semiconductor as a leader in the design and manufacture of high reliability radiation hardened integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable high reliability process technology and product design (discussed in the two previous Sections). It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

CONTROLLING AND IMPROVING THE MANUFACTURING PROCESS

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in process steps and raw materials used in production. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicate a trend toward the limit. These same control charts are powerful tools for continuous improvement by reducing variations in processing, materials, and products.

SPC is important, but is only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. Harris engineers use Design of Experiments (DOX) methodology, a scientifically disciplined mechanism for evaluating and implementing improvements to assure that requirements are met. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process and optimizing the procedures or design to yield the best result.

PROCESS QUALIFICATION

One of a product development team's objectives is to move the reliability assessment to an earlier point in the development cycle. Harris' qualification sequence focuses on the early stages of the process development. Initial work transfers a set of standardized test vehicles to the new process using the process layout ground rules. Combined with standard wafer acceptance structures, these test vehicles are placed on a mask set for the early reliability assessment of wearout failure mechanisms. Test vehicles usually contain specialized structures that actually violate ground rule limits in order to establish process margins.

With this mask set, reliability evaluation can be performed concurrently with process development. When a unit process such as interlevel or gate dielectrics or metallization levels has completed development (usually before the entire process sequence has been performed), reliability assessment can be initiated for time-dependent dielectric breakdown and metal electromigration. Feedback to the process development function during this phase contributes significantly to first-pass success and reduction of development cycle times. Product qualification now becomes a verification that earlier work using test vehicles has defined and eliminated all failure mechanisms.

Device end-of-life mortality, known as wearout, is an accepted concept in semiconductor manufacture and is graphically depicted by the increasing failure rate segment of the bathtub curve in Figure 1.

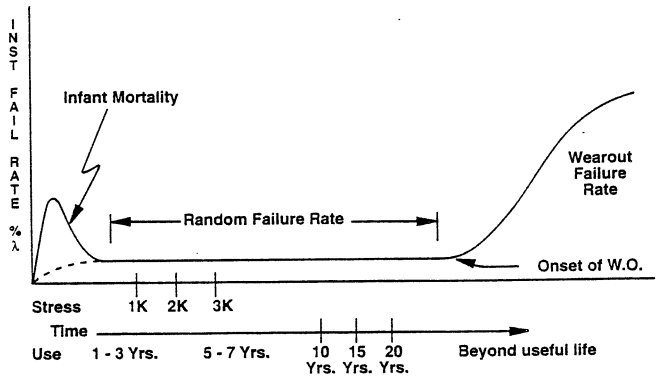


Figure 1
Reliability failure rate "Bath Tub Curve"

The mission of the process reliability group is to insure that the onset of wearout occurs at a time beyond the customer's projected use. The actions taken to fulfill this goal simultaneously improve all phases of a product's life cycle, from a decline in infant mortality and early life defect related failures to a reduction in midlife failure rates, and finally a postponement of wearout. Process reliability engineers focus their attention on wearout prevention early in the process development cycle. In particular, new unit processes, tools and fab line modifications, and material and structural changes are all assessed from a reliability standpoint. Appropriate tests are instituted as necessary for this assessment.

Wearout characterization is focused on those failure mechanisms common to ICs. An adaptable approach allows additional mechanisms unique to a given technology to be studied as necessary. Investigations are performed using the mask set of special test structures modified and fabricated for the process being studied. This permits highly accelerated testing and extrapolation to customer use conditions.

Present test vehicles at Harris consist of a standard 96-structure set that is continuously updated as improvements are defined. Failure mechanisms defined by these structures have been baselined and fitted to appropriate models, with the following wearout mechanisms investigated:

Electromigration-30 test structures are available to characterize metal electromigration. Data gathered at several accelerated temperatures and current densities are used with Black's equation, $MTF=AJ^{N}\exp[E_a/kT]$[1], to generate current density ground rules for the new process. A 1% cumulative failure rate over 10 years at a junction temperature of 175°C is used as a qualification limit.

Hot Electron Effects-Hot electron effects are studied by stressing MOS transistors at maximum substrate current for 1,000 hours. This mechanism, of major interest in high-density processes, is modeled based on work by Hu, et al. [2,3] using limits of 10mV threshold voltage shift or 10% transconductance degradation, depending on circuit application.

Time Dependent Dielectric Breakdown (TDDB)-Elevated voltages are used to accelerate gate oxide breakdown and provide data for determining the lifetime at use conditions according to available models (Crook, Hu. et al.) [4,5]. The final gate oxide recipe is required to have less than a 1% cumulative failure rate over 10 years at a junction temperature of 175°C.

Interlevel Dielectric Failure-Large area capacitors are constructed utilizing all process dielectrics. Breakdown voltages are required to significantly exceed the maximum specified voltages for the process and to be tightly distributed around the intrinsic limit for the given dielectric thickness.

Device Stability-A large number of transistors are subjected to excess gate voltage at high temperature (175°C) for 336 hours. A failure criterion is chosen in accordance with the nature of the process. The number of devices failing to meet this criterion must be sufficiently low to prove < 100 FITs (1 FIT = 1 failure in 10^9 device hours) at 55°C.

Stress Induced Voiding-Either long metal meander structures or a product die with sufficiently long metal lines are stressed at high temperature (180°C) without bias for up to 3,000 hours to induce metal migration and the formation of voids. The final process flow must have no failures due to this stress.

All of the wearout studies described above are conducted on devices from multiple wafers from numerous process lots. Results establishing insufficient lifetime or large defect population are com-

municated to the process development team for immediate investigation and correction. Properly designed experiments are used to modify the process or eliminate the reliability concerns. DOXs conducted on subprocess flows provide faster turn-around time and more efficient use of resources than running full process flows. The results define the critical process control variables that need to be monitored to ensure that reliability is built into the new process. Wearout testing thus provides the data for defining the critical process nodes and design for reliability through improvements to layout groundrules. A successful new process requires attaining all of reliability's wearout criteria.

When the process wearout characterization is complete and the first product types are fabricated, the next element of the process qualification is a thorough construction analysis, or Destructive Physical Analysis (DPA). This analysis entails a SEM (Scanning Electron Microscope) survey of the product topography, using MIL-STD-883 Method 2018, with particular emphasis on interconnect step coverage in the context of layout stacking rules. Die cross sections are also performed as a part of DPA, enabling direct evaluation of diffusions, oxidations, and thin films. The sample size for this characterization is the same as for wearout, that is, 3 wafer lots, 5 wafers per lot, and 5 die locations per wafer.

As a final phase of process qualification, initial product types in hermetic packages must successfully complete a series of operating life and environmental stress tests. Depending upon product type, these will include static and dynamic life at 150°C for 3,000 hours using sufficient samples to enable a predicted maximum failure rate of 100 FITs at 55°C with 95% confidence and storage life at 180°C, also for 3,000 hours with no failures allowed. Environmental tests include high temperature operating life (HTOL), temperature cycle and thermal shock. A summary of process testing is provided in Table 1 (page 3.3-4).

It is important to note that the reliability qualification standards as defined are designed to insure the following:

- The process qualified is the production process, and no engineering lots or lots from a pilot line may be defined as a product qualification.
- The lot sampling requirements insure that the qualification will represent the process variability.
- Durations of the stress tests are extended well into the useful life. Qualification decisions can be made as early as 1,000 hours.
- Extensive failure analysis is performed on all failures that occur during qualification. This is a team effort which includes Process Development, Design, and Product Engineering functions. Where failures are identified to be caused by processing/design/package deficiencies, changes are implemented by the qualification team and re-qualification/verification testing is performed to insure that the product and process will meet the reliability standards and the specific customer expectations.

ISO9000

In keeping with Harris' tradition of providing the most reliable circuits available and satisfying the requirements of our customers, Harris has made a commitment to become ISO9000 certified at all plant sites worldwide. The International Standards Organization (ISO)–9000 certification process, which has been created within and underwritten by the European Economic Community, is an outstanding process for examining a company's quality systems. It provides manufacturers and their customers a unified measure to baseline and improve operating systems. ISO9000 is total quality management (TQM) based, and is quickly becoming an audit standard by which customers will measure their supplier's ability to be a supplier of high quality, reliable semiconductors. To date,

Test/Conditions	Minimum Duration	Sample Size	Acceptance Criteria (A=x)
High Temperature Operating Life (HTOL) Static & dynamic V_{DD} = Max operating • Hermetic T_A=150° C (where V_{DD}=supply voltage and T_A=temperature ambient)	3,000 hours	400 cum 5 lots	≤1% PDA ≤ 100 FITs @ 55° C,95% CI
Temperature cycle • -65° C to +150° C MIL-STD-883 Method 1010 (Hermetic)	1,000 cycles	153 cum	A = 0
Thermal Shock MIL-STD-883 Method 1011 • Condition C -65° C to +150° C (Hermetic)	1,000 cycles	153 cum 3 lots	A = 2
Storage Life T_A =180° C No Bias Hermetic Frit Seal	3,000 hours	153 cum 3 lots	A = 0
Storage Life T_A=150° C No Bias	1,000 hours	90 cum 3 lots	A = 0

Table 1
New process qualification product type testing

three Harris Semiconductor manufacturing sites have attained certification status:

- Dundalk, Ireland
  1989 ISO9001 Certification (Certification when a contract between two parties requires the demonstration of a supplier's capability to design, produce, install, and service a product)
- Singapore Assembly/Test
  May, 1993 ISO9002 Certification (Certification for quality assurance in production and installation)
- Kuala Lumpur, Malaysia Assembly/Test
  May 1993 ISO9002 Certification

All domestic Harris Semiconductor sites are in the process of obtaining certification, with Palm Bay, Florida and Mountaintop, Pennsylvania targeted for June 1994 and Findlay, Ohio for December 1994. Det Norske Veritas (DNV) has been selected as the certifying agent for North America.

CONCLUSION

Semiconductors are the backbone of most of today's high-tech systems for commercial, industrial, and defense applications. Harris has been involved in understanding the effects of radiation on semiconductors since 1962, when its predecessor, Radiation Inc., was asked to develop highly reliable custom devices. We have a very long lineage of high reliability, high performance products that have resulted from our continued commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications.

SPC, DOX, and design for manufacturability and reliability combine in a product development system that delivers the quality and reliability performance demanded for today and for the future.

REFERENCES

[1] J.R. Black, "Electromigration Failure Models in Aluminum Metallization for Semiconductor Devices", *IEEE Transactions on Nuclear Science*, Vol. 57, No. 9, September 1969.

[2] C.Hu, et.al., "Hot-Electron-Induced MOSFET Degradation - Model, Monitor, and Improvement", *Transactions on Electron Devices*, Vol. Ed-32, No. 2, February 1985.

[3] E.Takeda and N.Suzuki, "An Empirical Model for Device Degradation Due to Hot Carrier Injection", *IEEE Electron Device Letters*, Vol. EDL 4, No. 4, April 1983.

[4] D.L.Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", *International Reliability Physics Symposium*, 1979, pp. 1-7.

[5] J.C.Lee, Ih-Chin Chen, and C.Hu, "Modeling and Characterization of Gate Oxide Reliability", *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, December 1988, pp. 2268-2277.

Bill Schultz is the Director of Reliability Engineering for Harris Semiconductor Sector. This responsibility includes worldwide IC product and package qualifications, customer product return services, failure analysis and analytical lab support. Prior to joining the Reliability organization, Schultz worked in Product Engineering and was responsible for CMOS SRAMs and yield enhancement. Schultz served in the U.S. Navy, and holds a BS degree in Electrical Engineering from the University of Florida.

GLOSSARY OF TERMS

Alpha Particles - The nucleus of a helium atom; double ionized (two electrons removed) helium. The lightest and most common "heavy ion". A small percentage constituent of the solar wind.

Bremsstrahlung Radiation - Literally, "braking radiation". Usually refers to the X-rays created when Van Allen electrons slow down in spacecraft structural material, box covers and shielding, etc.

Bulk CMOS - Junction isolated CMOS. This technology is particularly susceptible to single event upset (SEU) when small device geometries are employed. If an optimized epitaxial layer thickness is not used, this technology can also be very susceptible to latchup due to electrical transients or SEL.

Control Charts - A statistical tool used to monitor the performance of equipment, personnel, or processes. Usually used to define machine or process capabilities, this information is fed back into the product design cycle to improve manufacturability of the product.

Cosmic Rays - High energy heavy ions. Originate in violent stellar reactions outside the solar system.

Dielectric Isolation (DI) - A technique (invented by Harris) to obtain a very robust passive isolation layer between an IC's transistors. A very mature process technology, it still dominates over other technologies in sheer number of bipolar analog circuits fabricated on it. Circuits produced on DI processes have excellent single event effect (SEE) immunity and are electrically rugged.

Electrons - The electrically negative subatomic particle. An electron's charge is equal and opposite to that of a proton. Electrons orbit an atom's nucleus in quantized energy states; if they are energetic enough to escape an atom, they move under the influence of an electric field and produce electrical current. Electrons are emitted by the Sun (they are a main constituent of the solar wind) and are concentrated in the Van Allen belts.

Epitaxial Layer - A thin, single crystal layer of material grown over an existing single crystal material structure. This technique is used to grow a lightly doped silicon layer (doping optimized for transistor performance) over a heavily doped silicon wafer (doping optimized for low resistance). A wafer fabricated in this manner has lower parasitic substrate resistances than a non epitaxial wafer with low doping levels, but retains the transistor performance of the lightly doped wafer. The effect of the lower substrate resistance is to significantly reduce the susceptibility to latchup of circuits built on the epitaxial material.

Exoatmospheric - Outside the Earth's atmosphere.

Field Programmable Gate Arrays (FPGA) - A flexible architecture for implementing complex logic functions into a single programmable circuit. The architecture was pioneered by Xilinx Corp. and is being implemented in a high performance submicron radiation hardened process by Harris. These circuits function as user configurable gate arrays, using the SEU-proof RHD1 memory cell with Miller capacitors as the logic configuration storage element. Unlimited configuration cycles with no performance degradation make these devices attractive for use in system development, and can vastly reduce the need for long lead time, high risk ASICs.

Fluence - Number of particles, photons, etc. passing through a unit area.

Flux - Number of particles, photons, etc. through a unit area in a unit time.

Geomagnetic Shielding - An effect of the Earth's magnetic field on charged particles. Charged particles are deflected along magnetic lines of force; this prevents most low energy particles from penetrating to low altitudes at low latitudes, effectively shielding these regions from most space radiation.

Inclination - Angular displacement with respect to the equator. An equatorial orbit, for example, has an inclination of 0°, while a polar orbit has an inclination of 90°.

Ionization - Imparting enough energy to an electron to free it from its parent atom; the creation of an electron-hole pair. Ionization in a material will significantly increase its electrical conductivity; insulator and semiconductor junction performance degrade under the influence of ionization.

Ionizing Radiation - Radiation, particles or photons, that produces ionization in a target material. The types of ionizing radiation most important to designers of space electronics systems are electron, protons, Bremsstrahlung radiation, and cosmic rays; each of these radiation types can have significant negative effects on IC operation.

Kinetic Energy - Mechanical energy; energy due to velocity. Equal to one half of a body's mass times its velocity squared.

Magnetopause - The edge of the influence of the Earth's magnetic field on the interplanetary particle environment.

Magnetosphere - The region of influence of the Earth's magnetic field. The magnetosphere surrounds the Earth on all sides; it is compressed on the daylit side of the Earth and stretched outward (for several hundred Earth radii or more) on the night side.

Mobility - Refers to the ease with which a carrier (hole or electron) can move in a given material.

Neutrons - A subatomic particle found in the nucleus of atoms. Low energy neutrons are generated by the Sun and form a minor part of the solar wind. These particles do not become trapped in the Van Allen belts (no charge, therefore no magnetic deflection) and do not contribute significantly to the near Earth or interplanetary particle environments. Higher energy neutrons generated by cosmic ray interactions with the upper atmosphere have been shown to cause SEU in avionics.

Nova - The explosion of a small to medium size star that occurs when the star has exhausted its nuclear fuel. A very small percentage of the star's mass is ejected as high energy ions (predominately H^+ and He^{++}, but also includes ions up through iron).

Nucleus - The central structure of an atom containing the neutrons and protons. Its charge is electrcally positive. A high kinetic energy nucleus is a cosmic ray.

Parasitic Devices - Unintended or unwanted passive or active electrical components present in an IC fabrication process; devices that are a by-product of process design. The SCR responsible for latchup in bulk CMOS processes is a parasitic device.

Passive Isolation - General category of IC processes that isolate transistors by means of a layer of passive (insulating) material rather than a reverse biased PN junction. DI, SOS, and SIMOX are three different passive isolation fabrication technologies produced at Harris.

Photon - The smallest quantum of electromagnetic energy. Electromagnetic energy includes radio waves, microwaves, infrared light, visible light, X-rays and gamma rays; each of these types of radiation is a stream of photons of differing wavelengths and energies. Photon wavelengths are inversely proportional to energy.

Plasma - A collection of high energy subatomic particles; dissociated atoms.

Plasmasphere - The region of the Earth's magnetosphere containing high charged particle concentrations.

Proton - The subatomic particle with a positive charge; resides in the nucleus of the atom. Free protons are a significant constituent of the solar wind. Trapped in large numbers in the Van Allen belts.

Radiation - The transfer of energy in the form of particles or photons; alpha particles and gamma rays from nuclear decay are examples of ionizing radiation. Visible and infrared light and radio waves are examples of non-ionizing radiation.

Sensitive Device Volume - The portion of a transistor in an IC that contributes to the collection of charge from a single event.

Shewhart Control Charts - A particular type of control chart used in Harris' IC manufacturing processes.

Silicon Controlled Rectifier (SCR) - A four layer PNPN semiconductor device. It exhibits a very high resistance to the flow of electrical current until triggered. The triggering of parasitic SCRs is responsible for latchup in bulk IC fabrication technologies.

Silicon On Insulator (SOI) - A silicon IC fabrication process in which transistors are isolated from one another by an insulating material.

Silicon On Sapphire (SOS) - An example of an SOI process. A thin epitaxial layer of silicon is grown on a sapphire wafer. Silicon between transistors is etched away leaving isolated islands of silicon on the insulating sapphire substrate. This technology is capable of extreme levels of SEE and total dose hardness.

SIMOX - Separation by IMplanted OXygen. Another example of an SOI process. In this technology a high energy oxygen implant is made into a silicon wafer; a layer of oxygen ions forms below the silicon surface. After the implantation, the wafers are heated to a high temperature. The implanted oxygen forms a stoichiometrically correct layer of silicon dioxide, and the damage to the top silicon layer is annealed. The silicon layer between transistors is etched away leaving isolated silicon islands on an insulating silicon dioxide layer. This technology is capable of extreme SEE and total dose hardness.

Single Event - The passage of a single highly energetic heavy ion through an IC that results in some negative impact on the IC's operation.

Single Event Burnout (SEB) - Burnout of an IC due to a single event induced latchup.

Single Event Effects (SEE) - Any of the effects of single events on an IC or discrete device. Includes SEB, SEGR, SEL, and SEU.

Single Event Gate Rupture (SEGR) - Permanant damage to a power MOS transistor due to a single event. As an energetic heavy ion penetrates the gate of the transistor, an ionized trail is left in the oxide. The collection of this charge and avalanche multiplication of the deposited charge results in localized heating severe enough to damage the gate, permanantly disrupting device operation.

Single Event Latchup (SEL) - Activation of the parasitic SCR structure in junction isolated IC processes due to a single event.

Single Event Upsets (SEU) - Change in the state of a logic storage element (e.g. RAM cell or flip flop) due to a single event.

Shielding - Minimizing the radiation threat to a component by putting material between the radiation threat and the component. Can be used to somewhat reduce the total dose threat a component receives, but is not practical in use against single events.

Solar Wind - The stream of particles emitted by the Sun that flows out in all directions. The solar wind is the primary source of particles that become trapped in the Van Allen belts.

Spectrum - The full range of energies associated with photons or particles.

Supernova - The explosion of a large star when it has exhausted its nuclear fuel. A large percentage of the star's mass is ejected as high energy ions (predominately H+ and He++, but also includes all the naturally occuring elements).

Total Dose - The total amount of ionizing radiation a target receives; dose rate integrated over time. Also commonly called total ionizing dose.

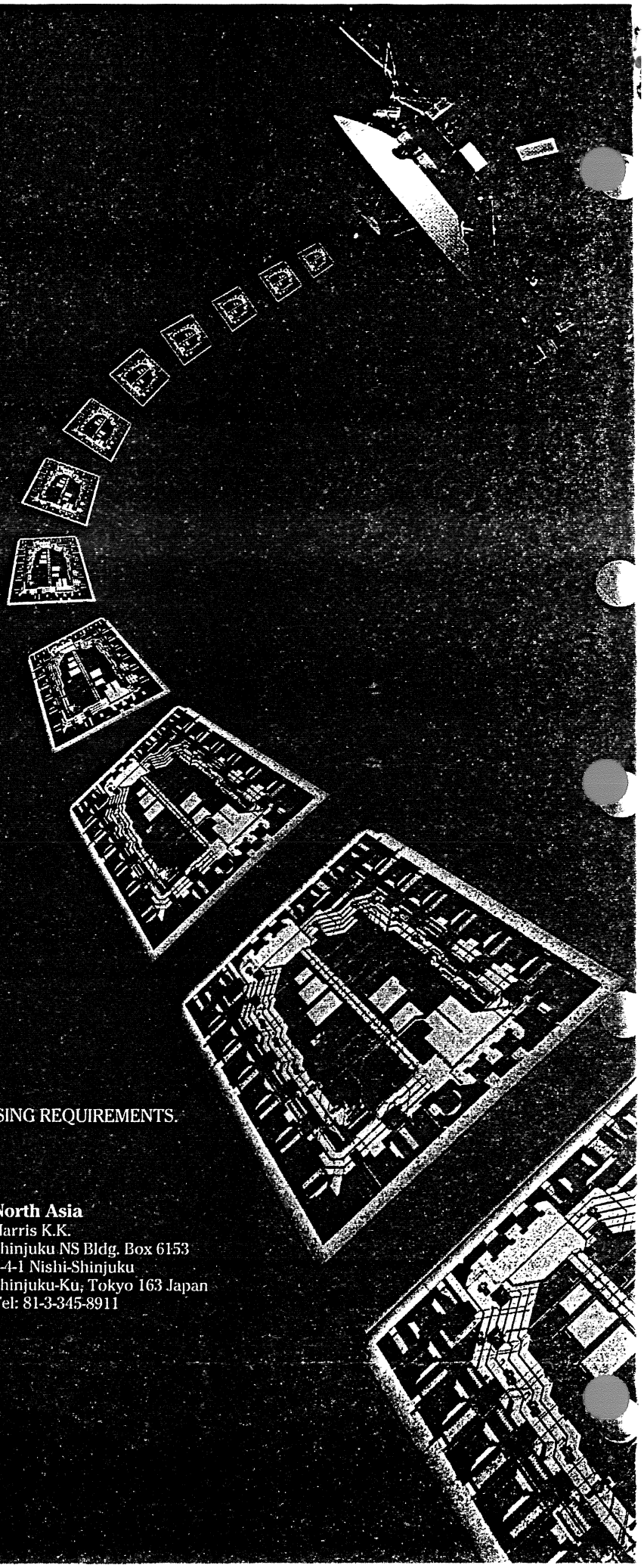
Transmission Gate - A transistor or circuit whose function is to act as a switch, either propagating or blocking the propagation of an electrical signal.

SPACE PRODUCTS NEWS
SPECIAL EDITION AUTHORS
AND EDITORIAL BOARD MEMBERS

NAME	PHONE NUMBER
Clark, Jack	(407) 724-7374
Craig, Darrell R.*	(407) 724-7008
Herrmann, James A.*	(407) 729-5025
Koch, Don G.*	(407) 729-4861
Moody, Scott*	(407) 729-5848
Rauback, Joe W.*	(407) 729-4198
Rivet, Steve*	(407) 724-7319
Schultz, Bill	(407) 724-7491
Strickler, Steve E.*	(407) 729-5869
Tabbert, Chuck	(407) 724-7550
vanVonno, Nick*	(407) 724-7546
Whelan, Linda J.*	(407) 729-4702

* Denotes Editorial Board Member

In addition to the authors and Editorial Board members, we would like to thank Sue Eberle, Sheldon Gottesfeld, Bill Huber, Jeffrey Lee, Ken Ports, Judy Rauback, Hank Swasey, Jim Swonger, Anil Vaswani, and Bill Vigrass for their contributions to this special edition.



ALL PRODUCT SHIPMENTS ARE SUBJECT TO PROPER LICENSING REQUIREMENTS.

Sales Office Headquarters

United States
Harris Semiconductor
1301 Woody Burke Road
Melbourne, Florida 32902
Tel: (407) 724-3739

Europe
Harris Semiconductor
Mercure Centre
Rue de la Fusee 100
Brussels, Belgium 1130
Tel: (32) 2-246-2111

North Asia
Harris K.K.
Shinjuku NS Bldg. Box 6153
2-4-1 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 163 Japan
Tel: 81-3-345-8911

HARRIS SEMICONDUCTOR

BR-035

RAD-HARD

Radiation Effects on CMOS

2

Radiation Hardening

Military, space, and industrial electronic systems are receiving increasing demands for higher immunity from the damage that radiation can inflict upon them. The optimization of radiation hardness is a systems problem which flows through to each subsystem and component integrated circuit. Harris/CICD is the leader in providing radiation-hardened microcircuits for systems designed to be exposed to space or nuclear events.

An integrated circuit can be classified as radiation hardened, radiation tolerant, or radiation resistant. Radiation-hardened devices are guaranteed to meet full parametric levels specified in the data sheets up to the radiation level specified. Functional failure of a radiation-hard device can be 10–100 times greater than the parametric levels listed in the respective data sheet. Devices classified as radiation tolerant or radiation resistant typically meet functional failure levels that are not guaranteed.

Hardening is achieved through:

- Design
- Special fabrication processes
- Continuous screening and quality control

Radiation affects circuits primarily through two basic mechanisms: displacement damage and ionization. Displacement damage occurs when high energy neutrons penetrate the semiconductor crystal lattice and physically dislocate atoms within the structure. It permanently affects lifetime, carrier mobility, leakage current, and bipolar device gain. Ionizing radiation effects can cause interface charge accumulation, which modifies MOS device thresholds and induces parasitic leakage paths. Both effects adversely affect IC performance.

After a device technology has been selected, the circuit is designed to take maximum advantage of the hardening options available for that technology.

BIPOLAR:

- Stabilizing expected gain
- Maximizing emitter current density
- Guard-banding for increased resistor values

MOS:

- Allowances for changes in threshold voltages and leakage currents
- Dielectric isolation
- P+ guard-bands of N-channel transistors

Processing also lends hardness to these circuits. By minimizing gate oxide thickness, employing "hardened oxides," and utilizing proprietary hardening processes, Harris/CICD delivers circuits with higher packing densities and lower redesign costs.

Reliability is an issue that has distinguished Harris/CICD as a leader in the design and manufacture of radiation-hardened memories, microprocessors, op amps, and full custom devices. Strict lot qualification, screening, and testing procedures are maintained, along with stringent radiation screening procedures. All wafers in a run are processed together through all high-temperature steps and metallization, and a sample of probed good dice is selected. These dice are assembled and tested for functionality, then subjected to the total dose radiation level guaranteed for each device, using Harris/CICD's own Gamma Cell 220 Cobalt 60 source with conditions specified by customer requirements. The samples are then tested and accepted by customer-defined criteria.

Introduction

Semiconductors are the backbone of most of today's high-tech systems for commercial, industrial, and defense applications. Whether they are found in land, air, satellite, or spaceprobe systems, such devices are often subjected to severe heat, cold, vibration, and shock. Various types of radiation, occurring either in nature or the result of man-made sources, also present critical environmental problems. In fact, it has been known for years that radiation can change the electrical properties of solid state devices, leading to possible system failure. In particular, gamma rays, x-rays and neutron bombardment have proven most harmful. Radiation-hardened devices and circuits have been developed to minimize the impact of such forces. Moreover, radiation hardening now permits system designers to take full advantage of the benefits of CMOS technology in high performance, high reliability products destined for use in radiation environments.

State-of-the-art wafer fab clean room facilities at Harris are maintained up to a class 10 level.

Hardening For Radiation Environments

Military and space applications require radiation hardened CMOS to operate at total dose and transient radiation levels which are beyond the capabilities of non-hardened devices. Radiation, which in the past had prohibited the use of CMOS technology, is no longer a barrier. Proper design and processing techniques allow CMOS devices to operate in this extremely harsh environment. This process enables system designers to take advantage of the extremely low standby and operating power requirements of CMOS. This publication is a primer on the effects of radiation on CMOS. It will provide the reader with a general understanding of the sources, doses, dose rates, and basic mechanisms that occur during operation of CMOS integrated circuits in a radiation environment.

Natural radiation sources

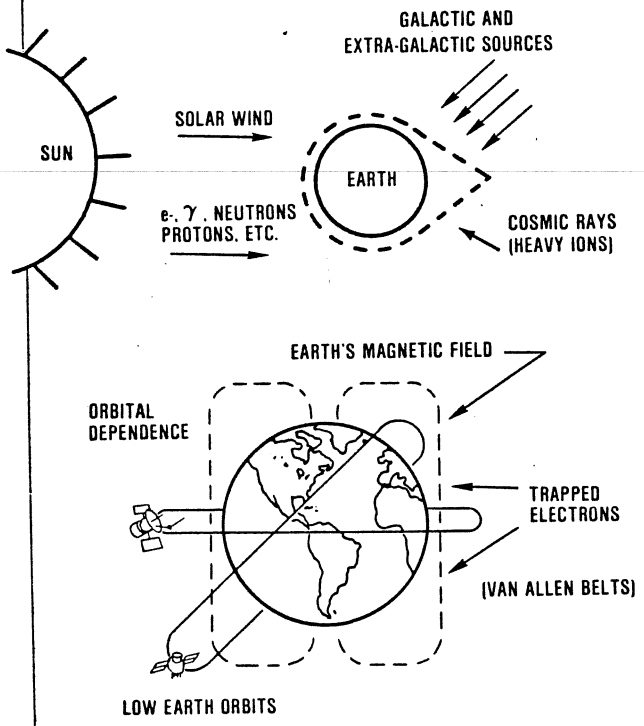


FIGURE 1.

Man made radiation sources

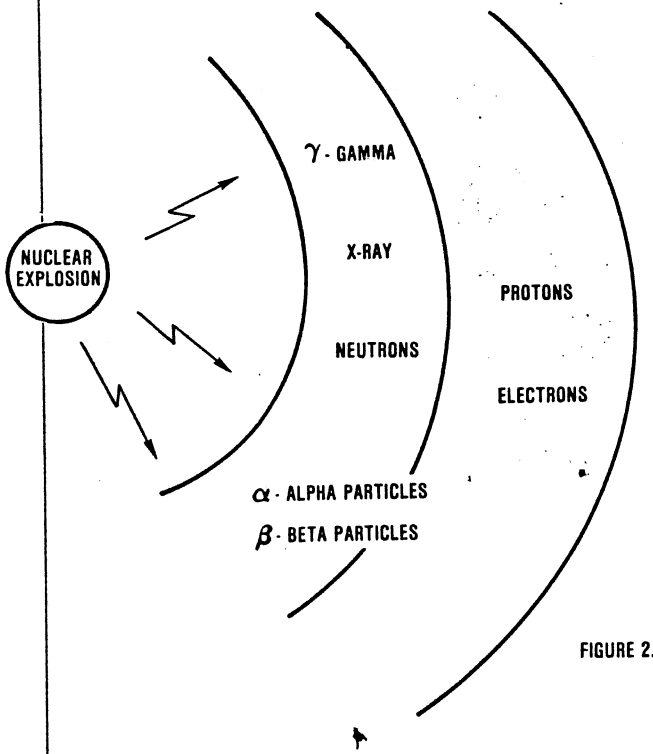


FIGURE 2.

An integrated circuit is said to be radiation-hardened ("rad-hard"), radiation-tolerant or radiation-resistant if it can continue to function within its specifications after exposure to a specified amount of radiation.
Radiation-hardened, as defined for this paper, means that parts are *guaranteed* to meet or exceed specified radiation levels which are one or two orders of magnitude higher than levels of radiation-tolerant or radiation-resistant parts. Radiation tolerance or resistance expresses a capability but does not imply any of the guarantees associated with high reliability rad-hard parts.

Military Radiation Hardness Designators

MIL-M-38510 requires a Radiation Hardness Assurance (RHA) designator to be incorporated into JAN microcircuit part numbers which are listed in Table 1, Appendix A.

The purpose of the RHA designator is to express the reliability of rad-hard microcircuits subjected to various levels of radiation.

In general, hardened CMOS devices will not fail, even in typically high radiation environments. Semiconductor technology has been improved to enable devices to continue to function in much higher radiation levels than ten or even five years ago. Although all semiconductors have some intrinsic resistance or tolerance to radiation, Harris Semiconductor Custom Integrated Circuits Division (CICD) has been able to achieve much higher levels of hardness and high reliability in its rad hard CMOS devices. This has been accomplished through:

- Integrated circuits specifically designed for radiation hardness.
- Special radiation hardening fabrication processes.
- Continous screening and quality control.

Sources of Radiation

Radiation can occur naturally or as the result of man-made sources, such as nuclear explosions and reactors.

As shown in Figure 1, space contains many sources of radiation not found on earth. The space environment is one of major concern for satellites, planetary travel and deep space probes.

Figure 2 identifies man-made radiation sources. A summary of the irradiating particles is given in Appendix A.

Radiation particles can be divided into three basic categories - photons, charged particles and neutrons.

Photons

Gamma rays are photons or quanta of energy. They have identical characteristics to those of x-rays. The difference between gamma rays and x-rays is their source. Gamma rays come from the nucleus, while x-rays are generated by processes outside the nucleus. Gamma rays and x-rays have no electrical charge, travel at the speed of light, and can be stopped by concrete or lead shielding.

Charged Particles

A beta particle is an electron traveling at a large fraction of the speed of light. It is the same as an electron orbiting a nucleus, differing only in speed. The range of a beta particle is about 20 feet in air, and can be stopped by 1/16 inch sheet of aluminum.

An alpha particle is a helium nucleus; that is, a helium atom with the electrons stripped away. It also travels at a large fraction of the speed of light, and can be stopped by a sheet of paper.

Ions are charged particles formed when one or more electrons are stripped away or added to a previously neutral atom or molecule.

Neutrons

A neutron is a particle with no electric charge. Its mass is approximately the same as that of a proton. In nature, neutrons are bound in the nucleus of an atom. They can be knocked out in various types of nuclear interactions.

Interactions

As one would imagine, the interactions of a particle with a target will depend on the properties of each. This dependency can be listed as:

- Particle Properties
  1. Mass
  2. Charge
  3. Kinetic Energy

- Target Properties
  1. Mass
  2. Charge
  3. Density

The types of interactions that can occur with each particle type are given in Appendix B.

The interaction of particles and energies can actually be broken down into two main mechanisms which dominate the effect of radiation in materials in the environments with which we are concerned:

1. Displacement of atoms from their lattice structure (displacement damage).
2. Generation of electron-hole pairs (ionization). Both effects can cause temporary (transient) or permanent damage to semiconductors.

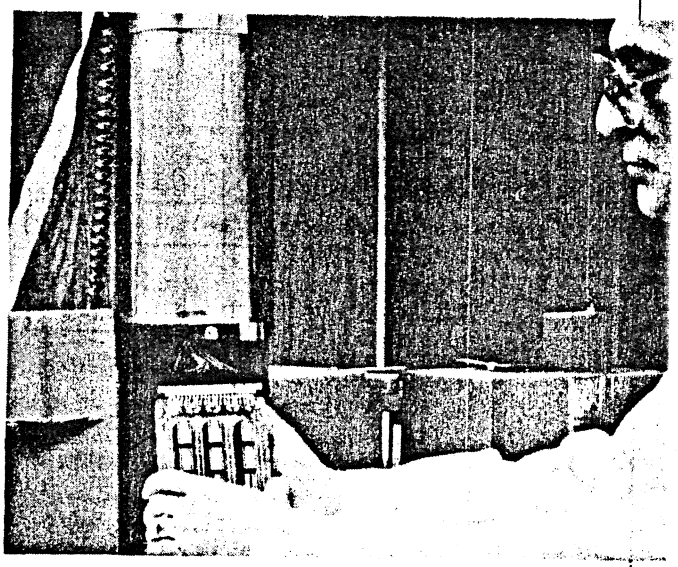
Energy Measured in Rads

The energy transferred to a material by ionizing radiation is measured in terms of rads (radiation absorbed dose). One rad is equal to the energy of 100 ergs per gram of material. The material must be specified, because this energy will differ with each material:

One rad (Si) = 100 ergs/gm (Si)
One gray (Gy) = 100 rads

The ionizing dose rate is referenced in rad (Si)/sec. Particles are referred to in terms of concentration as well as the time integral of concentration:

Flux = Particles/cm^2 x sec
Fluence = Particles/cm^2



The Cobalt-60 source tester provides a gamma radiation dose.

Radiation levels

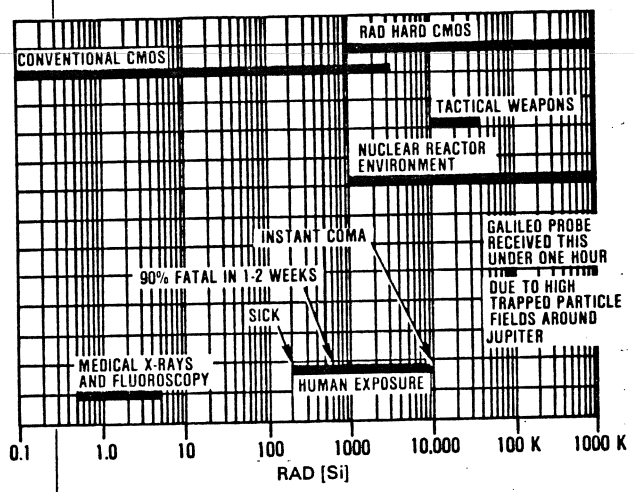


FIGURE 3.

N-channel transistor

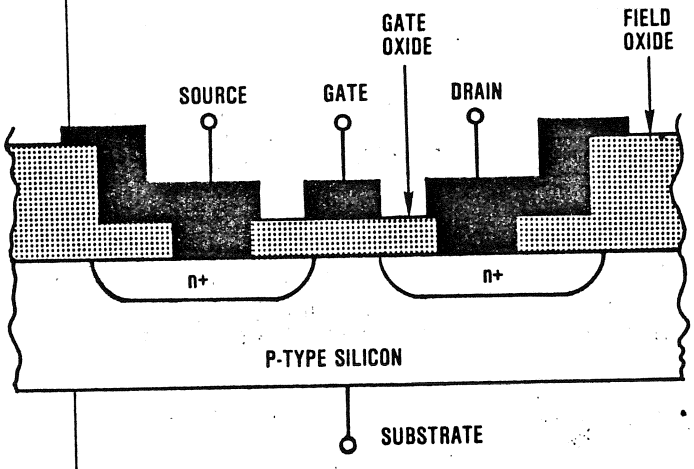


FIGURE 4.

Radiation Effects on CMOS Circuits

As mentioned earlier, radiation affects circuits primarily through two basic mechanisms, displacement damage and ionization.

Displacement damage is caused by heavy charged particles and neutrons. Neutrons are not considered to be a problem in CMOS, as they are in bipolar, until they reach a fluence of $10^{15}N/cm^2$ or greater. Heavily charged particles can cause single event upset. This topic will be discussed later.

Photon interactions, fast neutron interactions (E>1 MeV) and charged particles cause ionization, which is of major concern in CMOS. Photons (gamma) radiation is the primary source of this ionization radiation.

Various levels of radiation exist naturally and can also be generated by man. These levels range from less than one rad to over a megarad (10^6). Figure 3 depicts these levels and also shows the levels where radiation-hardened CMOS is generally utilized. This should give the reader a better idea of the spectrum of radiation levels and the effects of radiation relative to man. Be sure to note the scale is a log scale.

Ionizing Radiation Effects in CMOS/VLSI

The definition of a rad was presented earlier but, how does this relate to an actual device? First we will look at pure silicon:

1 rad (Si) = 100 ergs/gm x
1 electron-hole pair (e-h)
generated for 3.6ev absorbed in silicon

then 1 rad = (100erg/gm) =

$$\left(\frac{10\text{-}7eV}{1.6 \times 10\text{-}19\ erg}\right) X \left(\frac{2.3gm}{cm^3}\right) X \left(\frac{1(e\text{-}h)}{3.6eV}\right)$$

1 rad = 4×10^{13} (e-h)/cm^3 generated

It should be evident that as the dose increases, the number of carriers generated in silicon will also increase. In a space environment, the ionizing radiation that is absorbed by a device can be accumulated over a long period of time; for example, 100K rads (Si) in 20 years. This is referred to as the Total Dose. However, in a weapons environment, a device may be subjected to an extremely large dose within a short period of time.

Doses can be on the order of 10^8 - 10^9 rads (Si) for a few nanoseconds to hundreds of nanoseconds. This type of photon radiation is referred to as Transient Radiation, denoted by gamma dot ($\dot{\gamma}$) - the derivative of gamma with respect to time.

A typical N-channel transistor is shown in Figure 4. *(page 4).*

A MOS transistor can be looked at as a capacitor with the metal and semiconductor as the plates and the gate oxide (silicon dioxide SiO_2) as the dielectric.

Ionizing radiation produces its effects in the gate oxide and also the field oxide regions. These effects are threshold voltage shifts and channel mobility degradation.

The ionization process is illustrated in Figure 5. At $t=0^-$ (Figure 5a), the condition prior to irradiation is shown. At t=0 (Figure 5b), the ionizing energy is delivered to the SiO_2, and the electron-hole population is generated.

Immediately after ionization, the process of electron-hole recombination will occur, but so will electron transport. Electron mobility in SiO_2 at room temperature is approximately 20 $cm^2/V\text{-sec}$, while hole mobility is approximately $2 \times 10^{-5} cm^2/V\text{-sec}$. Because of the applied voltage, any electrons that do not undergo recombination will be swept to the gate and removed in picoseconds, leaving behind the less mobile holes.

These holes will begin a transport process toward the Si-SiO_2 interface as shown in Figure 5e. Some holes will pass into the silicon, while others will become trapped at defect centers very near the interface of the gate oxide and the bulk silicon. (2,3)

Figure 6 depicts the shift in the C-V curve associated with the entire process and the resulting permanent shift due to the trapped charge buildup. In the case of the N-channel device shown in Figure 4, the trapped positive charge will continue to build up and, in effect, make it easier to create the N-channel (inversion layer). This will lower the threshold voltage. See Figure 7 (page 2-8).

The reversal of the threshold shift is caused by saturation of the surface traps and interface state generation at the Si-SiO_2 interface that appear with higher levels of gamma radiation.

This mechanism of interface state generation is not well understood at this time. The simple fact that two different crystal structures meet, silicon and silicon dioxide, and interface will result with some irregularities. This number of irregularities increases with increased irradiation.

Carrier transport mechanism

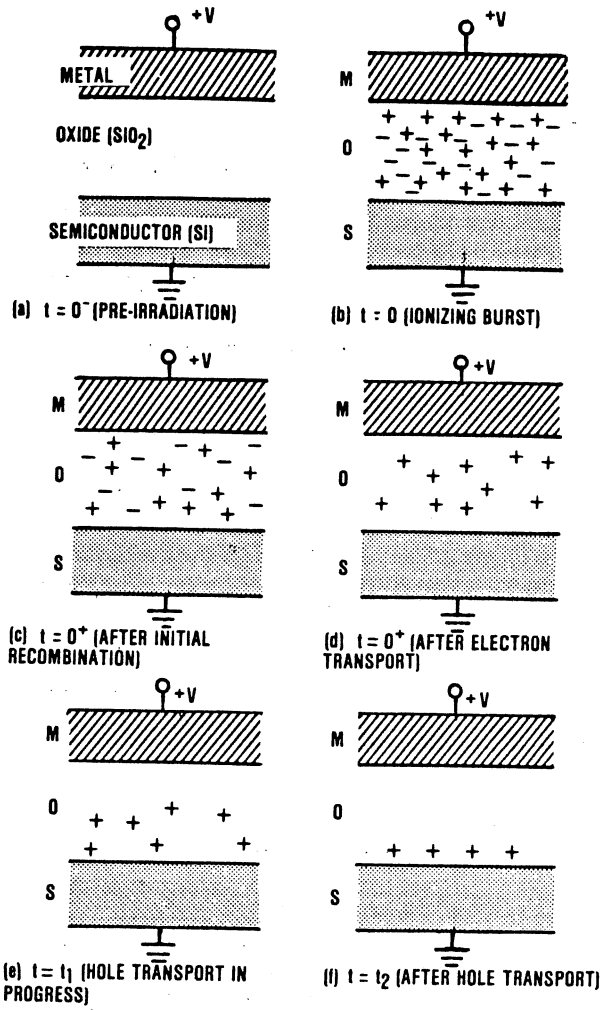


FIGURE 5. Illustration of recombination, transport, and trapping of carriers in SiO_2 films.

C-V curve

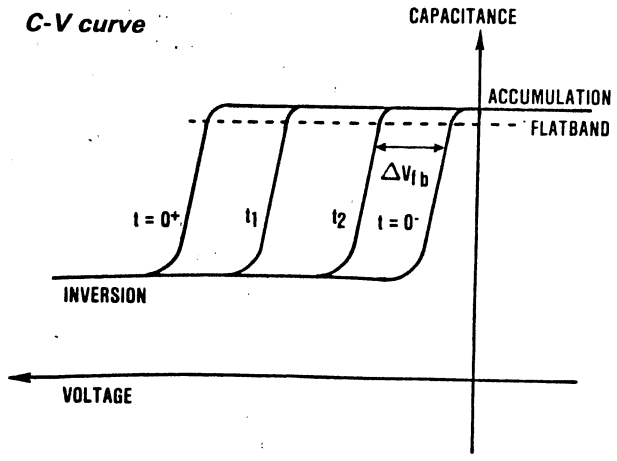


FIGURE 6. Capacitance-voltage curves corresponding to the conditions illustrated in Figure 5.

Radiation effects on P and N channel transistors

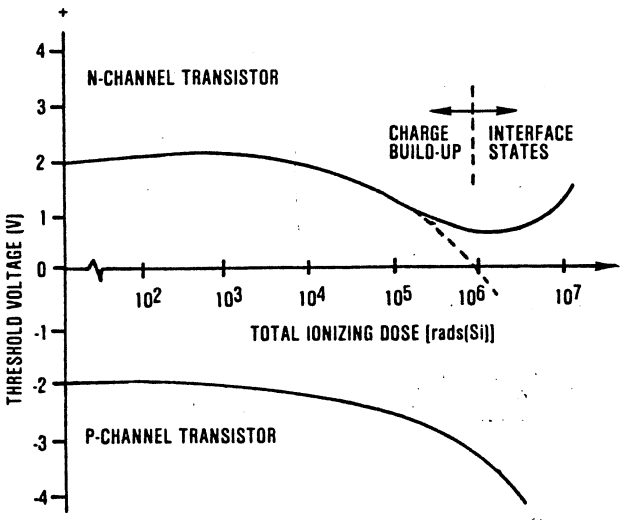


Illustration of the effect of positive charge buildup and interface state production on the threshold voltage in irradiated n- and p-channel MOS transistors.

FIGURE 7.

Carrier mobility degradation

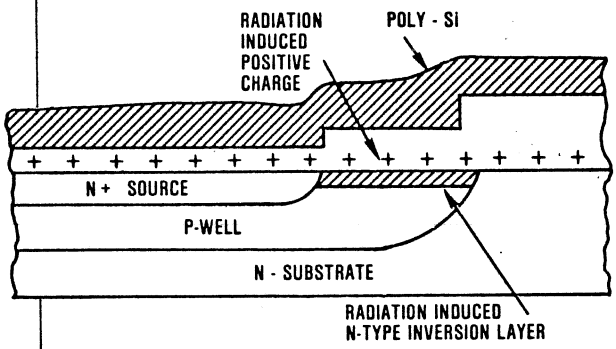


Illustration showing inversion layer which allows current to flow between N- substrate and N+ source.

FIGURE 8.

CMOS inverter

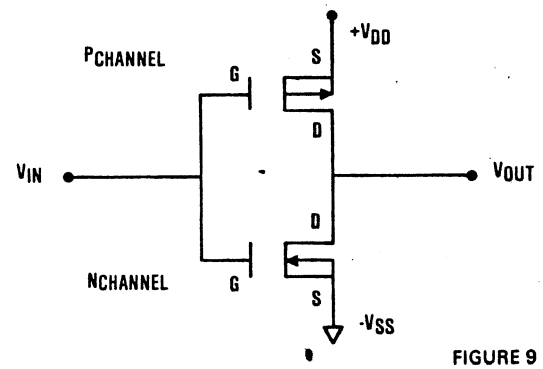


FIGURE 9

In the case of the corresponding P-channel device, the buildup will make it more difficult to create an inversion layer in an enhancement mode P-channel transistor. The effect of gamma radiation on a P-channel threshold is shown in Figure 7. (2)

The net effect of gamma radiation on a CMOS device as a function of threshold shifts is:

1. N-channel devices are easier to turn on or can actually become depletion mode.
2. P-channel devices become more difficult to turn on.

Mobility

Carrier mobility degradation occurs because of the presence of trapped charge near the Si-SiO_2 interface and interface state generation. Interface state generation is the dominant of the two effects.

Interface state generation is negligible at lower levels of gamma radiation. As these radiation levels are increased above 10^6 rad (Si), mobility degradation will affect P and N channel device performance, with increased interface states being the primary cause of the degradation.

Another performance problem induced by the radiation is the increase in leakage current due to surface effects. The ionizing radiation produces excess carriers which can also form a channel between the N+ source and N– substrate (Figure 8). This effect is dramatically reduced through processing techniques.

Annealing

Annealing is the time-dependent detrapping of trapped charge at the Si-SiO_2 interface. It is sometimes referred to as a self-healing effect, which is somewhat true. However, the time constant involved is on the order of minutes to over one year, depending on the level of radiation and the type of processing. The surface states generated are relatively permanent, but can be annealed with high temperatures (>125°C). Any lattice damage (interstitials, vacancies) is permanent.

CMOS

Since continuous operation in most systems is imperative, integrated circuits have been designed to operate within specifications after being subjected to high levels of radiation. Radiation-hardened CMOS has been developed because CMOS technology provides tremendous advantages over other

hardened technologies.

A typical CMOS inverter is shown in Figure 9. It is called CMOS because it is comprised of two complimentary MOS devices. It is a voltage-dependent device, and does not require large current for operation as do NMOS or bipolar devices. The low current requirements, typically 1/5 that of NMOS, provides several benefits.

First, its state of operation is cooler. This allows an increased packing density and lower power requirements. NMOS exhibits an exponential increase in power required as the transistor count goes up.

The lower power requirements yield a cooler operating device. Now systems without heat sinks or cooling fans are easily achievable. The reduction in required current produces smaller and lighter power supplies.

Even more desirable for the system designer is the fact that CMOS lends itself to use in static design. That is, a processor or memory retains its data values even with its clock stopped. Current draw under this condition is under 500μA for typical CMOS circuits. Lighter, smaller, cooler operating devices are essential for space applications where lighter payloads combined with low power consumption and static designs make CMOS ideal for satellite, deep space probes, and battery-powered applications.

Another advantage of CMOS is its property of high noise immunity. Fluctuations in Vin must reach the threshold voltage to cause a change in a CMOS inverter output.

Hardened CMOS at Harris

Harris has been involved in understanding the effects of radiation on semiconductors since 1962, when Radiation Inc. was asked to develop highly reliable custom devices. Radiation Inc. merged with Harris in 1967. Today the Custom Integrated Circuit Division (CICD) offers an extensive line of radiation-hardened data sheet products.

Radiation hardening is accomplished in two ways. The first is through specific design and processing techniques while the second method relies soley on processing techniques.

Basic Processes

The first process involves designing the part to be rad-hard from the very beginning (Figure 10a).

This requires the insertion of the P+ guardbands. During irradiation, the field oxide undergoes the same effects described earlier; i.e., generation of

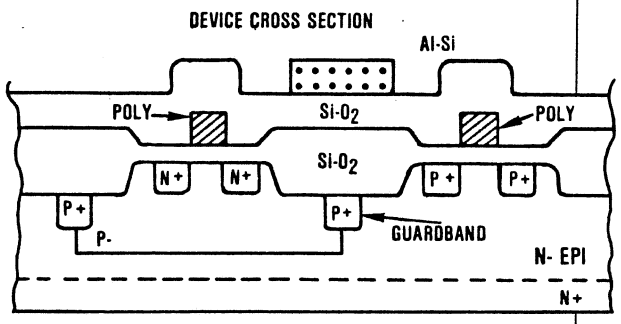


FIGURE 10A

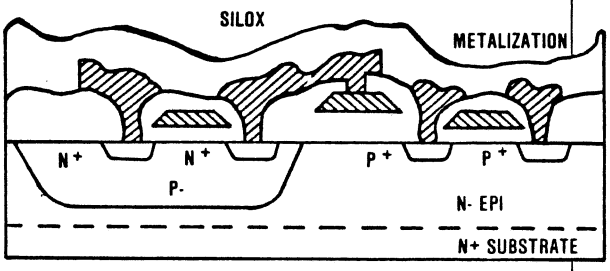


FIGURE 10B

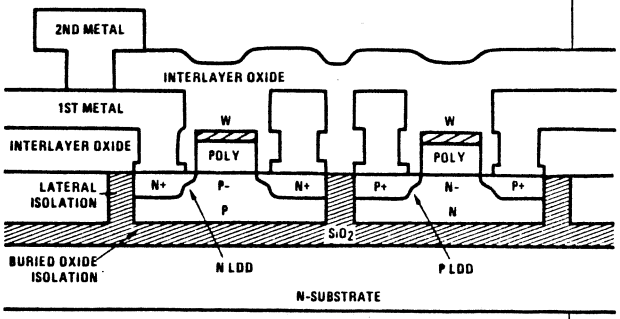


FIGURE 10C

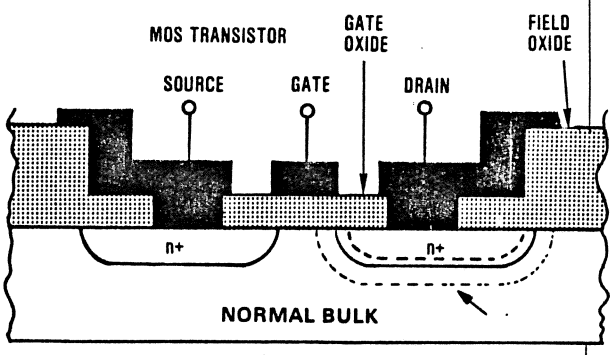


FIGURE 10D

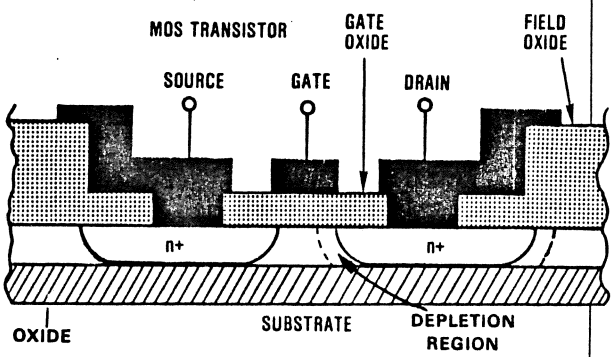
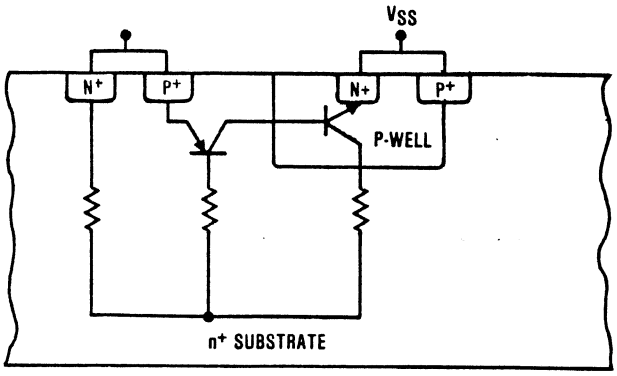
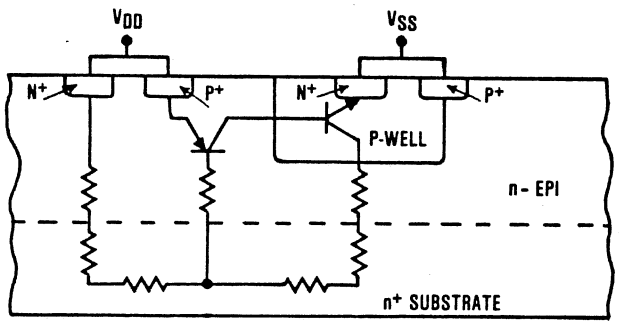


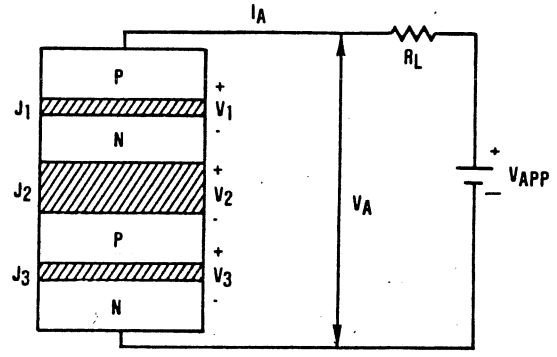
FIGURE 10E



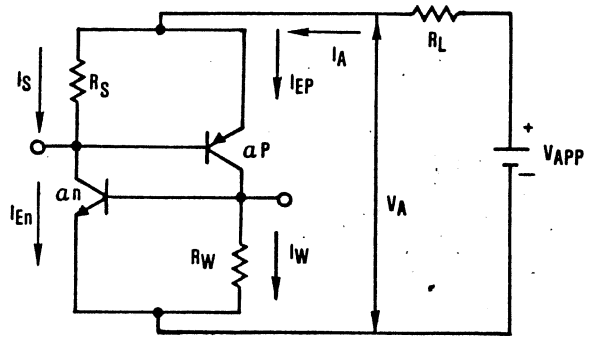
BULK CMOS STRUCTURE WITHOUT EPI LAYER



(a) BULK CMOS STRUCTURE WITH PARASITIC SCR



(b) ONE DIMENSIONAL REPRESENTATION OF SCR



(c) ASSUMED EQUIVALENT CIRCUIT

FIGURE 11.

carriers, trapped positive charge, etc. A parasitic channel (Figure 8) can then be formed in the P well between the N+ channel source and the N− substrate.

Current flowing down this path is called Leakage Current because the current has found an alternative path and is leaking out of the P−well. The guardband prevents this from happening.

It should be evident that every N-channel device would require a guardband. The guardbands are included during the design phase of a circuit. As mentioned earlier, this is done to reduce the leakage current (I_{DD}) that would occur.

Additional processing techniques are implemented that actually harden the gate and field oxides. (4)

It should be noted that the gate material used in both hardening techniques is polysilicon and not metal. (7) This polygate material is deposited first, followed by the P+ and N+ source and drain implants, providing a self-aligning of the gate with the drawn channel.

This eliminates the larger parasitic capacitances that occurred in metal gate technology because of alignment tolerance problems. Metal gates cannot withstand the high temperatures needed for activating the source and drain implants, and must be aligned and deposited after the source and drain are implanted. As a result, metal gates are harder to align and require a minimum of overlap of the drain and source regions to guarantee proper operation.

As device sizes are reduced, this minimum overlap can be large compared to the gate length. This is not a problem for large geometries, but becomes significant for small geometries when slight deviations in alignment can cause serious performance problems. The polysilicon gate completely eliminates these problems.

The second hardening technique has recently been developed at Harris Semiconductor. It provides the same hardness levels and the same low post-radiation leakage current as the guardband process - without the guardbands. This is shown in Figure 10b.

The advantages of this new process are significant. The removal of the guardbands frees up real estate on the chip, which leads to a higher packing density. The second, and more important feature, is the fact that standard CMOS masks can now be hardened without the overhead of redesign to include the guardbands.

A third technology is being developed now at Harris Semiconductor is called Silicon Isolated by

Implanted Oxygen (SIMOX), version of SOI. It will not latch-up, has the potential for increased speed and better packing density, while achieving the goals of increased hardness against transient radiation and single event effects.

This process requires that oxygen atoms be implanted a specified distance below the surface of a silicon wafer. The oxygen atoms form a silicon dioxide layer that becomes a buried insulator (See Figure 10c). This eliminates a large portion of the PN junction depletion region, which is the charge collection region for transient induced photocurrents. Also, by additional process steps for lateral isolation, latch-up is eliminated because four layer SCR paths no longer exist. An improvement in single event effects will also be seen because the funneling and charge collection shown later can not happen through the buried oxide layer (See Figure 10d). As the reader can see, SOI has all the advantages of SOS without the problems associated with growing sapphire and then growing silicon on top of it.

Latch-Up

A four-layer parasitic path exists in bulk CMOS devices. (5) This path can be activated by photocurrents generated by ionizing radiation. The result is a low-impedance, high-current path from V_{DD} to ground; i.e., latch-up.

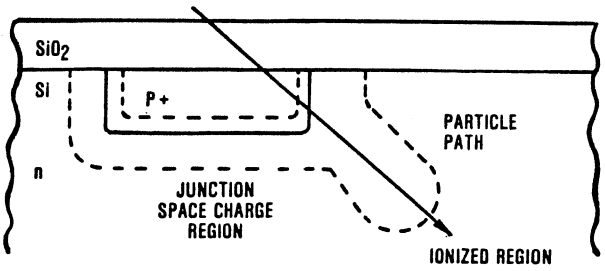
The four-layer path operates like an SCR (Silicon Control Rectifier). This phenomenon of latch-up has been eliminated by growing an epitaxial (epi) layer of lightly doped N material (N–) on the original heavily doped N+ starting material.

The epi material provides a shunt resistor to prohibit the four-layer device from sustaining latch-up. Figure 11 shows a cross-section of a bulk epi CMOS structure and a model of the parasitic SCR device.

Single Event Effects

Single event immunity has recently become a major concern for satellite and space bound systems with memory devices, i.e., RAMs. A single high energy particle can strike a critical node and leave behind an ionized track shown in Figure 12. If the particle hits the drain of the off p-channel device, the resulting voltage transient may be sufficient to cause the inverter in the other half of the memory cell to change state. Because the output of this changed inverter is fed back to the other inverter (the side originally hit), the memory cell

Soft error



CHARGE GENERATED DETERMINED BY:

SUBSTRATE DOPING
PATH
MASS OF PARTICLE — IRON GROUP (Fe, Ar, Kr)
ENERGY OF PARTICLE — AT 100-150 MeV ARE WORST

FIGURE 12.

Memory cells

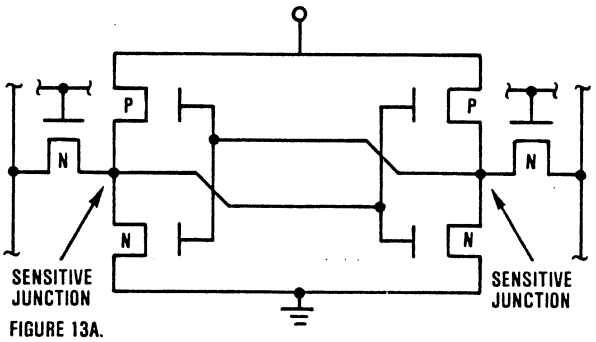


FIGURE 13A.

MODIFIED 6T CELL

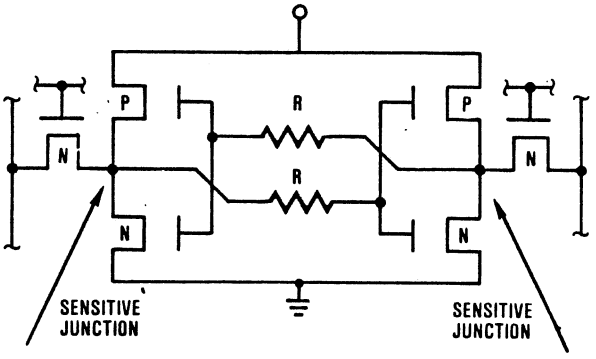


FIGURE 13B.

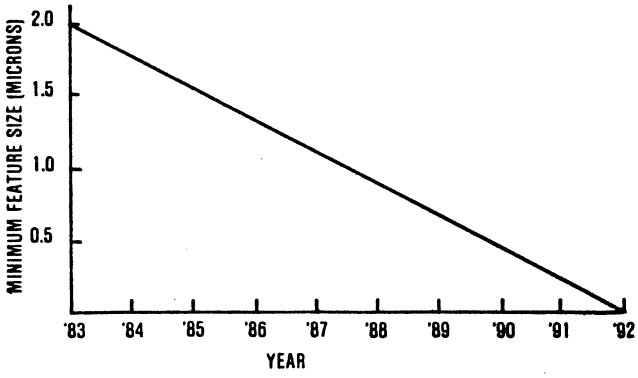
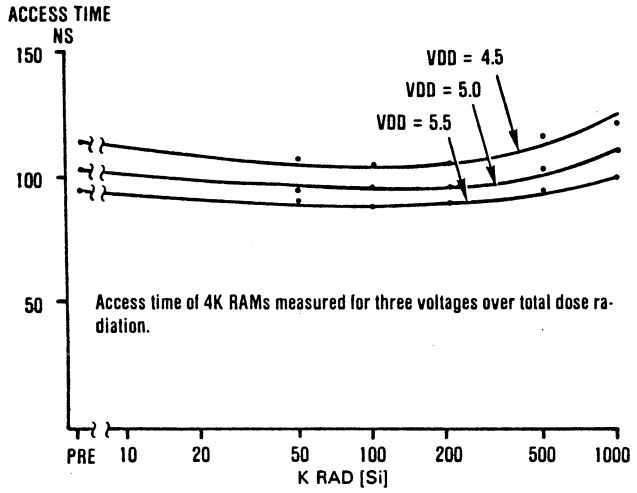


FIGURE 14.



Access time of 4K RAMs measured for three voltages over total dose radiation.

FIGURE 15.

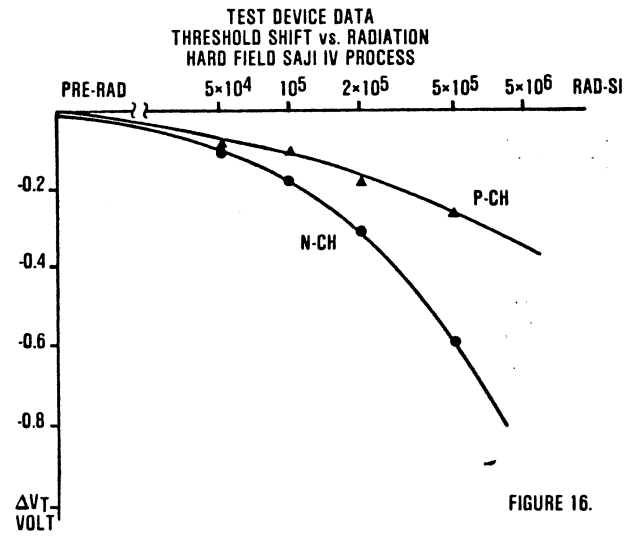


FIGURE 16.

changes state. This is referred to as a soft error (upset). Single event upsets are measured in terms of errors/bit day. A typical six transistor memory cell is shown in Figure 13a.

Figure 13b shows a modified memory cell. The addition of cross coupled resistors in the memory cell has inserted an RC time constant into the transient such that the deposited charge is swept out before the memory cell can react to the voltage transient. This has eliminated upset in bulk CMOS static RAMs to high energy particle impacts. (6)

Another single event effect in bulk CMOS that can be induced by high energy particles is latch-up. If a particle has enough energy, the ionized track left behind could be long enough to punch through the p-well and contact the substrate. This can induce the previously mentioned latch-up mechanism with the same result. As discussed before, the proper thickness epi material will prevent latch-up from sustaining.

EMP (Electromagnetic Phenomenon)

The detonation of a nuclear device will generate an extremely large pulse of electromagnetic energy. This pulse of energy will adversely affect electrical and electronic equipment, even at extreme distances from the source. Shielding is left to the systems designer.

Technological Forecast

Technology will continue to concentrate on advancing the state-of-the-art in radiation-hardened CMOS. This includes reduced geometries and improved process capabilities. See Figure 14.

Basic Hardened Device Data

Presented here is characterization data taken from a few of the product lines manufactured at Harris to show the actual effects of radiation on tested parts.

RAM Access Time

Figure 15 illustrates the steady performance of the Harris Rad-Hard 4K x 1 RAM at various voltage levels and characterized over radiation.

It can be noted from Figure 15 that the RAM access time initially improves with radiation. This can be interpreted as the lowering of the N-channel threshold with increased radiation. The part actually speeds up.

As exposure to radiation continues, the part begins to accumulate more trapped charge at the $Si-SiO_2$ interface and the part begins to slow down. This is due to P-channel threshold shift (more difficult to turn on) and the formation of interface states degrading mobility. It is clear from this figure that the performance is fairly constant out to 1000K rad.

Threshold Shifts

Figure 16 shows the threshold shift over radiation of N-channel and P-channel transistors as measured from a test device.

A summary of radiation effects on standard vs. hardened CMOS is presented in Figure 17. From this figure, it is clear that hardened CMOS is superior to standard bulk CMOS in the critical areas of total dose hardness and immunity to latch-up.

Harris CICD High Reliability

Reliability is a critical item, and often the limiting factor in systems that are unmanned or must remain on line in remote areas. It is an issue that has distinguished Harris Custom Integrated Circuits Division as a leader in the design and manufacture of high-reliability parts from cardiac pacer circuits to radiation-hardened memories, microprocessors, op amps and full custom devices.

Harris CIC Division maintains strict lot qualification, screening and testing procedures. A stringent radiation screening procedure is performed to assure continuous adherence to a parts respective data sheet.

In order to do this, two probed good samples are selected from at least 20% of the wafers in a run. All wafers in a run will have been processed together through all high-temperature steps and metallization. The sample die are then assembled and tested for functionality.

The sample devices are subjected to the total dose radiation level guaranteed for each device, using Harris CICD's own Gamma Cell 220 Cobalt 60 source. The test conditions for the device will be specified in its own data sheet.

The samples are then tested and accepted by the criteria identified in the respective data sheet.

Radiation effects summary

Bulk CMOS Integrated Circuits Can Typically Meet The Following Levels:

	Standard CMOS	Hardened CMOS
Neutrons	$>10^{15}$n/cm^2	
Total Dose	1K - 3K Rad-Si	10^5 - 10^6 Rad-Si
Latchup γ	$\sim 10^9$ Rad/Sec	None
Cosmic Ray	Kr and Ar	
Upset γ	5×10^7 Rads/Sec	3×10^8 Rads/Sec
Cosmic Ray	Kr and Ar	None (CROSS COUPLED RESISTORS)

FIGURE 17

Process control is maintained by such devices as a computer-assisted Nanospec measuring oxide or nitrate coatings.

Appendix A

Summary of irradiating particles:

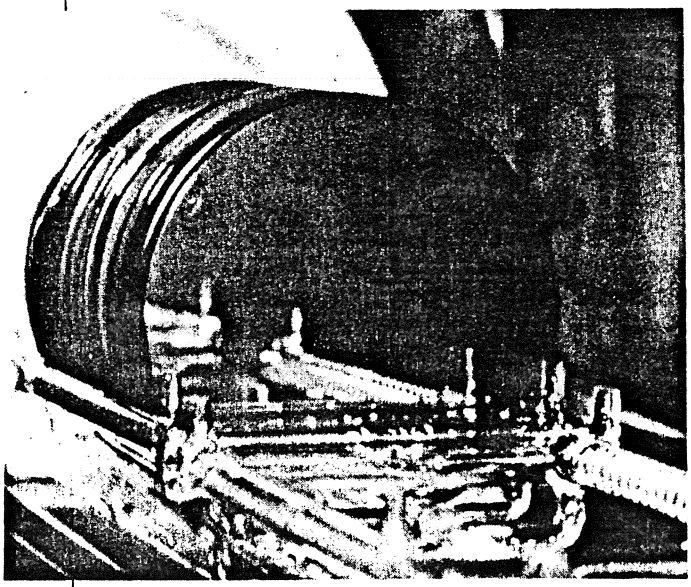
Neutrons
Gamma Rays
X-Rays
Electrons
Protons
Alpha Particles
Ions
Cosmic Rays
- Protons
- Electrons
- Alpha Particles
- Heavier Ions

These particles can be broken down into three categories:

A) Photons
- X-Rays
- Gamma Rays

B) Charged Particles
- Electrons
- Protons
- Alpha Particles
- Beta Particles
- Ions

C) Neutrons



Wafers enter a furnace for oxidation.

Table 1

Mil-M-3851 OF Radiation Hardness Assurance Designators

DESIGNATOR	TOTAL DOSE RAD (SI)	NEUTRON FLUENCE LEVEL n/cm^2
/	NO RHA	NO RHA
M	3000	2 x 10^{12}
D	104	2 x 10^{12}
R	105	10^{12}
H	106	10^{12}

Appendix B

Types of particle interaction:

Photons
- Photoelectric Effect
- Compton Scattering
- Pair Production

Charged Particles
- Rutherford Scattering
- Nuclear Interactions
- (Heavy Particles)

Neutrons
- Scattering
- Absorption

Photons

Photons are pure energy and are electrically neutral. Their effect on target atoms depends on their energy and also the atomic number (Z) of the target.

In all three cases, a free electron is generated. In the photoelectric effect, the photon is completely absorbed by the emitted electron. If there was sufficient energy to free a K shell electron, then an L shell electron will drop down to take its place. An x-ray or low-energy Auger electron will then be emitted, depending on Z. See Figures B1 and B2.

In Compton scattering, the photon has a greater amount of energy than is needed to free an electron from the target material. As a result, the photon is scattered, yielding an electron and a lower energy photon.

In pair production, the photon has a minimum of 1.02 MeV. At this energy, a photon striking a target of high Z is completely absorbed. A positron-electron pair is formed.

The relationship of photon energy and atomic number to interaction type is shown in Figure B3. It is clear from this graph that for silicon (Z = 14), pair production dominates at energies above 20 MeV, and

the photoelectric effect dominates at energies below 50 KeV. Compton scattering is the interaction of most concern in silicon. (2)

Charged Particles

Rutherford scattering is the interaction of charged particles. It can cause both excitation and ionization of atomic electrons. If the particle has enough energy, it can displace atoms in the lattice or even undergo nuclear interactions similar to those exhibited by neutrons.

Neutrons

Nuclear interactions involving neutrons can be classed in two categories: scattering and absorption.

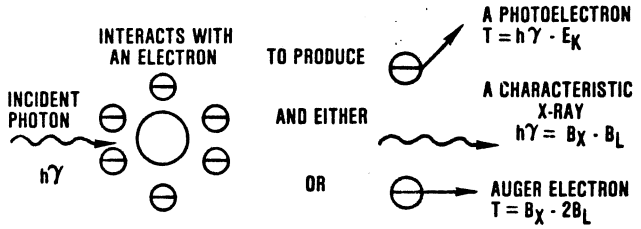
In scattering reactions the process is similar to photon scattering. The incident neutron remains free at a reduced energy, having transferred some of its energy to the target nuclei.

The absorption process is similar to the photoelectric effect of photon absorption, in that the neutron and its energy are absorbed and new particles are generated.

Neutron energies range from a few eV in thermally generated neutrons, to 1 MeV for fast neutrons (fission reactor neutrons), to 14 MeV for fusion neutrons. Neutrons can dislodge an atom from its lattice position.

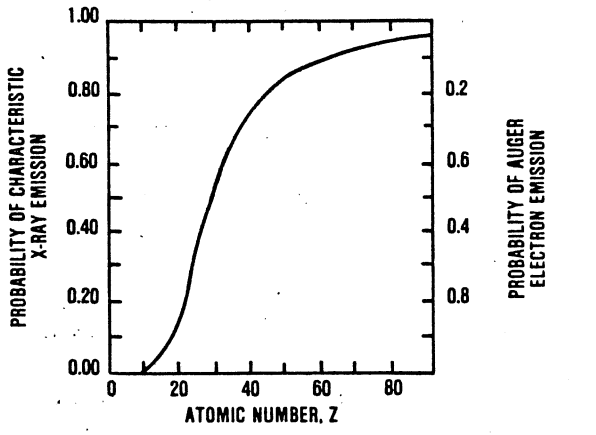
Displacement damage can also occur with high energy charged particles. Displacement of atoms from their lattice position leaves behind a vacancy. The displaced atom may come to rest in a non-lattice position. This non-lattice atom is referred to as an Interstitial.

These abnormalities in the crystal structure are called Defects (see Figure B4). Simple defects are called Point or Isolated Defects, while regions containing a large number of defects are known as Defect clusters.



Sequence of Events in Photoelectric Collisions, shown schematically above.

FIGURE B1.



Probabilities of Auger Electron and Characteristic X-Ray Emission Following the Ejection of a K-Shell Electron.

FIGURE B2.

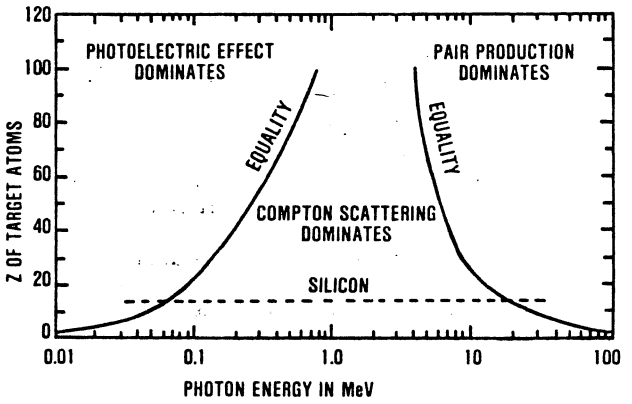
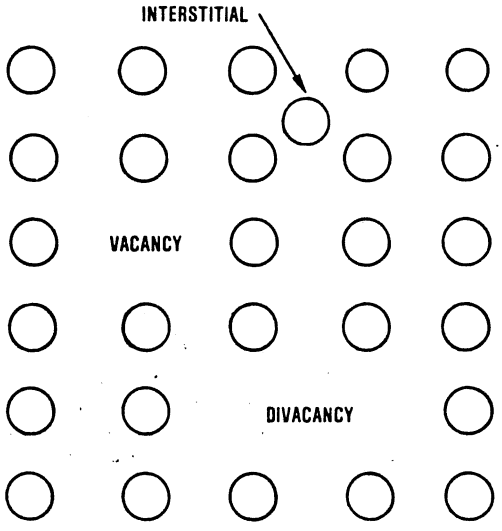


Illustration of the relative importance of the three photon interactions as a function of Z and photon energy. The solid lines correspond to equal interaction cross sections for the neighboring effects. The dashed line illustrates the situation for photon interactions with silicon.

FIGURE B3



Schematic illustration of three types of simple defects in a lattice structure.

FIGURE B4.

A Total Solution Organization

With over two decades of problem solving experience ... the Custom Integrated Circuits Division (CICD) of Harris Semiconductor is a total solution organization. Major military program involvement and specialized product needs are met.

CICD is a proven means of getting high performance, application-specific, custom, semicustom, standard cell and gate arrays. Strategic programs include Trident, MX, B-1B, and SICBM. Tactical programs such as Copperhead, Hellfire, the F-16, and F-18, along with many others, are serviced by this group. CICD has design and production facilities that are COMSEC cleared for classified communications programs.

Data-Sheet plug-in parts that replace non-hardened counterparts are available. Rad-hard bipolar and rad-hard CMOS products in analog, digital, or in combination are available. Advanced Schottky logic and high voltage analog, built to high-rel requirements in your choice of configurations are also available.

CICD is a fully facilitated division operating with a systems house approach to customer interfacing. A Program Manager is assigned to you at the very beginning. From design, masks, fabrication, assembly and testing ... your exact needs are met in product and timeframe. As little or as much as you want!

References

(1) MIL-STD-38510F 31 Oct. 1983

(2) J. Srour, "Basic Mechanisms of Radiation Effects on Electronic Materials, Devices, and Integrated Circuits," IEEE 1982 Annual Conference on Nuclear and Space Radiation Effects.

(3) J. E. Grover, "Basic Radiation Effects in Electronics Technology," IEEE Tutorial Short Course on Radiation Effects 1984.

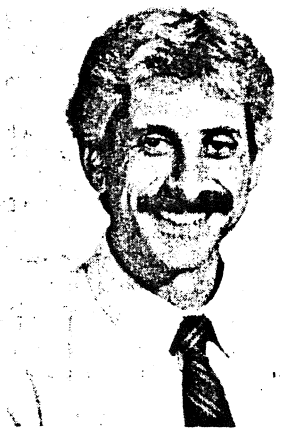
(4) T. J. Sanders, "CMOS Hardness Assurance Through Process Controls and Optimized Design Procedures," IEEE Transactions on Nuclear Science, Vol. NS-24, No. 6, p. 2051-2055, Dec. 1977

(5) J. E. Schroeder, A. Ocha Jr., and P. V. Dressendorfer, "Latch-up Elimination in Bulk CMOS LSI Circuits," IEEE Transaction on Nuclear Science, Vol. NS-27, No. 6, p. 1735-1738, Dec. 1980.

(6) J. L. Andrews, J. E. Schroeder, B. L. Gingerich, W. A. Kolanski, R. Koga, S. E. Diehl, "Single Event Upset Error Immune CMOS RAM," IEEE Transactions on Nuclear Science, Vol. NS-29, No. 6, p. 2040-2043, Dec. 1982.

(7) T. J. Sanders, "Silicon Gate CMOS on Bulk Silicon for Ionizing Radiation Environments," IEEE Transactions on Nuclear Science, Vol. NS-26, No. 6, p. 5056-5059, Dec. 1979.

Gordon Ansell, author of "Radiation Effects on CMOS", is the lead applications engineer with the Special Products Group of the Custom Integrated Circuits Division at Harris Semiconductor. Previously he was the clinical engineer for Mercy Hospital in Miami. He holds an MSE degree from Washington University in St. Louis, Mo.



USING RADIATION HARDENED SYNCHRONOUS STATIC CMOS 4K RAMs

Introduction

Harris Semiconductor offers two radiation hardened CMOS 4K RAMs. Radiation hardened means that the RAMs will continue to function within specifications after exposure to a specified amount of radiation. The HS-6504RH is a 4096 x 1 configuration while the HS-6514RH is available in a 1024 x 4 configuration. Both RAMs are completely static and synchronous in operation. Combining radiation hardness with low power and fast access time makes these RAMs ideal for satellite, space probe applications, or a weapons environment. This application note will compare the CMOS synchronous RAMs to asynchronous RAMs, describe the 4K RAM process, 4K RAM design features, radiation characteristics, and present an example array design and interface.

Synchronous RAMs

The difference between synchronous static RAMs and asynchronous RAMs is quite simple. An asynchronous RAM requires the address inputs to be valid during the entire read or write cycle. The cycle is defined by the address being held valid and by the device being selected for one access or cycle time. An asynchronous RAM may be accessed again before the device is deselected. That is, by changing the address with the RAM already selected, new data will be accessed. The synchronous static RAM requires the address to be valid for only a short period of time at the beginning of the cycle, but requires an edge or transition on the chip enable pin to initiate the cycle. Comparing the two designs (for otherwise equivalent memories), the access time is quicker in the synchronous memory. There is a finite period of time after the access during which the device must be disabled before beginning the next cycle. These differences are illustrated in Figure 1. The name synchronous applies because the chip enable signal synchronizes the internal operations of the memory with the external signal timing requirements. As shown in the figure, the cycle time is from one falling edge to the next. For an asynchronous RAM the cycle time is from one address change to the next and must be held valid throughout the cycle.

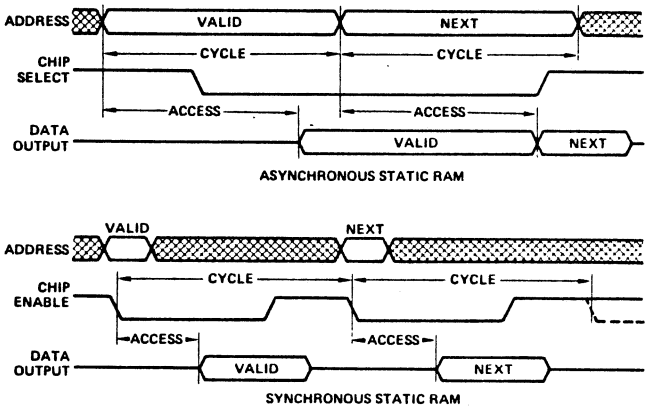


FIGURE 1. RAM TIMING COMPARISON

Power Savings With Synchronous RAMs

Low operating power is a critical feature in any satellite, space probe, or battery powered system. In synchronous CMOS RAMs power consumption is a function of design and operating frequency plus a small leakage current. This means that the RAM only consumes power when it is being accessed. Power is conserved when the RAM is not being used. However, the leakage current in radiation hardened asynchronous CMOS 4K RAMs is relatively high because the memory consumes steady state current to maintain DC paths when the memory is enabled.

In any design, tradeoffs must be made between speed and power, and it is no different in RAMs. In asynchronous CMOS RAMs either speed or power can be optimized but only by one adversely affecting the other. This is much less of a problem for synchronous CMOS RAM designs and therefore speed can be increased without sacrificing power. These tradeoffs can be seen by comparing specifi-

TABLE 1.

	HARRIS HS-6504RH SYNCHRONOUS	RCA CMM5104/1RZ ASYNCHRONOUS
Operating Ranges		
Temperature	-55°C to +125°C	-55°C to +125°C
VDD	4.5V to 5.5V	4.75V to 5.25V
Operating Current		
Maximum	7mA	4mA
Typical	4mA	3.5mA
Standby Current		
Maximum	200μA	1000μA
Typical	6μA	100μA
Operating Speeds		
Maximum Access (Select)	200ns	250ns
Maximum Access (Address)	210ns	250ns
Minimum Cycle	250ns	250ns

cations published by different manufacturers. Table 1 compares speed and power for the Harris synchronous HS-6504RH to RCA's asynchronous CMM5104/1RZ.

4K RAM Process

The 4K RAMs are designed using P well CMOS and are fabricated with a hardened gate oxide using a local oxidation guard ring process. The process involves 10 masking levels (see Figure 2) and uses an epitaxial layer grown on the starting material to eliminate latch up. Latch up is discussed in detail in the section on dose rate effects. The hard gate oxide has been developed to minimize the P and N channel threshold shifts while the guard rings are provided to control the post irradiation leakage current.

Total Dose Radiation Effects on Devices*

The interaction of particles and energies can be broken down into two mechanisms which dominate the effect of radiation in bulk CMOS. The first is displacement of atoms from their lattice structure (displacement damage) and the generation of electron-hole pairs (ionization). The main sources of ionizing radiation are gamma rays and charged particles, while the main source of displacement damage is neutrons and heavy charged particles. Both effects can cause temporary (transient) or permanent damage. The two major factors affecting the performance of any radiation hardened CMOS device are threshold shifts and mobility degradation.

An MOS device can be looked at as a capacitor with the gate material being one plate, the gate oxide being the dielectric and the P (or N) material being the other plate of the capacitor (see Figure 3). During gamma irradiation

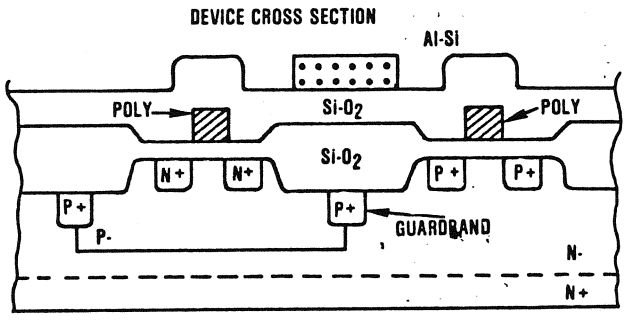


FIGURE 2. DEVICE CROSS SECTION

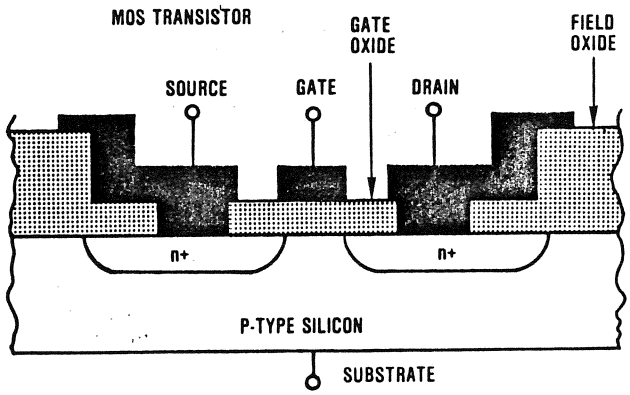


FIGURE 3. MOS TRANSISTOR

* For a more detailed explanation of these processes see Section 2: Radiation Effects on CMOS.

additional carriers are generated in the dielectric (the gate oxide). The mobility of the two carriers is very different. The mobility of the generated electrons is approximately 20cm^2/V-sec while hole mobility is approximately 2 x $10^{-5}cm^2$/V-sec. Because of the applied voltage any electrons that do not undergo recombination will be swept to the gate and removed in picoseconds leaving behind the less mobile holes. The holes will begin a transport process towards the Si-SiO_2 interface. Some holes will pass into the silicon while others will become trapped at defect centers near the interface of the bulk silicon and the gate oxide material (see Figure 4). This layer of trapped charge will actually shift the threshold voltage associated with this device by some delta. As a result N channel devices become easier to turn on (this example) and P channel devices become harder to turn. The same mechanism occurs in the field oxide region also. This will cause an increase in leakage current. In order to control the leakage current P+ guard rings are used to prevent a parasitic channel from being formed in the P well between the N+ source and the N- substrate (see Figure 5).

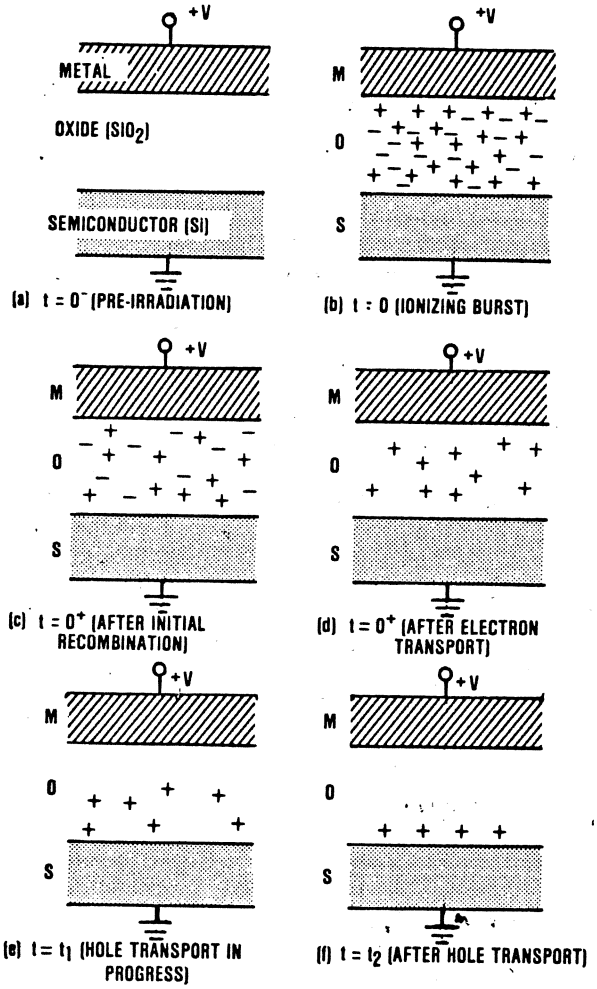


FIGURE 4. CARRIER TRANSPORT MECHANISM

Illustration of recombination, transport, and trapping of carriers in SiO_2 films.

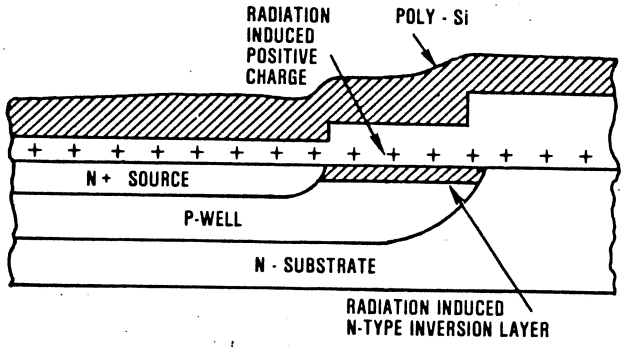


FIGURE 5. CARRIER MOBILITY DEGRADATION

Illustration showing inversion layer which allows current to flow between N- substrate and N+ source.

Carrier mobility degradation occurs because of the presence of trapped charge near the Si-SiO_2 interface and interface state generation. Interface state generation is the dominant of the two effects, but is beyond the scope of this application note. Mobility degradation begins to become significant at about one megarad (10^6 Rad(Si)).

Annealing is the time dependent releasing of trapped charge at the Si-SiO_2 interface. It is sometimes referred to as a self healing effect, which is somewhat true. However, the time constant involved is on the order of minutes to over one year depending on the radiation level and the type of processing. Any surface states generated are relatively permanent but can be annealed with high temperatures (>125°C). Any lattice damage is permanent.

Dose Rate Effects On Devices

During transient radiation up to 20,000 rads or more can impinge upon a semiconductor device in nanoseconds to microseconds. This sudden burst of energy will generate a very large amount of free carriers. In reverse biased junctions the electrons will be swept out immediately causing a large photocurrents to flow. These photocurrents can cause a device to latch-up (stop working) or even to burnout. This occurs in the following manner. A four layer parasitic path exists in conventional bulk CMOS devices. This path can be activated by photocurrents generated by ionizing radiation. The result is a low impedance, high current path from VDD to ground. The four layer path operates like an SCR. This phenomena of latch-up has been eliminated by growing an epitaxial layer of lightly doped N material (N-) on the original heavily doped N+ starting material. The epi material provides a shunt to prohibit the four layer

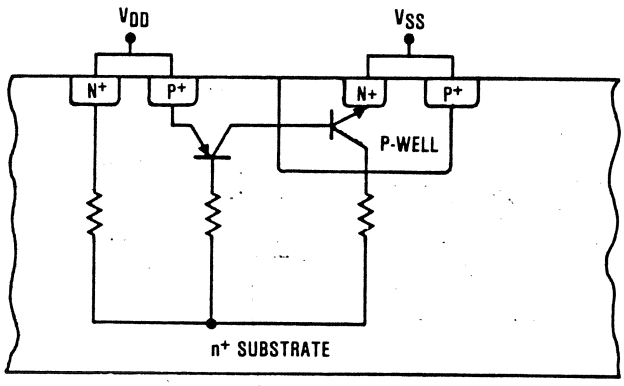


FIGURE 6. BULK CMOS STRUCTURE WITHOUT PARASITIC SCR

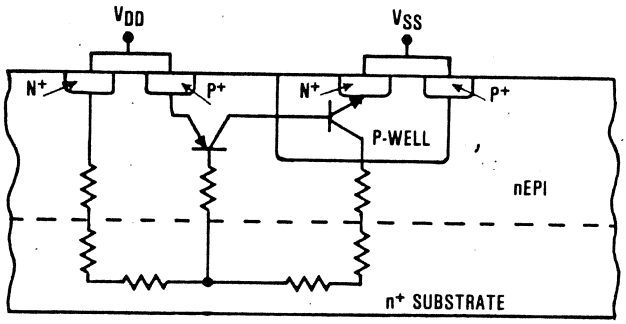


FIGURE 6a. BULK CMOS STRUCTURE WITH PARASITIC SCR

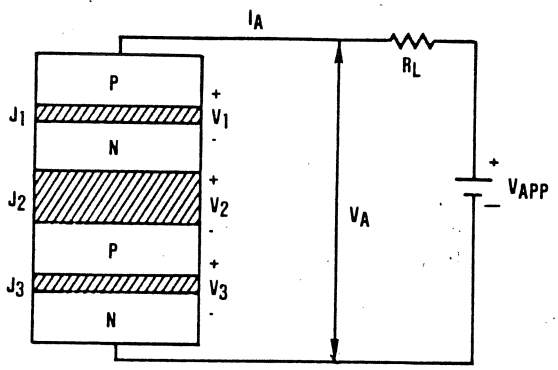


FIGURE 6b. ONE DIMENSIONAL REPRESENTATION OF SCR

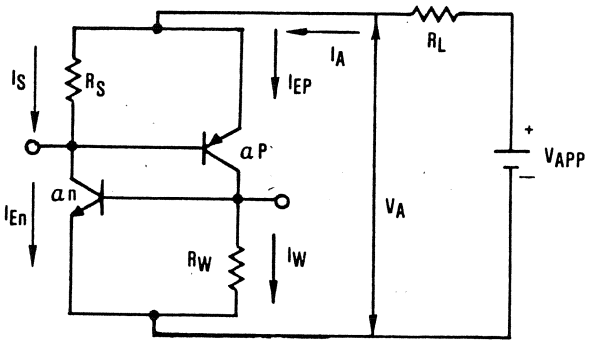


FIGURE 6c. ASSUMED EQUIVALENT CIRCUIT

device from sustaining latch-up. Figure 6 shows a cross section of a bulk EPI CMOS structure and a model of the parasitic SCR device.

4K RAM Design Features

Both of the Harris 4K CMOS synchronous static RAMs possess a number of features that provide added flexibility for the system designer. The address buffers and data inputs are TTL compatible (VIH min = 2.5V) so there is no need for any pull up resistors. This will help reduce the board count. The data outputs are also TTL compatible. On chip latches are provided for all inputs (address, data in, and read/write) and data out. This makes it much easier to interface to multiplexed bus and microprocessor systems and also helps reduce the chip count since these signals no longer need to be latched externally of the RAM. When the RAM is deselected (chip enable goes high) the data outputs are forced into a high impedance mode (three-state outputs). This is very advantageous if you are planning expanded memory arrays.

The low power consumption of CMOS was touched on earlier as being essential for satellite type applications. The low standby and operating current requirements of static synchronous CMOS RAMs (6μA standby typically) comes from the fact that CMOS inverters only draw current when they are switching from high to low or from low to high logic levels. A typical CMOS inverter is shown in Figure 7. From this figure it is easy to see that only one gate (either the N FET or the P FET) will be conducting at any one time. This prevents any current from flowing directly from VDD to ground except leakage current. However, during operation the input to the inverter will be making a transition from one logic level to another. When it is in between 1.5 V and 3.5 V both gates will be biased on allowing current to flow. This dynamic switching current is the major component of the operating current drawn by the RAM. In addition to the switching current there may be a direct current sourced by the RAM and supplied to a load. This load current only exists in systems where the

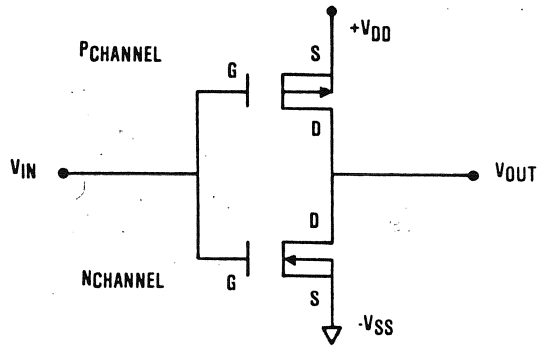


FIGURE 7. CMOS INVERTER

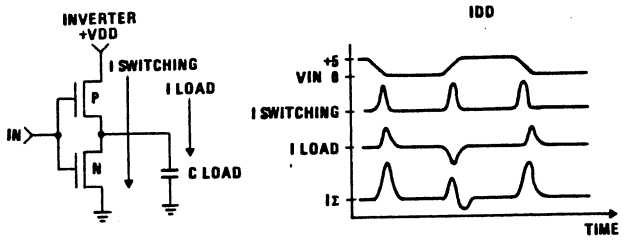


FIGURE 8. CMOS DYNAMIC OPERATING CURRENT

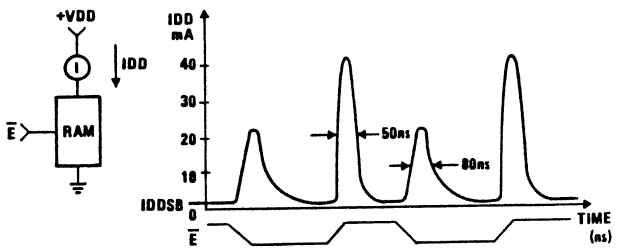


FIGURE 9. SYNCHRONOUS RAM IDD

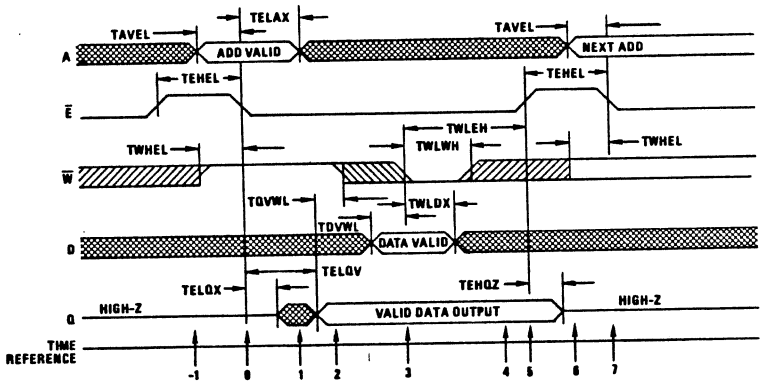
outputs drive a load containing a resistive component, such as a TTL load. Figure 8 depicts the dynamic operating current for an inverting buffer.

As a result of the synchronous design, the chip enable input controls many gating functions inside the RAM. It latches the address registers, gates column and row decoders as well as sense amplifiers. Every time the chip enable input makes a transition, hundreds of gates are switched. The dynamic current of all of these gates can be summed up and in doing so can be called the operating current of the RAM seen at the power supply pin. This current is shown in Figure 9.

Some systems may place the address and data lines in a high impedance mode or leave them floating. This could cause the RAM inputs to be at an intermediate voltage and hence, draw current. This is very important because floating address inputs could draw current even though the RAM is deselected. This would have an impact on the standby current. The Harris RAM inputs are unaffected by this because of a highly innovative input buffer design which firmly holds the input at its last logic level limiting the standby current to a maximum of 200μA under worst case conditions. The standby current under normal operating conditions at room temperature is 6μA.

Design Features Of The HS-6504RH 4K x 1 RAM

The HS-6504RH comes in a 4K x 1 configuration. As mentioned earlier it has internally latched addresses as well as data I/O. The RAM also has separate data in and data out pins. The latched data I/O and separate data in and data out pins allows the RAM to be operated in what is called a Read/Modify Write mode. In this mode data is read out of the RAM and new data written into the RAM all within the same cycle. The timing diagram for the read/modify write mode is shown in Figure 10. A typical



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disable
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid, Read and Modify Time
3	L	↘	X	V	V	Write Begins, Data is Latched
4	L	X	X	X	V	Write in Process Internally
5	↗	X	X	X	V	Write Completed
6	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
7	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

FIGURE 10. READ MODIFY WRITE CYCLE

application of the Read/Modify Write mode would be signal processing. Data could be read from the RAM, processed through a high speed processor and written back to the same memory location to be processed again later. Another application for this mode is pipeline data manipulation. The Read/Modify Write mode provides increased speed and power savings for the designer because in this mode data is read and written during the same cycle but chip enable has been strobed only once. Remember, the majority of the operating power is consumed when chip enable goes low. Precharge, address decode and a number of other internal functions have already been accomplished and do not need to be duplicated. This saves power and increases speed.

Since chip enable is used to clock the HS-6504RH, additional speed is achieved by making the chip enable a CMOS input. The minimum VOH of a TTL device is 2.4V, while the VIH of a CMOS device is 3.5V. This means the address and data inputs must be buffered up internally to the required CMOS level. The buffering does require time. This buffering time is not required for chip enable and the chip enable clocking occurs faster than it would if all the inputs were TTL compatible. The Read/Write input is also a CMOS input for the same reason.

Design Features of the HS-6514RH 1K x 4 RAM

The HS-6514RH 1K x 4 RAM features bi-directional I/O ports for the data inputs and data outputs. As a result, the pin count of the chip has been kept to a minimum. Because of this bi-directional configuration, the HS-6514RH does not need to have latched data inputs and data outputs as in the HS-6504RH. The RAM does feature the latched address buffers. All inputs and outputs are TTL compatible (VIH min = 2.5 volts) on the HS-6514RH. Under worst case operating conditions the HS-6514RH is about 25ns slower than the HS-6504RH.

4K RAM Total Dose Radiation Characteristics

As mentioned earlier, these memory devices are designed to withstand the effects of radiation. The radiation may be natural in origin or can also be man made. These sources can be solar wind, cosmic rays, trapped particles in the Van Allen belts, nuclear reactors, or nuclear weapons. The section on radiation effects briefly discussed how radiation can cause the threshold voltage of an MOS device to shift. These threshold shifts can cause a change in the operating characteristics of any device. In particular, gamma radiation can cause changes in the access time, standby leakage currents, address buffer input levels, and also set up a bias dependence, (preferential recognition of one logic level over another) in non-radiation hardened RAMs. However, these RAMs have been designed to minimize the threshold shifts and allow Harris to guarantee that the RAMs will operate within their specifications over a broad range of radiation levels.

The RAMs are first characterized over voltage and temperature to determine their performance. They are then subjected to radiation and characterized again. Any deviations in performance will then be noted. The total dose radiation testing conducted at Harris is performed using a Gammacell 220 Cobalt 60 source which has a minimum dose rate of 100 Rad-Si per second. A number of RAMs are placed under bias and radiated to a specific level and then tested. They are then returned to the Gammacell, radiated to the next level and retested. The post-rad data is compared to the pre-rad data. Figure 11 shows the pre-rad access time at three different operating voltages taken over temperature. The access time is well under the guaranteed worst case access time of 200ns. Figure 12 shows the same parameter measured over radiation at the worst case operating voltages. It can be

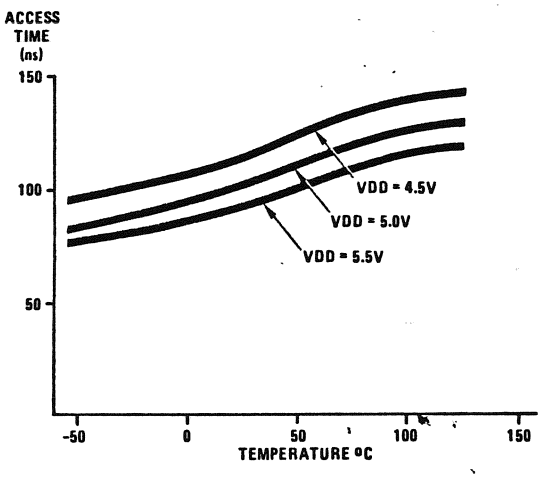


FIGURE 11. ACCESS TIMES OF 4K RAMs MEASURED OVER TEMPERATURE AT THREE VOLTAGES.

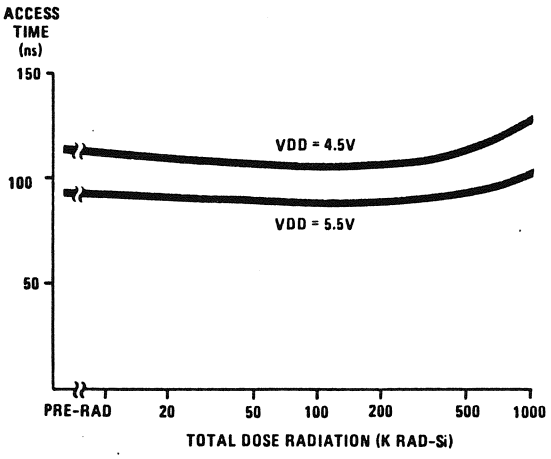


FIGURE 12. ACCESS TIMES OF 4K RAMs MEASURED FOR 2 VOLTAGES OVER TOTAL DOSE.

seen that the access time actually decreases over radiation because of threshold shifting of the n channel devices (they become quicker). After about 500K rads the displacement damage and interface state generation take over and mobility degradation becomes the dominant mechanism and the access time begins to rise.

After the devices under test are removed from the radiation source, another mechanism called annealing, will effect the device characteristics. Annealing is the time dependent detrapping of the trapped charges causing the thresholds to shift. It can be looked at as a self healing effect that can take days to over a year to complete. The two curves of Figure 13 show the effect of 96 hours of annealing at room temperature with no bias. The solid line represents the insitu measurements while the dashed line shows the threshold shift annealing out after 96 hours. The effect of mobility degradation on access time can be seen beginning at about 400K rads. Annealing is affected by temperature and bias conditions. Elevated temperatures aid in the detrapping of trapped charge by providing thermal energy needed for recombination to occur at the Si-SiO_2 interface. Reversing the bias across the gate oxide will also speed annealing by inducing the trapped holes to migrate back up through the gate oxide where there is an increased possibility of recombination.

The low SIDD, standby current, is an important feature of the RAMs. Figure 14 shows leakage current vs. radiation at 4.5 volts and 5.5 volts. It was discussed earlier that the CMOS static synchronous RAMs only draw current when they are switching except for a small leakage current. This leakage current is also affected by threshold shifts. The leakage current has been observed to anneal back to its prerad levels in about 10 to 24 hours. The standby leakage current SIDD versus radiation is shown in Figure 14.

Bias Dependent Radiation Effects

The effect of biasing on a circuit and state the circuit is in during rradiation can have a substantial impact on circuit performance. There are certain modes which minimize the bias effects while other modes make these effects more pronounced. In this section we will discuss these modes and show how to reduce bias dependency in the 4K RAMs.

The active mode in which the memory is written and read continually with different data patterns is the best bias condition for operation during irradiation. Actually no bias dependency will occur because no bias is maintained while the RAM is constantly being accessed, written, read and deselected. Under this condition a more even weighting of high and low bias conditions exist on the individual MOS devices.

The next best case for extended exposure to radiation is the static bias condition in which the memory is deselected. This biasing condition allows all critically matched devices of the differential sense amp and the address buffers to have the same bias across the gate oxide. Threshold shifting will occur but it will shift by the identical amount in these devices. They will shift but still be matched which is the essential part.

The bias condition which can reduce the total dose hardness the most is accessing one bit of the memory and leaving it in the selected state for exposure to radiation. The gates of two matched devices will now have different voltages across them. As a result, the devices now have different threshold voltages because the threshold shift of the matched devices is not the same. The threshold mismatch will cause the sense amplifiers to sense a pre-

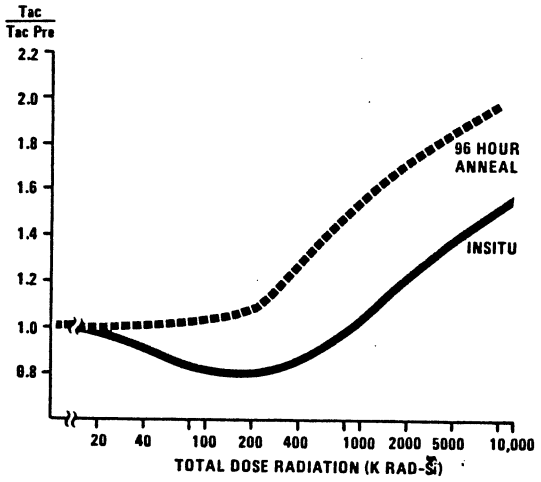


FIGURE 13. RELATIVE CHANGES IN ACCESS TIME OF 4K RAMs MEASURED OVER RADIATION.

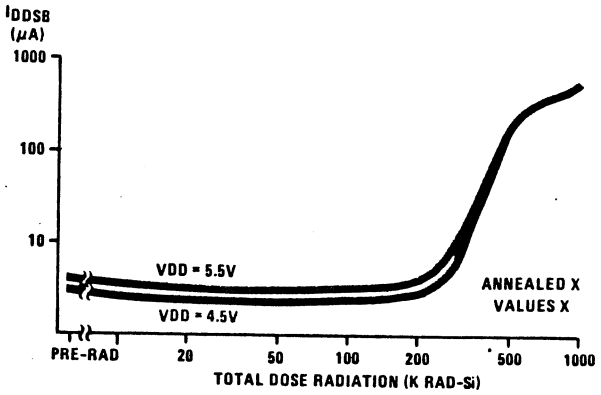


FIGURE 14. 4K RAMs IDD STANDBY vs. RADIATION FOR 2 VOLTAGES.

ferred logic state regardless of the data on the bit lines. This effect will anneal out as the device thresholds anneal. However, it will cause improper operation of the device for a short period of time (10 to 24 hours after irradiation). Another situation that can cause a problem is the reading of all ones or all zeros in a column during irradiation. This will also cause the sense amplifier transistors to become unmatched due to bias dependent threshold shifting. Although this is "dynamic" operation and the mismatched condition will not be as severe as the static mode, it can cause reduced total dose hardness.

4K RAM Dose Rate Effects

The effect of transient radiation and the mechanism of latch-up on CMOS was discussed earlier. In addition to latch-up, memory cell upset (loss of stored data) can also occur. Tests have been performed using short duration x-rays (they exhibit the same properties as gamma rays) to determine what radiation level is required to cause the memory to upset. Typically, 20ns wide pulses are used. No latch-up or burnout has been seen with dose rates as high as 2×10^{12} rads/sec with pulse widths of 20ns. This test was performed in both the static deselected mode as well as in the static selected mode. Anomalous high currents have been seen if the RAM is biased in the static selected mode. This will occur if the row decoders are upset. Simply deselecting the RAM will bring it out of this high current mode and place the row decoders in a known state.

Tests of memory cell upset have been performed with a 20ns pulse width and found to occur between 3×10^8 and 5×10^8 rads/sec. Memory cell upset from a 100ns pulse can be caused by a slightly reduced dose rate between 1×10^8 and 1.5×10^8 rads/sec. Long pulse effects (> one microsecond) have also been studied. For static mode tests, memory cell upset could be found to occur at about 5×10^7 rads/sec. Dynamic operation was upset at 1×10^6 rads/sec. During the long pulse tests the large photocurrent present causes the reference voltage on the address buffers to disappear. Data being read or written would be incorrect because the addresses would be invalid.

Single Event Upset

Single event upset immunity has recently become a major concern for satellite and space bound systems with memory devices, i.e., RAMs. A single high energy particle can strike a critical node and leave behind an ionized track shown in Figure 15. If the value of this charge is high enough, a voltage change can occur causing a bit to change states. This is referred to as a soft error. Single event upsets are measured in terms of errors/bit day. A typical six transistor memory cell is shown in Figure 16a. Figure 16b shows a modified memory cell. The addition of cross coupled resistors has made the memory cell immune to single event upset. The mechanism is as follows. The transistor gate (capacitor) and resistor act like a low pass filter and prevent the sudden voltage change at the node from affecting the gate voltage. The duration of the event is so swift that the memory cell remains stable. Single event testing has been performed at the Berkeley cyclotron with the results listed in Table 2.

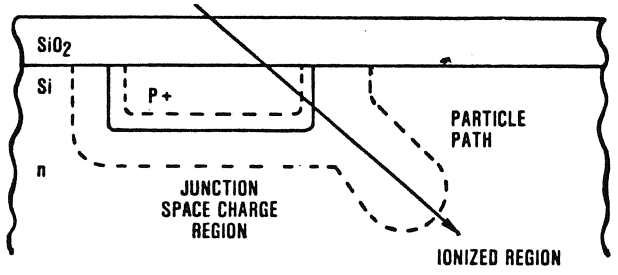


FIGURE 15.

The heavy charged particle used in the tests is krypton and several different angles of incidence were used. 70° has been found to deposit the most charge and cause the most upsets in cells without the cross coupled resistors. No upsets are seen under the same conditions with the cross coupled resistors.

The resistors are made of polysilicon and have a negative temperature coefficient. As the temperature goes down the resistance goes up and as the temperature goes up the

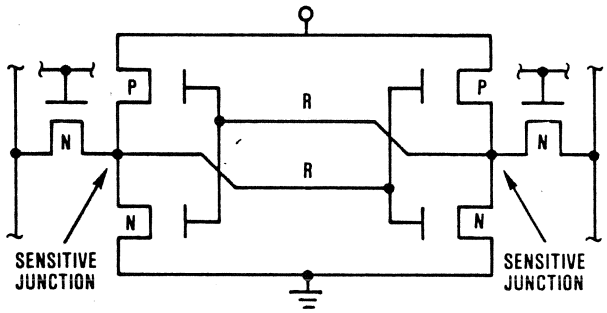


FIGURE 16a.

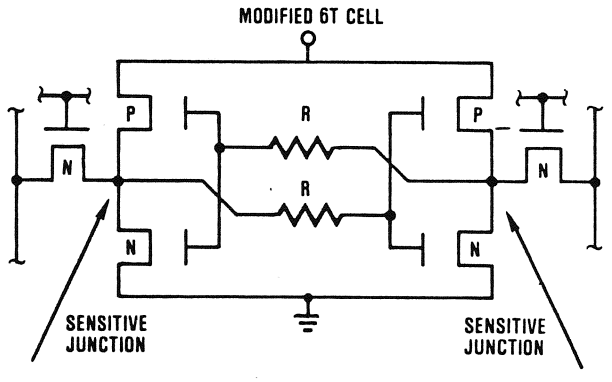


FIGURE 16b. MODIFIED 6T CELL

TABLE 2.

Charge Generated Determined By:	
Substrate Doping Path	
Mass of Particle	IRON Group (Fe, Ar, Kr)
Energy of Particle	100-150meV are Worst
Angle of Incidence	70°

resistance goes down. As a result, single event immunity is offered as an option when ordering either 4K RAM and has a slightly reduced operating range of -20°C to +80°C. Beyond +80°C the value of the polysilicon resistor becomes too low to prevent single event upset from occurring. The RAMs will still operate to the data sheet but will no longer be immune to single events. As the temperature drops below -20°C the resistance of the polysilicon resistors increases making it more difficult to write data into the memory cell. The RAMs will still be immune to single events but the write cycle is lengthened and no longer meets the data sheet. Since most satellite applications do not exceed these temperatures the reduced temperature range for single event upset immunity should not be a problem. If the RAMs are being used in a ground or aircraft system there is no need for single event immunity and the standard RAMs with full temperature range (-55°C to +125°C) can be used.

Additional Applications of Synchronous Memories

One of the primary applications of radiation hardened synchronous CMOS memories is multiplexed bus memory arrays used in some satellites. The on board address, and data latches provide easy interface to microprocessor. Figure 17a and Figure 17b show typical examples of memory arrays using the 4K x 1 configuration and the 1K x 4 configuration, respectively. The design engineer must take the same precautions with radiation hardened memories as with any other CMOS static synchronous memory. Input bus capacitance must be considered.

In Figure 17a all 32 RAMs are addressed at the same time for example.This is a highly capacitive load. Driving this with a TTL load can cause ringing to occur. This is because the printed circuit board traces have inductive properties and yield a distributed LC network. The most common solution is to add series resistance to dampen the ringing. Other methods can be implemented to reduce ringing, but these usually increase overall system power consumption. These methods include terminating the receiving end to VDD or ground. This will draw more current from the driver. The alternative choice to a TTL device is a CMOS device. The HS-82C12RH is well suited for this task.

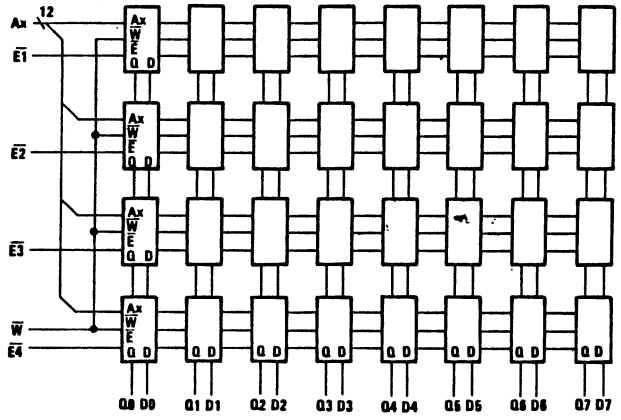


FIGURE 17a. 16K x 8 RAM ARRAY, 32pcs. HS-6504RH

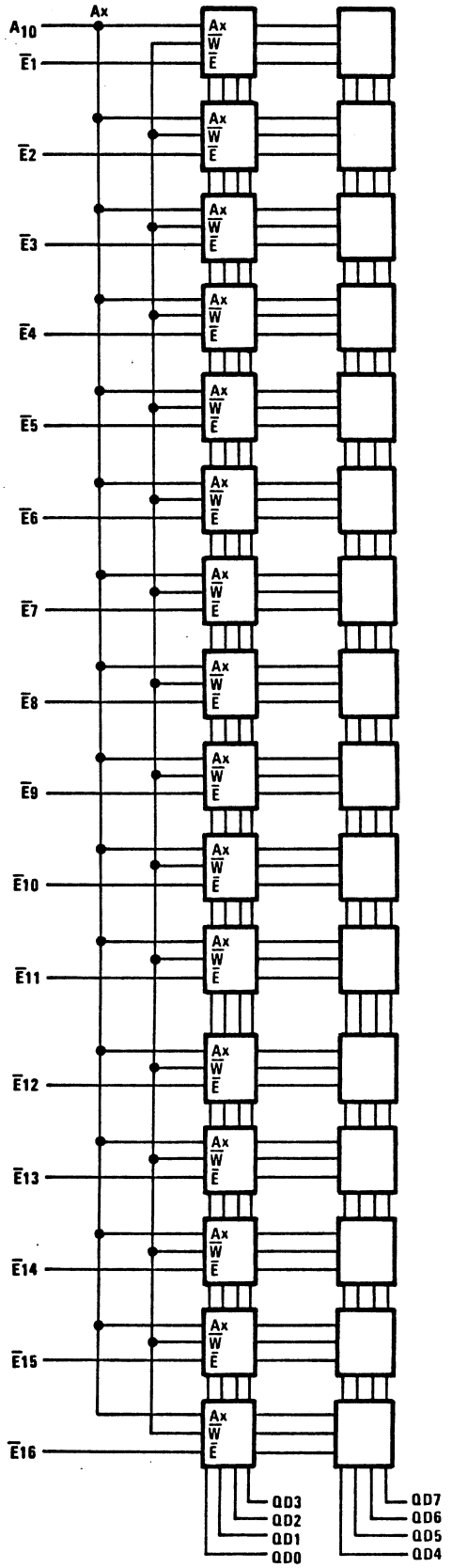


FIGURE 17b. 16K x 8 RAM ARRAY, 32pcs. HS-6514RH

Another area for concern is the output drive capability of the RAMs. The RAMs are guaranteed for speed with a 50pF load. However, there will be a difference between the two arrays (17a and 17b) in terms of the access time because of bus capacitance. The HS-6514RH will be slower than the HS-6504RH because the bus capacitance will be about four times a great. That is, the data bus capacitance will increase as more devices are placed on the bus.

A speed versus power tradeoff also exists when considering the 4K x 1 or 1K x 4 RAMs for array configurations. The propagation delay of the address decoding logic is traded for the operating power of the array. For an example, a 16-bit wide word will be considered. Sixteen one bit wide RAMs will be needed or four four bit wide RAMs will be needed. Since they both consume the same operating current, the 1K x 4 array will consume less power than the 4K x 1 because only four RAMs will be operating at a time instead of all sixteen. However, the additional address decoding needed to decode down to the 1K word level will incur a propagation delay time that will have to be added to the access time when calculating system timing.

Microprocessor Interfacing

These RAMs can be interfaced and used with any microprocessor. Because of the special feature of operation in a radiation environment it makes sense to interface to a microprocessor that will also be able to operate in the same environment. The Custom Integrated Circuits Division (CICD) of Harris Semiconductor offers the only radiation hardened CMOS microprocessor. It is a radiation hardened CMOS version of the Intel 8085. The part number is HS-80C85RH. A family of radiation hardened peripherals is also available to further enhance design capabilities.

The key to interfacing to any microprocessor is deriving the chip enable signal from control line signals. The chip enable signal is needed to latch the addresses into the RAM and begin the memory cycle either to read or to write. Some processors provide this signal to indicate that the address lines are stable. If not, additional logic gates are needed to produce the chip enable signal from timing and control signals.

In the case of the HS-80C85RH (Figure 18) interfacing is quite simple. The chip enable signal can be derived from the ALE signal provided by the processor. The ALE signal can be used to gate a decoder (HS-54C138RH radiation hardened 3-8 line decoder/demux) and supply the chip enable signals needed to latch the addresses into the RAM. The higher order addresses need not be latched because they are held stable for the entire length of the cycle.

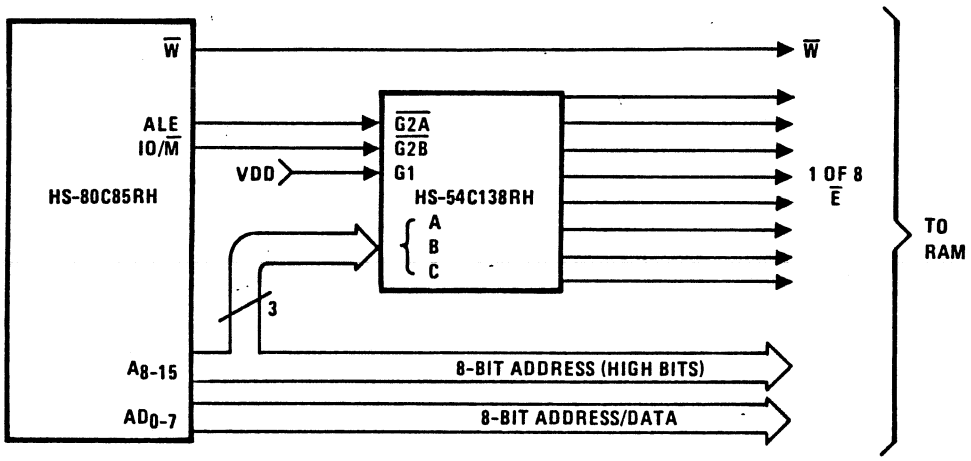


FIGURE 18. HS-80C85RH INTERFACE TO RAM

For additional information on interfacing either the HS-6504RH or HS-6514RH 4K RAMs with the HS-80C85RH, refer to Tech Brief 501, page 12-20: "Interfacing Rad Hard 4K RAMs to the HS-80C85RH Rad Hard μP".

Bipolar processors exist that can also operate in a radiation environment. The SBP 9000 is an example. Interface to it is simple because the signals necessary to generate the chip enable signal is available (Figure 19). However, the power requirements of this device is 400mA compared to the 6mA/MHz of the HS-80C85RH. The high power needed for operation make this device inappropriate for satellite and space applications.

Radiation Screening and Production Flows

Harris Custom Integrated Circuit Division maintains strict lot qualification, screening and test procedures. A stringent radiation screening procedure is performed to assure that the RAMs adhere to their respective data sheets.

Conclusion

The use of radiation hardened synchronous static CMOS RAMs has been presented with applications emphasizing their speed, low power, and synchronous operation. In addition, the RAMs characteristics and performance in various radiation environments was also presented. General interfaces and preferred modes of operation under radiation have been given to provide the design engineer with an increased knowledge of designing systems with radiation hardened memories.

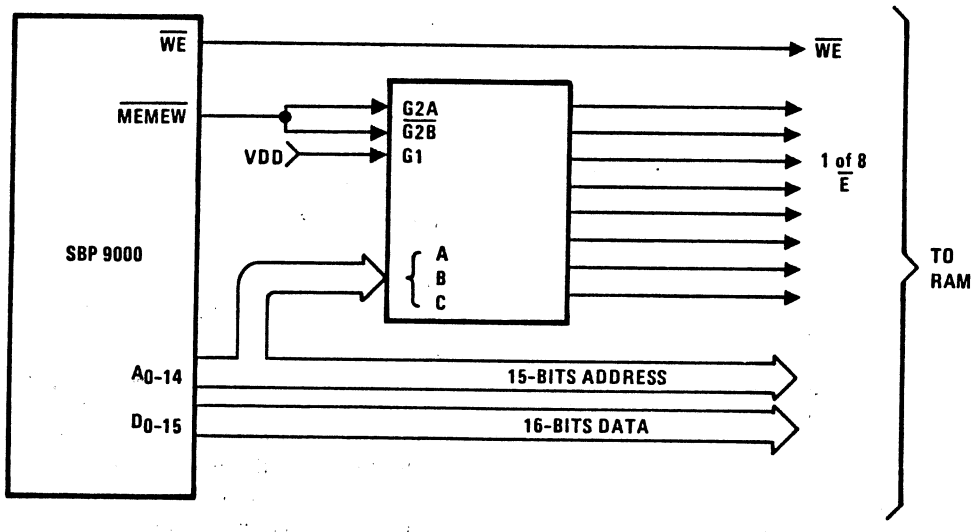


FIGURE 19. SBP-9000 INTERFACE TO RAM

CMOS in Radiation Environments

Gordon P. Ansell and Joe S. Tirado, Harris Semiconductor, Melbourne, FL

Military semiconductors have been manufactured for many years. These devices are tested to military standards and can survive the effects of heat, shock, vibration, and moisture. In today's modern battlefield, these devices must also survive the effects of radiation from nuclear weapons and space environments.

Semiconductors used in military systems need to survive the effects from total dose, transient, and neutron radiation from nuclear events. In space, devices must survive the additional effects of single-event upset from bombardment by ions present in galactic cosmic rays, solar flares, or trapped protons in radiation belts around Earth. Thus, designers need radiation-hardened or radiation-tolerant devices.

Radiation-hardened devices fit the needs of many systems quite well, providing megarad protection for many strategic programs. Recently, however, a number of IC manufacturers not previously concerned with IC radiation survivability have been making claims regarding the *radiation tolerance* of their devices. These devices typically are not designed to survive radiation effects, yet offer survivability as a by-product of the manufacturing process. Radiation-tolerant devices do not offer a guaranteed radiation specification, but have been sample-tested to show their inherent tolerance to radiation. For many tactical or low Earth orbit systems with low radiation requirements, rad-hard devices may offer survivability levels far greater than are necessary. In these cases, radiation-tolerant devices may offer an alternative to rad-hard devices. However, test data on radiation effects must be understood in order to make an accurate assessment.

Typical Radiation Effects

Semiconductors may encounter many different kinds of irradiating particles including photons (gamma rays and x-rays), charged particles (electrons, protons, alpha particles, and other ions), and neutrons. Although all types of radiation may be present, the important ones are ionizing radiation, heavy ions, and neutrons.

Two primary mechanisms dominate the radiation effects in the environments with which we are concerned: displacement of atoms from their lattice positions (displacement damage) and generation of electron-hole pairs (ionization). Both effects can cause temporary (transient) or permanent damage to semiconductor devices.

The types of radiation with which we are concerned and their effects are presented in Table 1. Total dose radiation is the accumulation of ionizing radiation over a period of time—hours, days, or years in a space environment. The total dose could also be accumulated in a short period in a weapons environment. The dose is the energy transferred to the material; it is measured in terms of rads (radiation absorbed doses). One rad is equal to 100 ergs of transferred energy per gram of material. The material must be specified, because this energy will differ with each material.

Exposure	Performance degradation	Upset or data loss	Latch-up	Catastrophic failure
Total dose	CMOS Bipolar			CMOS Bipolar
Transient (γ)	CMOS Bipolar	CMOS Bipolar	Conventional CMOS	Conventional CMOS
Single-event effects	CMOS Bipolar	CMOS Bipolar	Conventional CMOS	Conventional CMOS
Neutron	Bipolar			Bipolar

TABLE 1. Radiation types and effects on CMOS and bipolar devices.

Transient (prompt gamma) radiation refers to the large pulse of ionizing radiation seen in a short period of time (nanoseconds to microseconds) following a nuclear event. The total dose is the time integral of this dose rate. The major concern in transient radiation from weapons outside the atmosphere is short-pulse radiation and within the atmosphere, the major concern is long-pulse radiation. The ionizing dose rate is given in rad (Si)/s.

Heavy ions (iron in particular) cause single event effects by depositing charge in critical areas or nodes. Finally, neutrons cause crystal damage. Neutron fluence is given as particles per square centimeter, or N/cm^2. Neutron fluence is the time integral of the particle flux, N/cm^2-s.

Note that the level of radiation (total dose, transient, and so on) required to cause the effects listed across the top of Table 1 will be different for CMOS and bipolar devices. Bipolar devices are minority carrier devices and will be affected by radiation that causes lattice damage and creates additional recombination sites.

Radiation Effects on CMOS Circuits

Whereas displacement damage caused by heavy charged particles and neutrons is a concern with bipolar devices, neutrons are not considered to be a problem in CMOS until they reach a fluence of 10^{15} N/cm^2 or greater. Rather, ionizing radiation is the major concern in CMOS and photon (gamma) radiation is the primary type. (Other types are charged particles and fast neutrons). Various levels of radiation exist naturally and can also be generated by man. These levels range from less than one rad to over a megarad (10^6 rad).

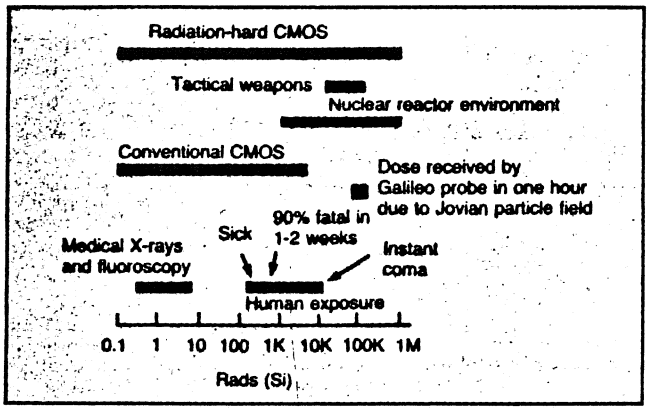


FIGURE 1. Radiation levels.

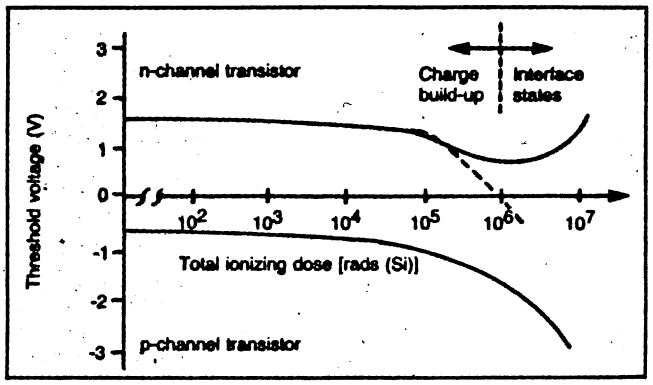


FIGURE 2. Threshold voltage shift versus radiation dose.

Figure 1 depicts these levels. Radiation-hardened CMOS is generally utilized at 1000 rad and above. This should give you a better idea of the spectrum of radiation levels and the effects of radiation relative to man.

How does the radiation dose relate to an actual device? One electron-hole pair is generated for 3.6 eV of energy absorbed in pure silicon. The density of silicon is 2.3 g/cm^3, so 100 erg/g corresponds to 1.44×10^{12} eV/cm^3. Thus, 1 rad generates an electron-hole pair concentration of 4×10^{13} per cm^3. In a space environment, the ionizing radiation that is absorbed by a device can be accumulated over a long period of time, say 10^5 rads (Si) in 20 years. However, in a weapons environment, a device may be subjected to an extremely large dose in a very short period of time—on the order of 10^8-10^9 rads (Si) for a few nanoseconds to hundreds of nanoseconds.

Threshold Voltage Shift

A MOS transistor can be viewed as a capacitor, with the polysilicon (or metal) and semiconductor as the plates and the gate oxide (SiO_2) as the dielectric. Ionizing radiation affects the gate oxide and the field oxide regions. These effects are threshold voltage shifts and channel mobility degradation. Initially, the ionizing energy is delivered to the SiO_2 and an electron-hole population is generated. Immediately after ionization, the process of electron-hole recombination will occur, as will electron transport. Electron mobility in SiO_2 at room temperature is approximately 20 cm^2/V-s while hole mobility is approximately 2×10^{-5} cm^2/V-s. Because of the applied voltage, any electrons that do not undergo recombination will be swept to the gate and removed in picoseconds, leaving behind the less mobile holes. These holes will begin a transport process toward the Si-SiO_2 interface. Some holes will pass into the silicon while others will become trapped at defect centers very near the interface of the gate oxide and the bulk silicon (Srour, 1982; Grover, 1984).

In the case of the n-channel device, the trapped positive charge will continue to build up and make it easier to create the n-type channel (inversion layer). This effect will lower the threshold voltage, as illustrated in Figure 2. The reversal of the threshold shift shown in the figure is caused by the saturation of the surface traps and the generation of electron states at the Si-SiO_2 interface that appear with higher levels of gamma radiation (above 5×10^5 rads).

In the case of the corresponding p-channel device, the build-up will make it more difficult to create an inversion layer in an enhancement mode p-channel transistor. The effect on the p-channel threshold is also shown in Figure 2.

Latch -Up

A four-layer (pnpn) parasitic conduction path exists in bulk CMOS devices (Schroeder et al., 1980). The four-layer path operates like an SCR. This path can be activated by photocurrents generated by ionizing radiation. The resulting low-impedance, high-current path from V_{DD} to ground is known as latch-up. Latch-up has been eliminated by growing an epitaxial layer of lightly doped n^- material on the original heavily doped n^+ starting material.

The epi material provides a low resistivity shunt resistor to prohibit the four-layer device from sustaining latch-up. Figure 3 shows a cross section of a bulk epi CMOS structure and a model of the parasitic SCR device. The use of epi starting material is an effective method of preventing latch-up only if it is the correct thickness. If the epi layer is too thick, it is ineffective because its impedance will be too high.

Although it is possible to simulate device performance, the proper method to determine the effects of transient radiation on a device is to operate it in the environment under that conditon. When dealing with survivability and vulnerability, very few device manufacturers have information on the transient radiation response of their rad-tolerant circuits.

Single-Event Effects

Single-event immunity has recently become a major concern for satellite and space-bound systems with memory devices, that is, RAMs. A single high-energy particle can strike a critical node and leave behind an ionized track. If the particle hits the drain of the off p-channel device, the resulting voltage transient may be sufficient to cause the inverter in the other half of the memory cell to change state. Because the output of this changed inverter is fed back to the other inverter (the side originally hit), the memory cell changes state. This event is referred to as a soft error (upset) and is measured in terms of errors/bit-day.

The addition of cross-coupled resistors in the memory cell inserts an RC time constant into the transient such that the deposited charge is swept out before the memory cell can react to the voltage transient. This has eliminated upset in bulk CMOS static RAMs from high-energy particle impacts (Andrews, et al., 1982).

Latch-up in bulk CMOS can also be induced by high-

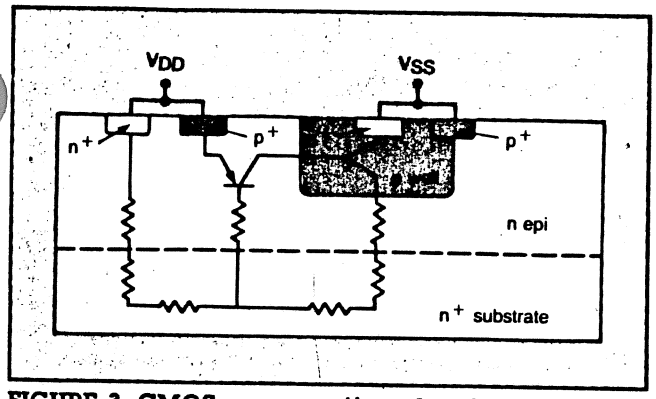


FIGURE 3. CMOS cross-section showing parasitic SCR structure.

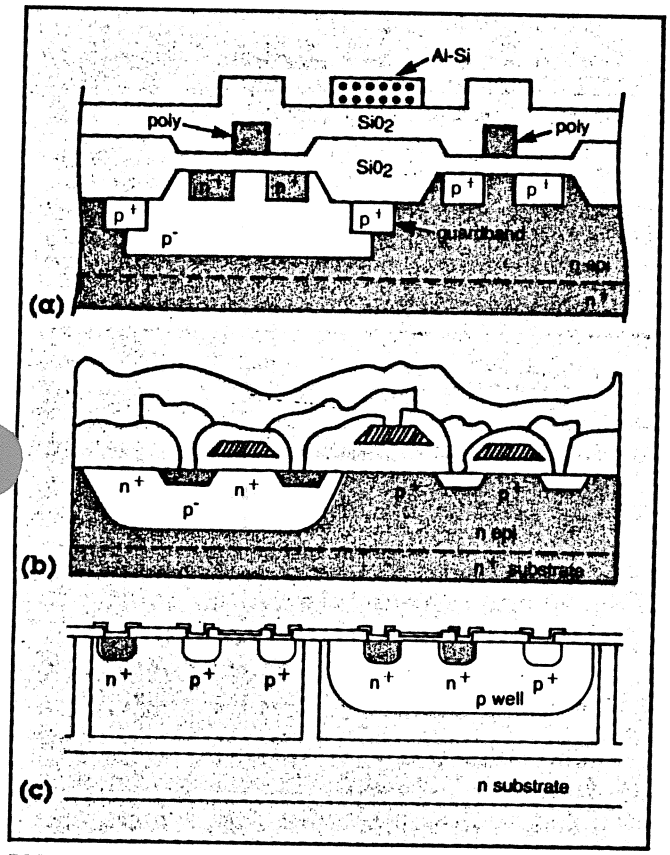


FIGURE 4. CMOS cross-sections showing guardbands (a) and implanted isolation (c).

energy particles. If a particle has enough energy, the ionized track left behind could be long enough to punch through the p well and contact the substrate.

Radiation Hardening

In general, hardened devices will not fail, even in typically high radiation environments. Radiation hardness can be achieved through several means. Gate oxide thickness has a direct bearing on device hardness. By reducing the gate oxide thickness, the volume that can generate carriers due to impinging radiation is reduced. As a result, the amount of trapped charge can be reduced, reducing the amount of threshold shift of the n-channel and p-channel devices. However, the thinner gate oxide also gives a higher gate capacitance. Also, if the gate oxide thickness is reduced too much, then breakdown of the oxide can become a potential failure mechanism.

Large photocurrents can cause loss of stored data, and if high enough, latch-up. By making the p well as small as possible, one can reduce the charge collection area and therefore reduce the photocurrent. Also, by beefing up the metal lines, larger photocurrents can be handled with the same or less voltage drop seen from V_{DD} to V_{SS}.

Transistor sizing is often used to compensate for threshold shifts and photocurrent generation. It is possible to size the p-channel and n-channel transistors so as to balance the carriers generated during a transient radiation pulse. That is, if equal numbers of holes and electrons are generated, then recombination is more likely to occur. This is usually difficult to accomplish while maintaining the correct drive capability for each device. It tends to work in the opposite direction.

Radiation-hardening of CMOS devices involves special design, fabrication, and screening and quality control. Radiation hardening at Harris Semiconductor is accomplished in two ways. The first is through specific design and processing techniques while the second method relies solely on processing techniques. The first process involves designing the part to be rad-hard from the ground up (Figure 4a). Hardness is obtained by the insertion of the p^+ guardbands shown in the figure. During irradiation, a parasitic channel can be formed in the p well between the n^+ source and the n^- substrate, causing increased leakage current. The guardband prevents this from happening. Therefore, every n-channel device requires a guardband. The guardbands are included during the design phase of a circuit. Additional processing techniques are implemented to harden the gate and field oxides (Sanders, 1977). The second hardening technique does not require guardbands (Figure 4b). It nonetheless provides the same hardness levels and the same low post-radiation leakage current as the guardband process. The removal of the guardbands frees up real estate on the chip, which leads to a higher packing density. A second and more important feature is the fact that standard CMOS layouts can be hardened without the overhead of redesign to include the guardbands.

At this time, there are two process technologies used by Harris Semiconductor in the production of rad-hard CMOS ICs. These are identified by their starting material: bulk silicon and silicon on insulator (SOI). SOI starting material is harder to produce than bulk silicon; however, CMOS/SOI does not latch up. Latch-up in bulk silicon must be eliminated through the use of epitaxial starting material. The transient upset level of CMOS/SOI is generally better than that of bulk silicon. On the other hand, the most common SOI configuration, silicon on sapphire, usually leads to higher power consumption than found in bulk silicon devices.

An alternative SOI technology now being developed at Harris is called SIMOX, for silicon isolated by implanted oxygen. It will not latch up, has the potential for increased speed and better packing density, and achieves the goals of increased hardness against transient radiation and single-event effects. This process requires oxygen atoms to be implanted a specified distance below the surface of the silicon. The oxygen atoms form a silicon dioxide layer that becomes a buried insulator. This configuration eliminates a

Manufacturer	Process	Part number	Date code	Test type	Radiation source	Device dose rate (rad/s)	Results
Harris (Standard CMOS)	SAJI IV	MD80C86	8520	Dynamic	Co-60	80	6 devices tested; first functional failure at 14.9 krads; high at 19.6 krads; average 16.4 krads
Harris (Rad-hard CMOS)	SAJI IV	HS-80C86RH	8545	Dynamic	Co-60	80	Meets data sheet at post 100 krads; functional at >1 Mrad
Intel (Standard nMOS)	HMOS II	8086	8125	Dynamic	Co-60	50	8 devices tested; first functional failure at 9.3 krads; all failed by 16.2 krads except one unit that failed at 25.9 krads
Intel (Standard CMOS)	CHMOS III	MC80C31 (8085 μcontroller)	(unknown)	Dynamic	Ce	2.78	12 devices tested; first functional failure at 580 krads; average 640 krads
Harris (Rad-hard CMOS)	SAJI IV	HS-80C85RH	8515	Dynamic	Co-60	80	Meets data sheet at post 100 krads; functional at >1 Mrad
Intel (Standard CMOS)	CHMOS III	MD51C87	(unknown)	Iterative	(unknown)	(unknown)	5 devices tested; first functional failure at 360 krads; average 496 krads
Integrated Device Technology (Standard CMOS)	CEMOS	IDT 6167 (16K×1 RAM)	(unknown)	Iterative	Co-60	4.17	10 devices tested; 2 failed at 3 krads; 6 failed at 6 krads; all failed at 10 krads
Harris (Rad-hard CMOS)	SAJI V	HS-65262RH	8530	Dynamic	Co-60	80	10 devices tested; meet data sheet spec at post 200 krads; functional at >1 Mrad

TABLE 2. Some device testing results.

large portion of the pn junction depletion region, which is the charge collection region for transient-induced photocurrents. Also, by additional process steps for lateral isolation, latch-up is eliminated because four-layer SCR paths no longer exist. An improvement in single-event effects will also be seen because the funneling and charge collection shown earlier cannot happen through the buried oxide layer. SOI has all the advantages of SOS without the problems associated with growing sapphire and then growing silicon on top of it.

Rad-Hard versus Rad-Tolerant

Key process and dimensional parameters are normally monitored in a radiation-hard manufacturing sequence. Dimensional parameters include gate oxide thickness, gate oxide tolerance, field oxide thickness and tolerance, chip topology (mask changes), and polysilicon resistor design values. Process parameters include doping concentrations, all chemical process steps, methods of oxide growth, gate threshold voltage, and post-gate thermal processes. Unless the manufacturer is willing to control these parameters, radiation tolerance differences between lots can occur.

Standard (not rad-hard) devices are always designed to meet or exceed certain electrical specifications. Manufacturers, however, in seeking ways to enhance yields and lower costs often change products in ways that do not affect the customer and the data sheet specification. Since radiation tolerance is not typically monitored on standard products, sufficient lot variation can exist to wreak havoc with system radiation specifications.

Table 2 contains total dose information for some similar devices. It is important to note that the non-hardened devices were tested to functional failure while the rad-hard devices were tested to parametric limits. Where available, the dose rate and type of radiating source is also given.

Parameter	Standard CMOS	Hardened CMOS
Neutron fluence (N/cm^2)	$>10^{15}$	$>10^{15}$
Total dose [rad (Si)]	$1-3\times10^3$	10^5-10^6
Latch-up dose rate (rad/s)	10^9	(none)
Upset dose rate (rad/s)	5×10^7	3×10^8

TABLE 3. Radiation resistance of standard and hardened CMOS.

Radiation hardness assurance level	Total dose [rad (Si)]	Neutron fluence (N/cm^2)
/	—	—
M	3×10^3	2×10^{12}
D	10^4	2×10^{12}
R	10^5	2×10^{12}
H	10^6	2×10^{12}

TABLE 4. Government requirements.

Table 3 summarizes radiation effects on standard versus hardened CMOS. From these figures it is clear that hardened CMOS is superior to standard bulk CMOS in the critical areas of total dose hardness and immunity to latch-up.

Rad-tolerant devices can be an effective option to using more expensive rad-hard products with high levels of radi-

ation survivability. For many tactical military programs with "man-rated" system requirements or for low Earth orbit satellites this can be true. However, the test data must be understood and the system requirements clearly defined in the detailed customer specification. Because of the complexity of LSI devices, many laboratories make functional rather than parametric measurements. In other words, the device is tested to the point of catastrophic failure, or when it is no longer able to perform its function. Unless the failure mode is clearly defined, it will be difficult to make adequate comparisons between similar devices from different manufacturers. Other things that must be understood when using rad-tolerant parts are the dose rate when tested, test condition, and test method.

The dose rate used can be critical in determining the hardness of a device. If the device is tested at a low dose rate, it could anneal (self-heal) almost at the same rate that it is irradiated. If the device is tested iteratively, that is, removed from the chamber periodically, the results could be even more dramatic. MIL-STD-883C, Method 1019, Steady State Total Dose Irradiation Procedure allows a dose rate variation of 1.67-2500 rads/s. This wide margin can yield tremendous differences when comparing similar devices. The government has recognized this problem and will correct it by amending the procedure to permit a rate range of 100-300 rads/s.

In comparing data, the test conditions must be understood. For example, were the devices biased or unbiased? Was the temperature allowed to rise? If the devices are unbiased during irradiation, they could withstand significantly higher levels of radiation than if they were biased. In fact, if a nuclear event could be detected and the equipment shut down soon enough, system survivability would be enhanced. Temperature during irradiation should also be controlled. Typically, the temperature will rise while a device is exposed to radiation. This rise will allow the device under test to anneal at a faster rate and tend to make the test results appear to be better than they actually are.

Finally, how the device is tested is very important to the results. There are two methods of performing radiation tests: iterative and in-situ. In the iterative method the device is irradiated to a particular level then physically removed from the chamber for electrical measurements. If the device is still good, it is then placed back into the chamber for another incremental dose. This process continues until the device fails functionally or parametric limits are reached. When tested in-situ, the device is monitored electrically while it is being irradiated. Some argue that this is the best way of testing a device, since it more closely mirrors the way it would fail under actual conditions. Parametric measurements, however, are more difficult to make in-situ.

Government Requirements

The DoD is engaged in a major effort to increase the radiation resistance of existing and new military electronics systems. MIL-M-38510F now lists four levels of radiation hardness for JAN qualified devices. These are defined in Table 4. Pass/fail criteria will be "as defined per detailed specification." The test methods used are defined by the new Group E qualification chart in Method 5005 of MIL-STD-883C. Group E qualification testing will be used to qualify individual lots on a sample basis to determine if the devices meet the specified levels of radiation listed in the table.

Although transient radiation and single-event upset testing are not presently required, they probably will be before long. DoD has also published some new guideline documents dealing with this area. Two excellent references that can be used in designing a radiation resistant system are MIL-HDBK-279 and MIL-HDBK-280. These handbooks deal with total dose and neutron hardness assurance guidelines, respectively, for semiconductor devices and microcircuits.

Conclusions

Although Harris has been engaged in selling rad-hard devices for some time, we recognize the need for rad-tolerant devices as well. Our Standard Products Division is now engaged in determining the radiation-tolerance of its devices. Once this effort is completed, we will be publishing the results and offering a rad-tolerant product line. Our combined product lines will offer a full spectrum of devices to meet all the categories listed in MIL-STD-38510F. □

References

Andrews, J.L., J.E. Schroeder, B.L. Gingerich, W.A. Kolanski, R. Koga, and S.E. Diehl. December 1982. "Single Event Upset Error Immune CMOS RAM," *IEEE Transactions on Nuclear Science*, Vol. NS-29.

Grover, J.E. 1984 "Basic Radiation Effects in Electronics Technology," *IEEE Tutorial Short Course on Radiation Effects.*

Sanders, T.J. December 1977. "CMOS Hardness Assurance Through Process Controls and Optimized Design Procedures," *IEEE Transactions on Nuclear Science*, Vol. NS-24.

Schroeder, J.E., A. Ocha, Jr., and P.V. Dressendorfer. December 1980. "Latch-up Elimination in Bulk CMOS LSI Circuits," *IEEE Transaction on Nuclear Science*, Vol. NS-27.

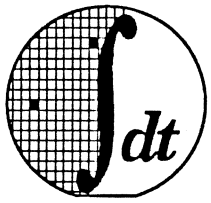
Srour, J. "Basic Mechanisms of Radiation Effects on Electronic Materials, Devices, and Integrated Circuits," *IEEE 1982 Annual Conference on Nuclear and Space Radiation Effects.*

Tirado, J.S. 1985. "Radiation Capability in Microprocessor-Based Systems," *Government Microcircuit Applications Conference.*

About the Authors

Gordon P. Ansell is the lead applications engineer for data sheet products with Harris Semiconductor's Custom Integrated Circuits Division. Prior to joining Harris in 1984, Ansell was the director of electronics engineering for Mercy Hospital in Miami, FL. He holds a B.S. degree in biomedical engineering from the University of Illinois, Chicago, and an M.S.E. degree from Washington University, St. Louis, MO.

Joe S. Tirado is the manager for business development in military and high-reliability programs with Harris Semiconductor's Custom Integrated Circuits Division. Prior to joining Harris, Joe was an officer in the U.S. Air Force and worked at the Electronics Systems Division, Air Force Weapons Laboratory, Test and Applications Center, and other assignments. Tirado earned the B.S.E.E. degree from the University of Wyoming and the M.B.A. from New Mexico Highlands University.



Integrated Device Technology, Inc.

1991
STATIC RAM
DATA BOOK

3236 Scott Boulevard, Santa Clara, California 95054
Telephone: (408) 727-6116 • TWX: 910-338-2070 • FAX: (408) 492-8674
Printed in U.S.A.

NEW HAMPSHIRE

IDT
(Eastern Headquarters)
#2 Westboro Business Park
200 Friberg Pkwy.,
Ste. 4002
Westboro, MA 01581
(508) 898-9266

NEW JERSEY

IDT
(NE Regional Office)
One Greentree Centre,
Ste. 202
Marlton, NJ 08053
(609) 596-8668

SJ Associates
Mt. Laurel, NJ
(609) 866-1234

NEW MEXICO

Western High Tech Mktg.
Albuquerque, NM
(505) 884-2256

NEW YORK

IDT
(NE Regional Office)
250 Mill St., Ste.107
Rochester, NY 14614
(716) 546-4880

Quality Components
Buffalo, NY
(716) 837-5430

Quality Components
Manlius, NY
(315) 682-8885

SJ Associates
Rockville Centre, NY
(516) 536-4242

NORTH CAROLINA

Tingen Technical Sales
Raleigh, NC
(919) 870-6670

OHIO

Norm Case Associates
Rocky River, OH
(216) 333-0400

OKLAHOMA

IDT
(Central Headquarters)
1375 E. Woodfield Rd.,
Ste. 380
Schaumburg, IL 60173
(708) 517-1262

OREGON

Westerberg & Associates
Portland, OR
(503) 620-1931

PENNSYLVANIA (WESTERN)

Norm Case Associates
Rocky River, OH
(216) 333-0400

PENNSYLVANIA (EASTERN)

SJ Associates
Rockville Centre, NY
(516) 536-4242

RHODE ISLAND

IDT
(Eastern Headquarters)
#2 Westboro Business Park
200 Friberg Pkwy.,
Ste. 4002
Westboro, MA 01581
(508) 898-9266

SOUTH CAROLINA

IDT
(SE Regional Office)
1413 S. Patrick Dr., Ste. 10
Indian Harbor Beach, FL
32937
(407) 773-3412

TEXAS

IDT
(S. Central Regional Office)
6034 W. Courtyard Dr.,
Ste. 305-48
Austin, TX 78730
(512) 338-2440

IDT
(S. Central Regional Office)
14285 Midway Rd., Ste. 100
Dallas, TX 75244
(214) 490-6167

UTAH

Anderson Associates
Bountiful, UT
(801) 292-8991

VERMONT

IDT
(Eastern Headquarters)
#2 Westboro Business Park
200 Friberg Pkwy.,
Ste. 4002
Westboro, MA 01581
(508) 898-9266

VIRGINIA

IDT
(NE Regional Office)
428 Fourth St., Ste. 6
Annapolis, MD 21403
(301) 858-5423

WASHINGTON

Westerberg & Associates
Bellevue, WA
(206) 453-8881

IDT
(NW Regional Office)
7981 168th Ave. N.E.,
Ste. 32
Redmond, WA 98052
(206) 881-5966

WEST VIRGINIA

Norm Case Associates
Rocky River, OH
(216) 333-0400

WISCONSIN

Synmark Sales
Park Ridge, IL
(708) 390-9696

WYOMING

Thorson Rocky Mountain
Englewood, CO
(303) 799-3435

IDT TECHNICAL CENTERS

Integrated Device Technology
(Western Headquarters)
2972 Stender Way
Santa Clara, CA 95054
(408) 492-8350

Integrated Device Technology
(Southwestern Regional Office)
6 Jenner Drive, Suite 100
Irvine, CA 92718
(714) 727-4438

Integrated Device Technology
(South Central Regional Office)
14285 Midway Road, Suite 100
Dallas, TX 75244
(214) 490-6167

Integrated Device Technology
(Eastern Headquarters)
#2 Westboro Business Park
200 Friberg Parkway, Suite 4002
Westboro, MA 01581
(508) 898-9266

INTEGRATED DEVICE TECHNOLOGY, INC.
(European Headquarters/Northern Europe Regional Office)
21 The Crescent
Leatherhead
Surrey, UK KT228DY
Tel.: 44-372-377375

AUTHORIZED DISTRIBUTORS

HALL-MARK ELECTRONICS | **HAMILTON/AVNET** | **INSIGHT ELECTRONICS** | **VANTAGE COMPONENTS** | **ZENTRONICS**

Contact your local office.

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiati Tolerant/Enhanced versions of all product types (some spe grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K X 8 BIT)

IDT6116SA
IDT6116LA

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed
  - — Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power operation
  - — IDT6116SA
    Active: 180mW (typ.)
    Standby: 100µW (typ.)
  - — IDT6116LA
    Active: 160mW (typ.)
    Standby: 20µW (typ.)
- Battery backup operation - 2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK
- Military product compliant to MIL-STD-833, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology - CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

Access times as fast as 15ns are available with maxim power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20µW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

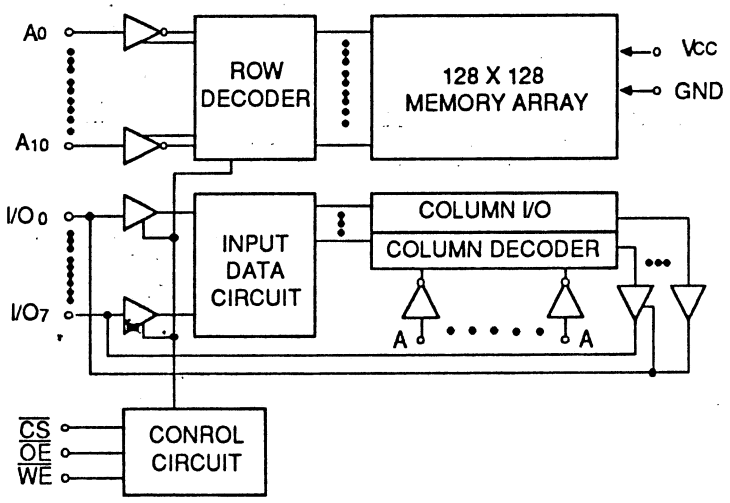
All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

5

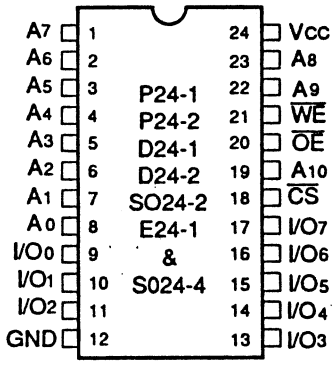
FUNCTIONAL BLOCK DIAGRAM



2954 drw 02

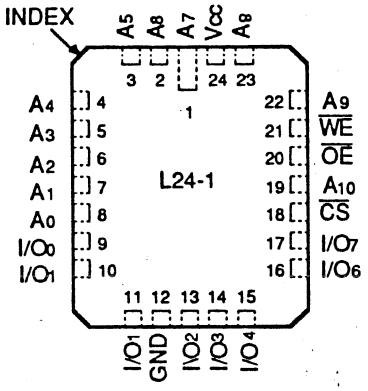
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



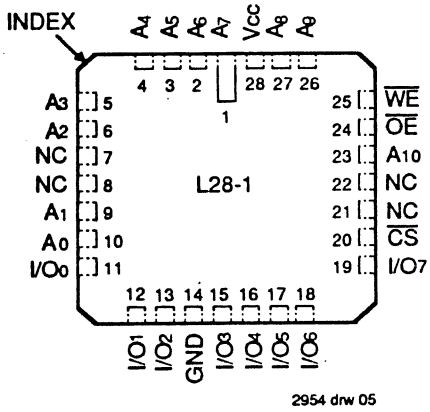
2954 drw 01

DIP/SOIC/CERPACK/SOJ
TOP VIEW



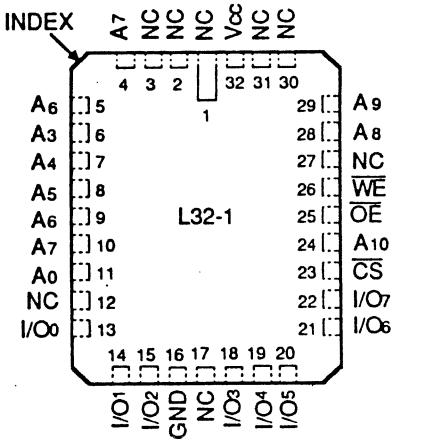
2954 drw 03

24-PIN LCC
TOP VIEW



2954 drw 05

28-PIN LCC
TOP VIEW



2954 drw 04

32-PIN LCC
TOP VIEW

PIN NAMES

A_0- A_{10}	Address	$\overline{WE}$	Write Enable
I/O_0 - I/O_7	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
Vcc	Power		

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
T_A	Operating Temperature	0 to + 70	-55 to + 125	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	-65 to + 135	°C
T_{STG}	Storage Temperature	-55 to + 125	-65 to + 150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V
C_L	Output Load	—	—	30	pF

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		IDT6116SA Min.	IDT6116SA Typ.(1)	IDT6116SA Max.	IDT6116LA Min.	IDT6116LA Typ.(1)	IDT6116LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	10	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, + 25°C ambient.

5

AC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA15(2) 6116LA15(2) Com'l.	6116SA15(2) 6116LA15(2) Mil.	6116SA20 6116LA20 Com'l.	6116SA20 6116LA20 Mil.	6116SA25 6116LA25 Com'l.	6116SA25 6116LA25 Mil.	6116SA35 6116LA35 Com'l.	6116SA35 6116LA35 Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	125	—	110	130	100	110	80	90	mA
		LA	115	—	100	120	90	105	75	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}

AC ELECTRICAL CHARACTERISTICS [1] (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA45 6116LA45		6116SA55[3] 6116LA55[3]		6116SA70[3] 6116LA70[3]		6116SA90[3] 6116LA90[3]		6116SA120[3] 6116LA120[3]		6116SA150[3] 6116LA150[3]		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	100	100	—	100	—	100	—	100	—	1005	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}

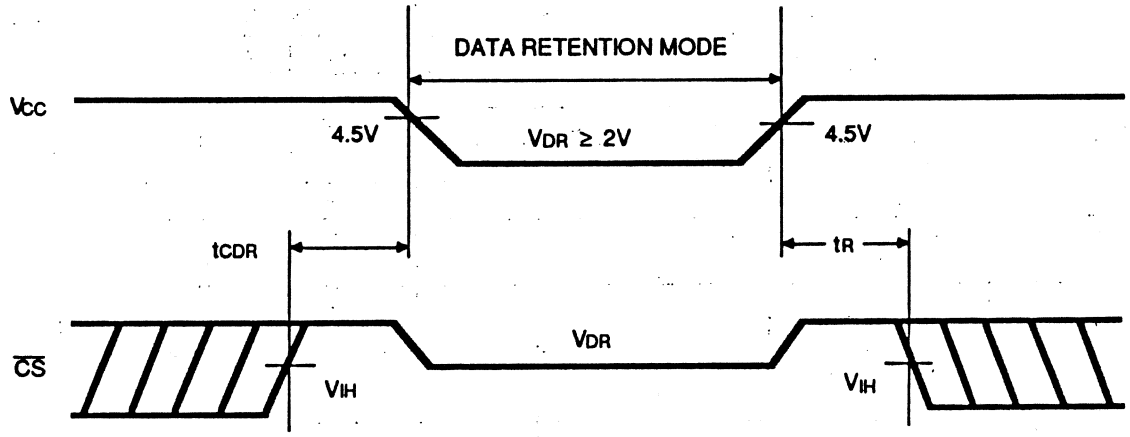
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.[1] Vcc @ 2.0V	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC}	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CCR}[3]	Data Deselect to Data Retention Time	V_{IN} ≥ V_{HC} or ≤ V_{LC}		—	0	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = + 25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2954 drw 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

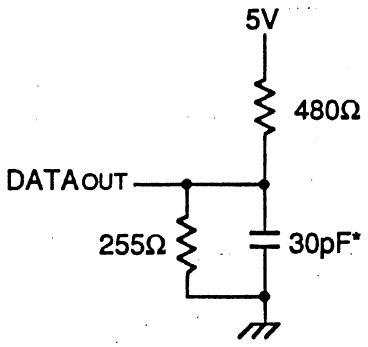


Figure 1. Output Load

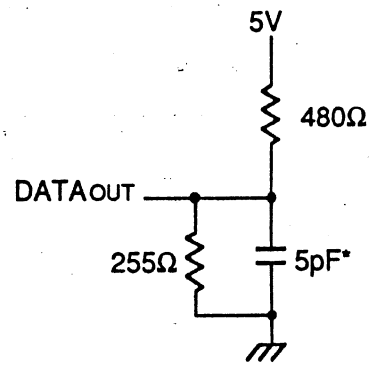


Figure 2. Output Load (for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ, tOW)

2954 drw 08

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

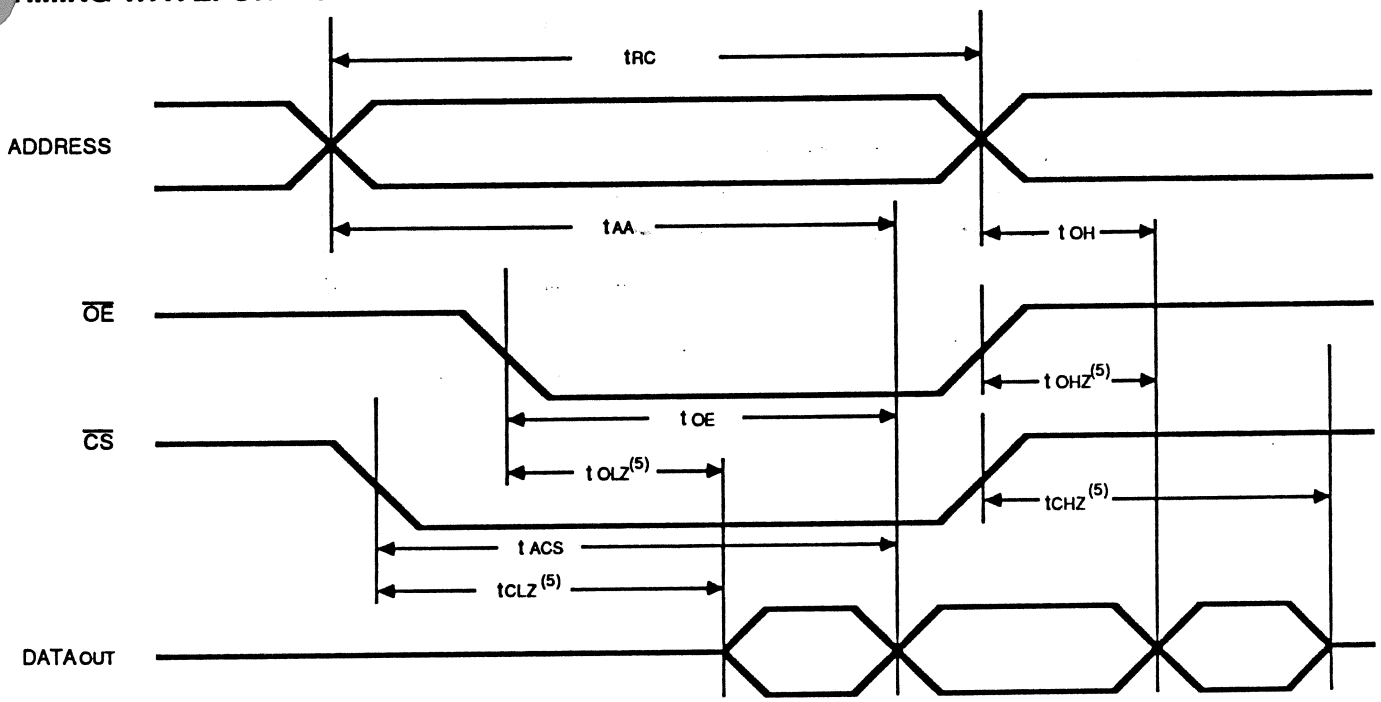
Symbol	Parameter	6116SA15[1] 6116LA15[1]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
tCLZ	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
tOLZ	Output Enable to Output in Low Z[3]	0	—	0	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High Z[3]	—	10	—	11	—	12	—	15	ns
tOHZ	Output Disable to Output in High Z[3]	—	8	—	8	—	10	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	5	—	5	—	ns

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
tRC	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tAA	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
tACS	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
tCLZ	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
tOLZ	Output Enable to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High Z[3]	—	20	—	30	—	35	—	40	—	40	—	40	ns
tOHZ	Output Disable to Output in High Z[3]	—	15	—	30	—	35	—	40	—	40	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0°C to + 70°C temperature range only.
2. -55°C to + 125°C temperature range only.
3. This parameter guaranteed but not tested.

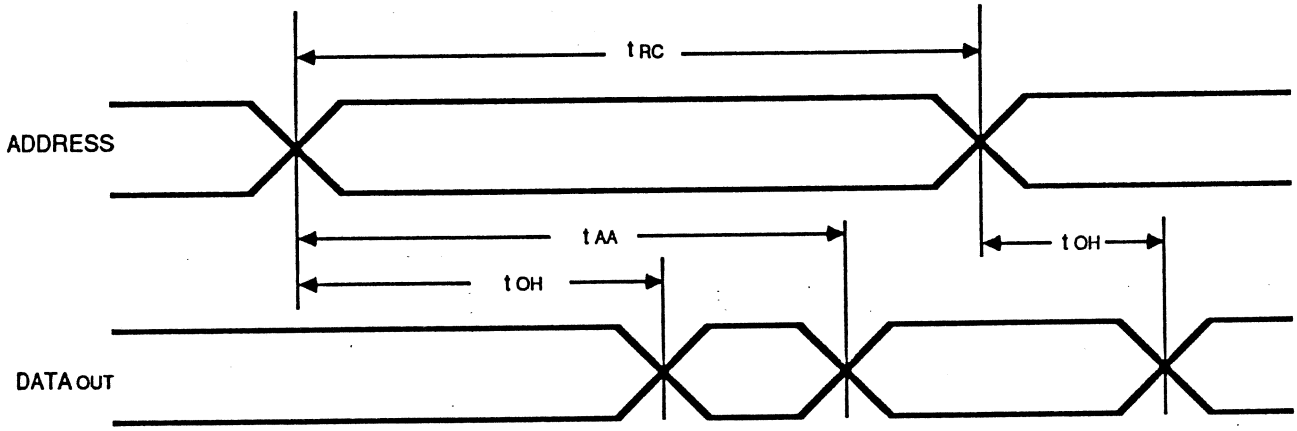
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2954 drw 09

5

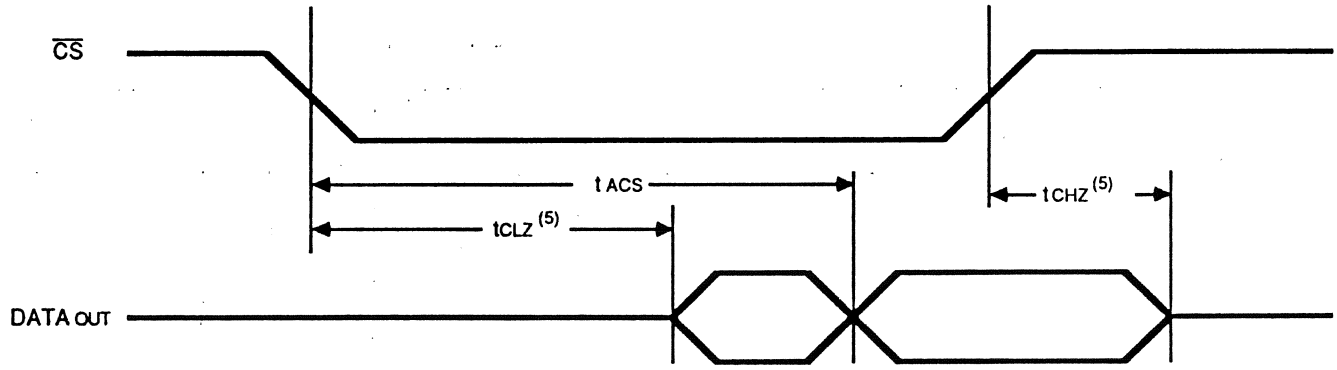
TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



2954 drw 10

NOTE:
1 $\overline{WE}$ is high for read cycle.
2 Device is continously selected, $\overline{CS}$ = VIL.
3 Address valid prior to or coincident with $\overline{CS}$ transition low.
4 $\overline{OE}$ = VIL.
5 Transition is measured ±500mV from steady state with 5pF load (including scope and jig.)

TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



2954 drw 11

NOTE:
1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig.)

AC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15(1) 6116LA15(1)		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tCW	Chip Select to End of Write	13	—	15	—	17	—	25	—	ns
tAW	Address Valid to End of Write	14	—	15	—	17	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tOHZ	Output Disable to Output in High Z(3)	—	8	—	8	—	10	—	13	ns
tWHZ	Write to Output in High Z(3)	—	7	—	8	—	16	—	20	ns
tDW	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
tDH	Data Hold from Write Time(4)	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write(3,4)	0	—	0	—	0	—	0	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

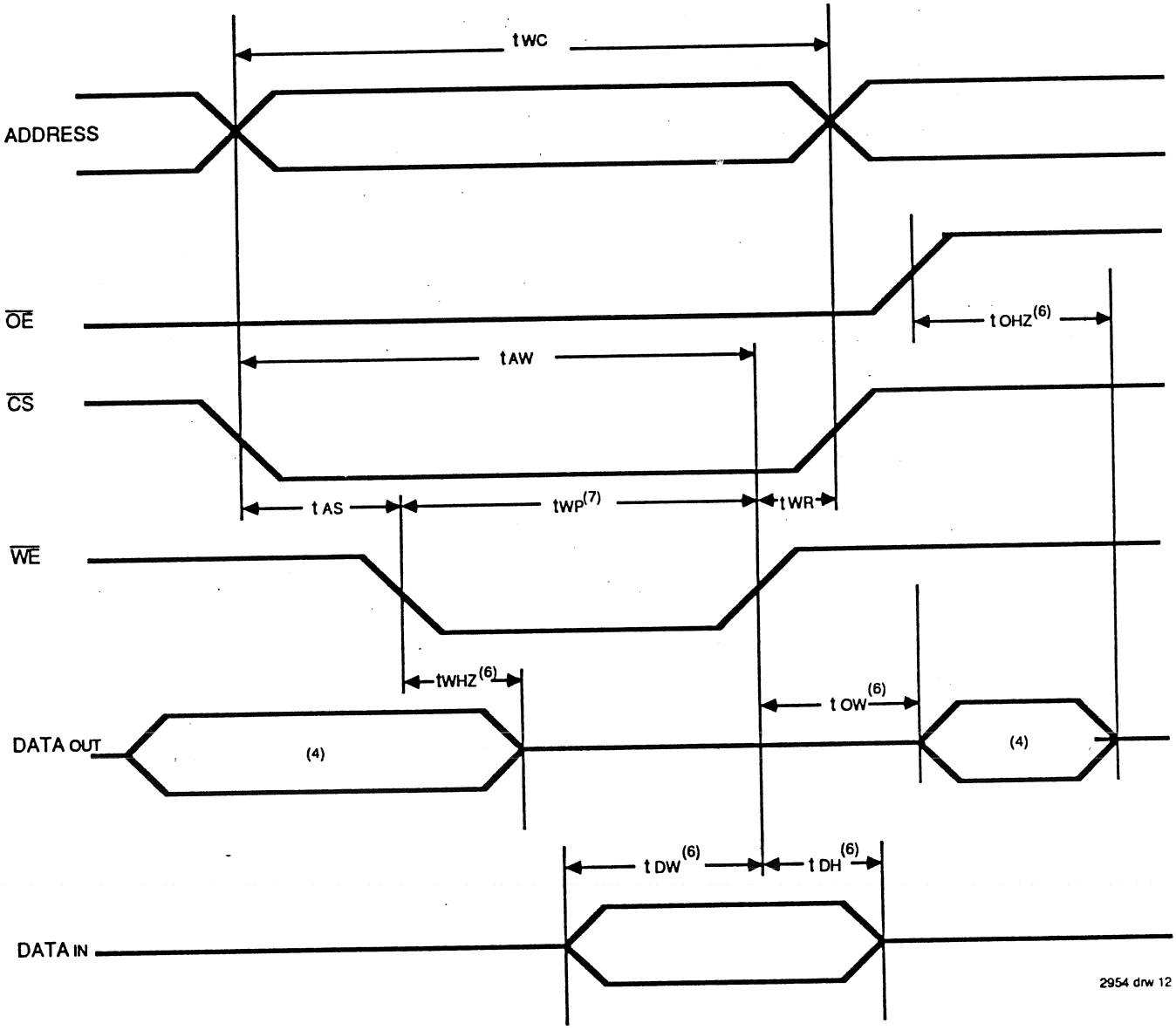
AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE														
tWC	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tCW	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
tAW	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
tAS	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
tWP	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
tWR	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOHZ	Output Disable to Output in High Z[3]	—	25	—	30	—	35	—	40	—	40	—	40	ns
tWHZ	Write to Output in High Z[3]	—	25	—	30	—	35	—	40	—	40	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time[4]	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOW	Output Active from End of Write[3,4]	0	—	0	—	0	—	0	—	0	—	0	—	ns

5

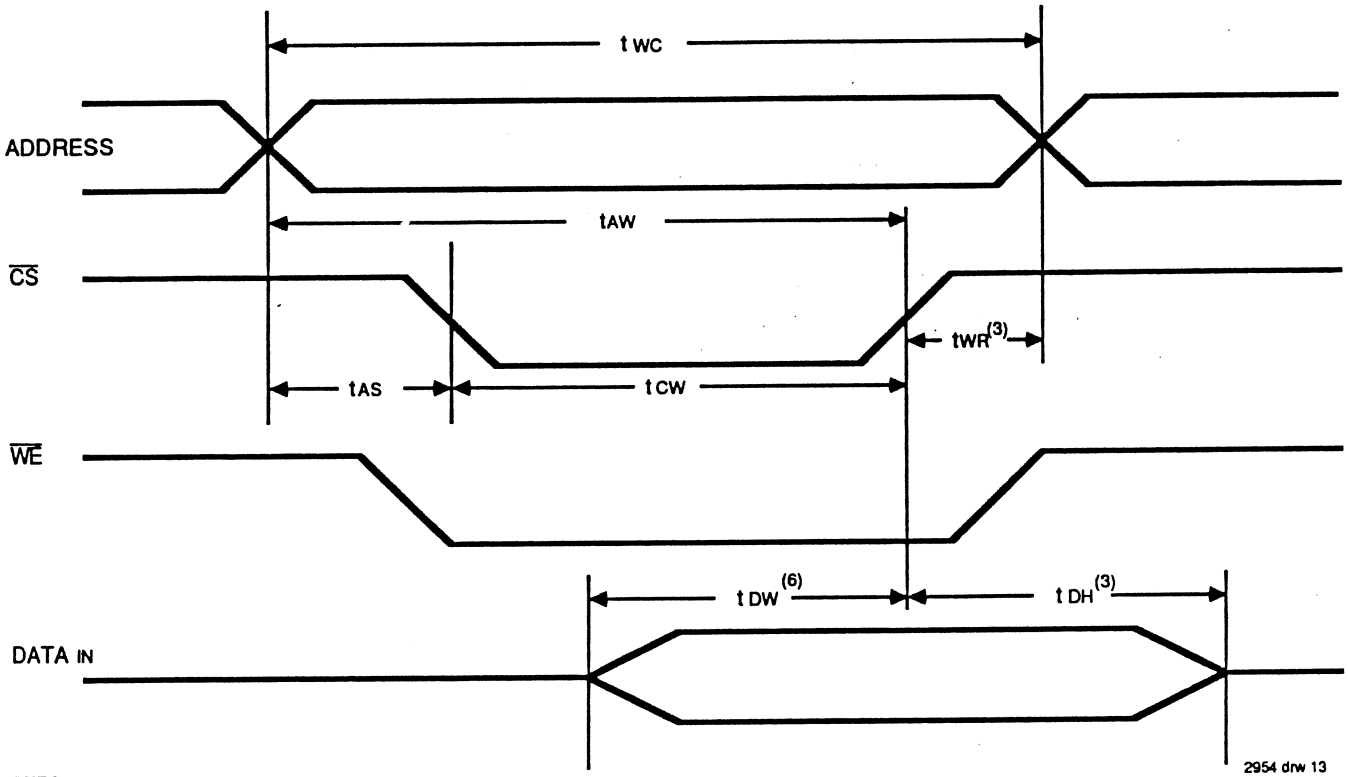
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be a short as the specified tWP.

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state wih a 5pF load (includng scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be a short as the specified tWP.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High Z
Read	L	L	H	DATAOUT
Read	L	H	H	High Z
Write	L	X	L	DATAIN

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

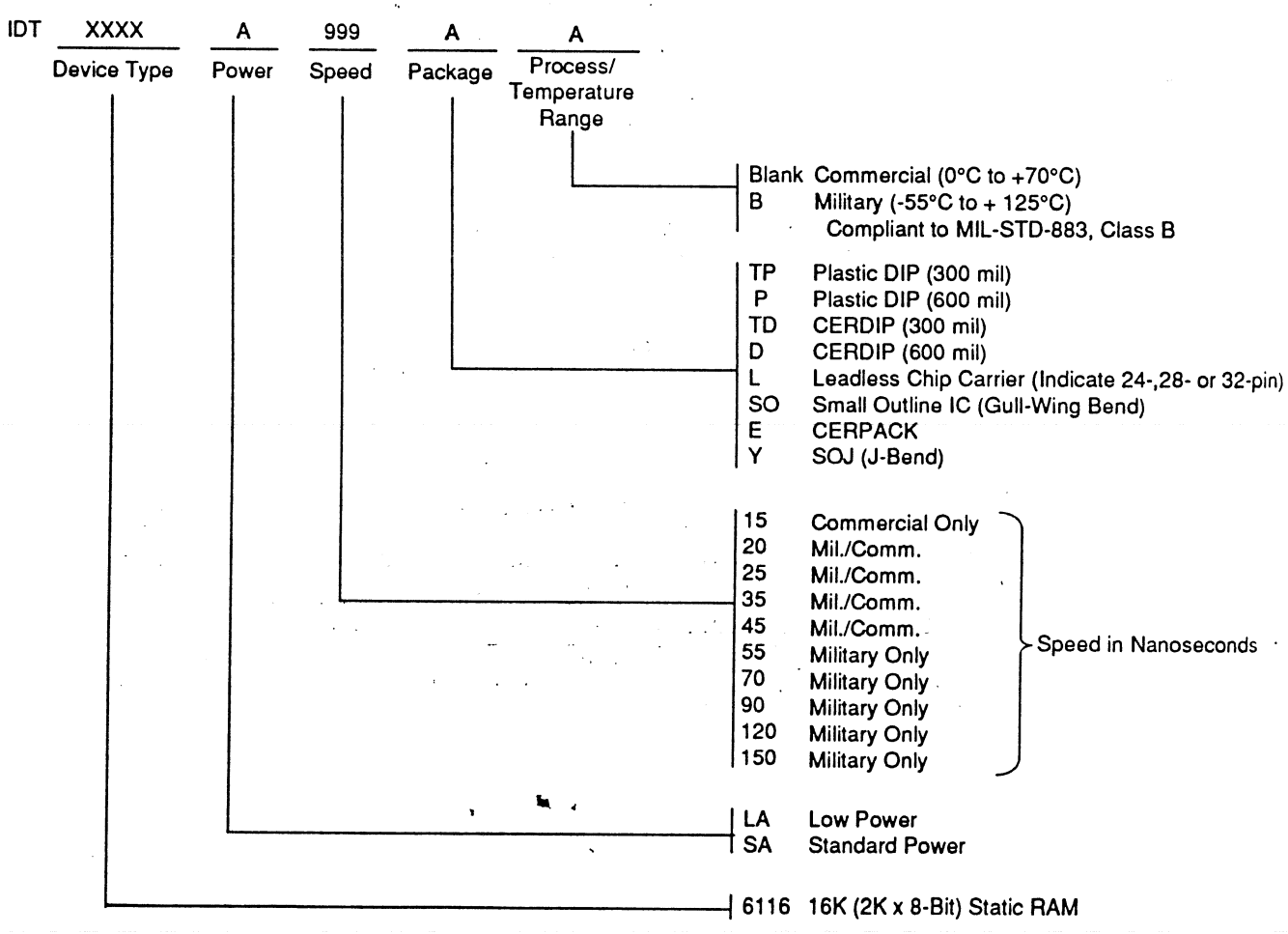
Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

THERMAL RESISTANCE (Typical)

Package	Pin Count	ΦJA	ΦJC	Unit
300 Mil Plastic DIP	24	54-58	28-32	°C/ WATT
600 Mil Plastic DIP	24	53-56	25-30	
300 Mil CERDIP	24	48-52	24-28	
600 Mil CERDIP	24	50-55	17-25	
Flatpack	24	85-90	24-28	
LCC	24	85-110	30-45	
LCC	28	85-90	28-35	
LCC	32	80-90	25-35	
SOIC, SOJ	24	45-70	25-30	

ORDERING INFORMATION



2954 drw 14

HARRIS
SEMICONDUCTOR

SPACE PRODUCTS NEWS

VOLUME 1, NUMBER 4, 1992
A QUARTERLY PUBLICATION
OCTOBER – DECEMBER

Directions in Space

By Scott Moody

Quality ... Delivery ... Price ...

I'm sure many of you can remember when the joke went, "Quality, Delivery, Price: Pick Two." While this joke has long been passé in many commercial markets, the same has not been true of many within the space supplier market. Not so of Harris' Space Products Operation, where we are out to bring the best commercial practices to our customers in the space community. That means being able to deliver product quickly, *designed and manufactured using advanced technologies* to meet the harsh environments of space, and to do it at a continually lower component and system cost. But let's not forget a fourth and equally important element — product that provides value to the overall system design.

In our previous newsletters, we've highlighted two of these four critical elements, those being delivery and products. For example, in the delivery area, you can now buy our standard product offering directly from our distributors, Hamilton/Avnet and Arrow Electronics. That's right; off-the-shelf, next day delivery of radiation hardened space qualified product, something your counterparts in the commercial markets have enjoyed for years! In the product area, we've highlighted many of our new rad hard products coming out over the next year — forty-eight, to be exact. By listening to you, we have established an aggressive new product plan that allows you to design with radiation hardened versions of your favorite commercial products.

When it comes to reduced costs, you'll find Space Products leading the charge with such initiatives as lower minimum quantities, low cost sample availability and several product

continued on page 5

Radiation and Integrated Circuits

By Ken Ports

When an integrated circuit is placed in a radiative environment, it may be affected by the radiation and its performance may be compromised. The tolerance a device has for a given type of radiative exposure, its "radiation hardness," is not an intrinsic property of an IC. Unless hardness is specifically designed into a device's fabrication process and circuitry, the resulting part generally will be sensitive to radiation and upon exposure will ultimately malfunction or fail.

For satellite applications, the two types of radiation of greatest concern are radiation which produces cumulative degradation of performance (total dose effect) and transient radiative events which generate short signal pulses within a circuit and upset its operation. In each case, it is important to recognize the implications of the planned system application and to specify the component ICs for that environment accordingly.

Cumulative degradation of circuit performance is caused by radiation which produces a charging effect or by radiation which produces physical damage to the IC material. The charging

continued on page 4

Radiation and Integrated Circuits

continued from page 1

effect is due to high energy photons; the physical damage, to neutrons and other particles.

High energy photons (gamma rays and x-rays) generate a "wake" of positive and negative charges which rapidly recombine and disappear when they are in a conducting medium. In the insulating portions of an IC, however, the charges tend to stay separated, move about, and ultimately disappear into the silicon or become trapped, producing a charging effect. This undesired electrical charge shifts the operating point of nearby transistors and ultimately will degrade circuit performance or cause general failure of the part. Devices which reside at the surface of the silicon, such as in MOS or CMOS technologies, are those most affected by this type of radiation.

IC tolerance for total dose radiation can be improved by using very thin insulators, by fabricating the insulators with special processing techniques to minimize the charging effects, and by designing circuits which are less sensitive to drift in the operating points of their component transistors.

Unlike gamma and x-rays, high energy neutrons cause systematic physical damage. While neutrons have relatively little effect in insulators, in silicon they displace atoms from their lattice sites, reduce the minority carrier lifetime and cause electrical leakage within transistors and diodes. Devices where the action occurs inside the silicon, such as bipolar transistors and diodes, are those most affected by neutron exposure.

Meticulous device design, fabrication process design which anticipates the silicon damage, and circuit design which is forgiving of leakage, transistor gain degradation and other neutron effects is the key to success here.

The other type of radiation effect of concern is that which generates a short signal pulse within the circuit while it is operating. If the pulse is small, it may be interpreted by the circuit as a normal signal and processed out, causing a data error known as single event upset. If the pulse is large enough, it may cause a signal to flow through obscure paths not designed as part of the circuit, resulting in a condition known as single event latchup. The signal pulse effect can be induced by a variety of types of incident radiation, including several associated with nuclear events. For many satellite applications, however, the principal cause of this effect is exposure to cosmic rays.

Cosmic rays are actually single, high energy, heavy ions. They are relatively abundant in space and are regularly encountered by the electronics in satellites. When one strikes the surface of an integrated circuit it causes physical damage and also generates a cloud of positive and negative charges. Though the physical damage may degrade circuit performance, it is the generated charges which have the immediate effect. If the cosmic ray strike is near a transistor or other device, the charges may be swept into the device and interpreted as a signal by the circuit. A data upset in a circuit can be caused by cosmic rays and by energetic protons. Both CMOS and bipolar technologies are vulnerable to this type of radiation.

The use of technologies which utilize thin films of silicon, such as silicon-on-sapphire (SOS) and silicon-on-insulator (SOI), significantly reduces sensitivity to cosmic rays by minimizing the silicon volume available for charge generation. Special circuit designs which are specifically intended to "damp out" the spurious signal pulse before it causes trouble are also used to harden satellite integrated circuits and systems against SEU.

The design and processing techniques used to provide radiation hardness are sophisticated and

continued on page 10

New Product Release Schedule

Product Type	Product Description	Package Type	Sample Availability	Product Introduction	Datasheet Availability
ACTS04	Hex Inverter	D,K	Now	Now	Now
HCS05	Hex Inverter	D,K	Now	Now	Now
HCS112	Dual J-K Flip Flop	D,K	Now	Now	Now
HS-26C31	CMOS Line Transmitter	1,9	Now	Now	Now
HS-26C32	CMOS Line Receiver	1,9	Now	Now	Now
HS-565ARH	12-bit D/A Converter	1,9	Now	Now	Now
HS-546RH	16 Channel Analog Multiplexer	1,9	Now	Now	Now
HS-9008RH	Flash A/D Converter	1,9	Now	Now	Now
HCS139	Decoder/Demultiplexer	D,K	Now	Jan. 93	Jan. 93
HCS157	Quad 2-input Multiplexer	D,K	Now	Jan. 93	Jan. 93
HCS163	Presettable Counter	D,K	Now	Jan. 93	Jan. 93
HCS240	Octal Buffer/Line Driver	D,K	Now	Jan. 93	Jan. 93
HCS241	Octal Buffer/Line Driver	D,K	Now	Jan. 93	Jan. 93
HS-547RH	Differential 8 Channel Analog Multiplexer	1,9	Now	Jan. 93	Jan. 93
HS-548RH	8 Channel Analog Multiplexer	1,9	Now	Jan. 93	Jan. 93
HS-549RH	8 Channel Analog Multiplexer	1,9	Now	Jan. 93	Jan. 93
HS-65758RH	SOI 256K SRAM	1,9	Now	June 93	Prelim. Now
HS-65759RH	SOI 256K SRAM	1,9	Now	June 93	Prelim. Now
HCS125	Quad Buffer	D,K	Jan. 93	Feb. 93	Feb. 93
HS-2420RH	Sample/Hold Amplifier	1,9	Jan. 93*	Feb. 93	Feb. 93*
ACS00	Quad 2-input NAND Gate	D,K	Feb. 93	Feb. 93	Mar. 93
ACS521	8-bit Identity Comparator	D,K	Feb. 93	Feb. 93	Mar. 93
ACTS00	Quad 2-input NAND Gate	D,K	Mar. 93	Apr. 93	Apr. 93
HS-506RH	16 Channel Analog Multiplexer	1,9	Mar. 93*	Apr. 93	Apr. 93*
HS-507RH	Differential 8 Channel Analog Multiplexer	1,9	Mar. 93*	Apr. 93	Apr. 93*
HS-508RH	8 Channel Analog Multiplexer	1,9	Mar. 93*	Apr. 93	Apr. 93*
HS-509RH	Differential 4 Channel Analog Multiplexer	1,9	Mar. 93*	Apr. 93	Apr. 93*
ACS161	Binary Counter	D,K	Apr. 93	May 93	May 93
ACTS161	Binary Counter	D,K	Apr. 93	May 93	May 93
HS-2510RH	High Slew Rate Op Amp	1,9	Apr. 93*	May 93	May 93*
HS-2520RH	High Slew Rate Op Amp	1,9	Apr. 93*	May 93	May 93*
ACS125	Quad Buffer	D,K	May 93	June 93	June 93
ACTS125	Quad Buffer	D,K	May 93	June 93	June 93
ACS280	Parity Generator/Checker	D,K	May 93	June 93	June 93
ACTS280	Parity Generator/Checker	D,K	May 93	June 93	June 93
HS-139RH	Quad Comparator	1,9	May 93*	June 93	June 93*
HS-2600RH	High Slew Rate Op Amp	1,9	May 93*	June 93	June 93*
HS-2620RH	High Impedance Op Amp	1,9	May 93*	June 93	June 93*
HS-6664RH	8Kx8 CMOS PROM	1,9	May 93	July 93	Advanced Now
HS-XC3020	FPGA	9	June 93	Oct. 93	Prelim. Now

Now = Released in current quarter (October-December 1992)
* = Non-rad hard product datasheets and samples are available now

Package Types = 1: Ceramic Dual-in-Line (DIP) D: Dual-in-Line Metal-Seal Ceramic
9: Flatpack K: Flatpack

Radiation and Integrated Circuits

continued from page 4

more expensive to develop and manufacture than those for ordinary commercial products. Similarly, the product assurance activities to verify consistent radiation hardened performance go beyond those required for commercial and industrial levels. The incremental investment can be very wise, however, in terms of the resulting assured IC performance in adverse radiative environments.

Space Product WINS

HARRIS SPACE PRODUCTS was selected by Fujitsu to design and develop a rad hard A/D converter for use on ASTER ... *and* ... was awarded Certified Supplier status by TRW Electronics Systems ... *and* ... HARRIS SPACE PRODUCTS' HS-26C31 and HS-26C32 are being used by Deutsche Aerospace on the AMOS Satellite.

Specifying Integrated Circuits For

By Chuck Tabbert

Until recently, most integrated circuit (IC) technologies for the manufacturer of products guaranteed to withstand the severe radiative environment of space were available only to the military. These technologies are now considered "dual use" in nature and can have significant positive impact on the burgeoning commercial space market. And burgeoning it is! For example, a growth market in small, commercial satellite programs (SMALLSATs) alone is expected to generate an estimated 4 billion dollars in revenue if all of the estimated 270 satellites are built and launched.

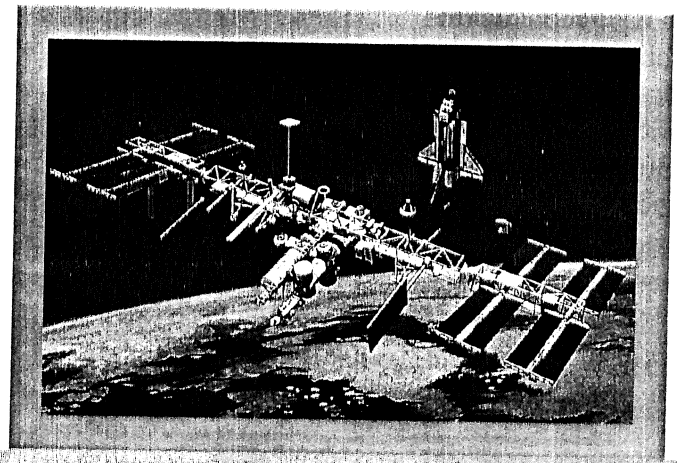
"Radiation hardness" is the magical attribute provided by these technologies which is leading to a win-win situation for both commercial and military designers alike. There are several reasons for this, including:

- a wider commercial market provides a potential volume of sales necessary for rad hard circuit vendors to continue to operate fabrication lines
- commercial circuit designers receive the benefits of this already developed rad hard technology without having to resort to exotic techniques to diminish radiation effects
- rad hard circuit vendors are beginning to inventory their more common products and offer them, for the first time, through various distributors because commercial concerns drive the market
- vendors are pursuing licensing agreements and have become internationally competitive

Designers must consider several key factors in the space applications environment to properly determine the requirements they must place on the ICs and other components of a satellite system. Critical factors relating to radiation effects are orbit shape (elliptical to circular), orbit altitude (low earth to geosynchronous), orbit inclination (equatorial to polar), mission life (6 months to 15 years), and IC location (internal or external to main spacecraft).

Because elliptical orbits traverse a wider region of trapped particle belts, satellites in elliptical orbits tend to have higher radiation exposures than those in more circular orbits. Similarly, the orbit altitude is extremely significant in that at certain altitudes, for instance those of the Van Allen Belts, there are high concentrations of charged particles and consequently a greater exposure to radiation. The Van Allen Belts are not homogeneous, however. At lower altitudes, the concentration of charged particles is significantly higher at high latitudes, a fact which causes radiation issues for certain altitudes to be a function of the orbital inclination.

Many types of radiation produce a cumulative effect over time, slowly shifting operating points and ultimately causing parametric and possibly functional failures. For this reason, the length of the mission is considered in the system analysis. Finally, since the structural material in a spacecraft provides a certain amount of radiation shielding for portions of the electronics, the actual physical location of system components is analyzed to yield the best tradeoffs between cost, reliability and performance.



Much has been learned about the radiation attributes of earth orbits. For purposes of discussion, they can be broadly grouped according to orbital altitude and inclination.

Spacecraft in ***Low***

Space Radiation Environments

Altitude (200 - 500 km), Low Inclination (28° And Below) Orbits experience an estimated 100 Rad to 1KRad (Si)/year of orbit. This radiation is primarily due to incident charged particles creating trapped charge in the semiconductor device. Although protons residing in the Van Allen Belts make Single Event Upset (SEU) a more important concern at this inclination, geomagnetic shielding provides a natural barrier where SEU rates can be reduced by 100X. Therefore, carefully screened rad-tolerant ICs can be considered for these applications and can be expected to operate for several years.

Radiation tolerant ICs are products which have been shown to have an ability to tolerate certain levels of given types of radiation, but usually specification parameters on "data sheets" are not guaranteed. Although radiation tolerant circuits tend to be less expensive than equivalent rad hard products, system designers usually have to take extraordinary measures to compensate for radiation effects, including:

- shielding in the form of thicker container structures
- characterizing each lot of parts for their particular radiation environment
- periodic refreshing of memory circuits

Radiation hardened ICs, on the other hand, are guaranteed by design and verified by repeated testing to have tolerance for given types of radiation and are specified post radiation over the full temperature range. They tend to be more expensive at the unit level due to the design investment and manufacturing sophistication required to produce them but system designers do not have to resort to the techniques mentioned above and can concentrate on system performance.

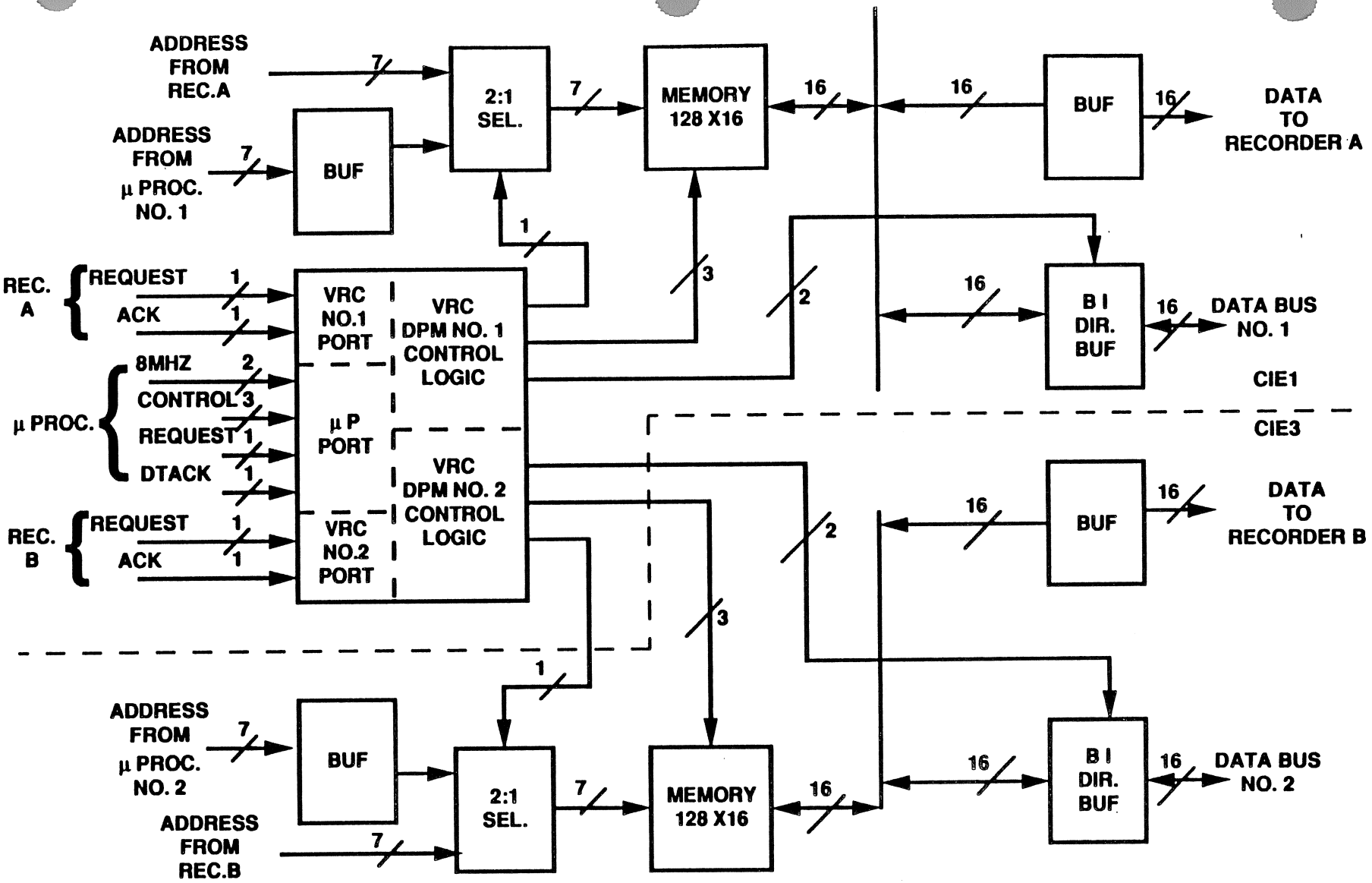
Designers should take precautions to insure that these devices do not latch-up [usually linear energy transfer (LET) >40]. Most system designs include safety factors for radiation of 10 times the expected radiation level, leading to a recommended total dose requirement of up to 10KRad (Si)/year for these orbits and inclinations.

Total dose radiation of spacecraft in ***Low Altitude (200 - 1000 km) But High Inclination (Greater Than 28°) Orbits*** varies between 1KRad and 10KRad (Si)/year of orbit. Proton damage is more prevalent due to the increase in traversed area through the Van Allen Belts. For this reason the Adams 10 percent worst case environment, a standard environment combining the effects of solar minimum galactic cosmic rays and solar particle activity is recommended for SEU calculations. Accordingly, rad-hard devices are recommended and can fly in this environment for several years. Again, with design safety factors considered, the part technology should tolerate greater than 100KRad and should not latch-up (LET > 40).

Historically in the realm of military special missions (short-term reconnaissance spacecraft), more programs seem to be approaching ***Medium Altitudes*** **(1000 - 4000 km)** or passing through them on highly elliptical orbits. Total dose radiation in this region increases to the range of from 100KRad to 1MRad (Si)/year, independent of inclination. Geomagnetic shielding for SEU is significantly reduced at this altitude, and only radiation hardened ICs will perform at these altitudes for more than a short period of time.

Geosynchronous Orbits **(36,000 km)** are primarily the realm of communications satellites, both commercial and military. Here, the total dose effects drop back into the KRad (Si) per year range, but spacecraft charging caused by the interaction of the Earth's magnetic field and solar wind comes into play, so the SEU effects are primarily dominated by the Adams 10-percent worst case environment. A recommended approach is to use rad-tolerant ICs where possible and rad hard technologies for critical mission functions.

continued on page 11



VIE RECORDER DUAL PORT MEMORY BLOCK DIAGRAM

FIGURE 3 -15

The control logic on CIE1 also controls the data into and out of the dual port memories on CIE3. Only the source/destination of the data and the source of the address are different.

3.3.3.2 Computer Interface PWA No. 2 (CIE-2)

The Computer Interface schematic is found in drawing number 34069289 and the assembly drawing is 34069291. This assembly consists of the following functions:

- o The Interrupt Logic
- o I/O Decode Part 2
- o VIE Command Muxer
- o Real Time Counter

3.3.3.2.1 Interrupt Logic

The requirements for the interrupt logic are:

- o Interface with 21 interrupts
- o Provide, masking for 19 of the 21 interrupts
- o Latch all interrupts/software reset latches
- o Prioritize all interrupts
- o Generate interrupt vector number for all interrupts

3.3.3.2.1.1 Interrupt Levels

The MC68000 handles seven levels of interrupt processing plus the reset line processing, which can be considered a unique interrupt. Six of the seven levels are internally maskable by the MC68000. Level 7 and Reset are not maskable.

The SSMEC Block II has 21 interrupts which are encoded into these 7 levels of interrupt. Table 3 - 1 contains a list of the interrupts and their levels. In addition to the level masking, the nineteen interrupts in level 5 and lower each have individual bit masking that can be set and reset by software command.

Each interrupt as it is received by the CIE2 Printed Wiring Assembly (PWA) is stored in a latch. These latches can be cleared by cycling power or by software commands. The twelve servo error latches are all cleared by one command. Each of the other latches has its own clear command.

3.3.3.2.1.2 Encoding

The CIE2 Interrupt Encoding Logic takes the 21 interrupt levels and encode them into a three bit octal number that defines the level of the interrupt and an eight bit code that defines the vector number. See Table 3 -3.

Interrupt request are provided to the DCU interface indicating the priority level of the highest mask enabled interrupt that is active in the Interrupt Logic. This request is provided to the DCU via the three IPL output lines. When the request is accepted, the DCU sets the three function code inputs (1FCX1) to ones and the three LSB address bits to the priority level of the interrupt request being acknowledged. The high to low transition of the lower data strobe (1LDSTRBO) stores the active interrupts in a register, generates the vector number of the interrupt and transmits it over the lower byte of the common data bus (C0MDBXX1).

If more than one interrupt is active at the acknowledged priority level, the vector number of the highest interrupt is transmitted.

The undefined interrupt vector number (79) is transmitted if the active interrupt is at some priority level other than the acknowledged priority level. A spurious interrupt vector number (80) is transmitted if there are no active interrupts when the interrupt acknowledge is received by the interrupt logic.

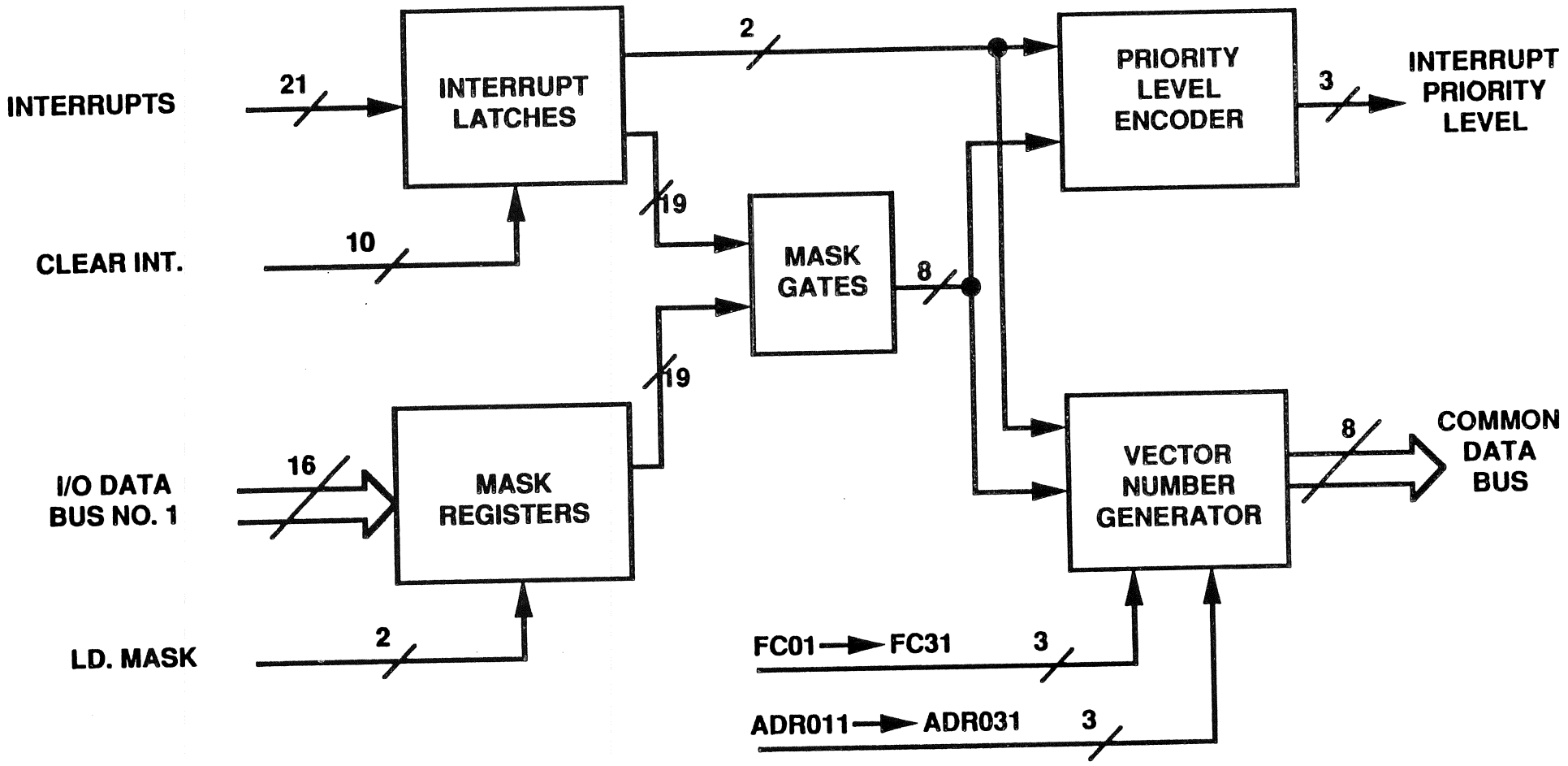
A block diagram of the interrupt logic is given in Figure 3-16.

3.3.3.2.2 Command Multiplexer

The Command Multiplexer on CIE 2 is a 16 bit wide 8 to 1 multiplier that routes data to the controller common data bus from:

- o Command Test Word (AAAA)
- o Command Channel A
- o Command Channel B
- o Processor Signal
- o Command Channel C
- o Real Time Clock
- o Servo Interrupt Errors
- o Command Test Word (5555)

The three LSB from processor number ones address bus (1ADRXX) and the decode of address 820 COX (ENMUX00) are used to decode the 16 bit wide 8 to 1 multiplexer. The common data bus is used to supply data to both processors of the SCP.



INTERRUPT CONTROL LOGIC BLOCK DIAGRAM

FIGURE 2-6

3.3.3.2.3 Real Time Clock (RTC)

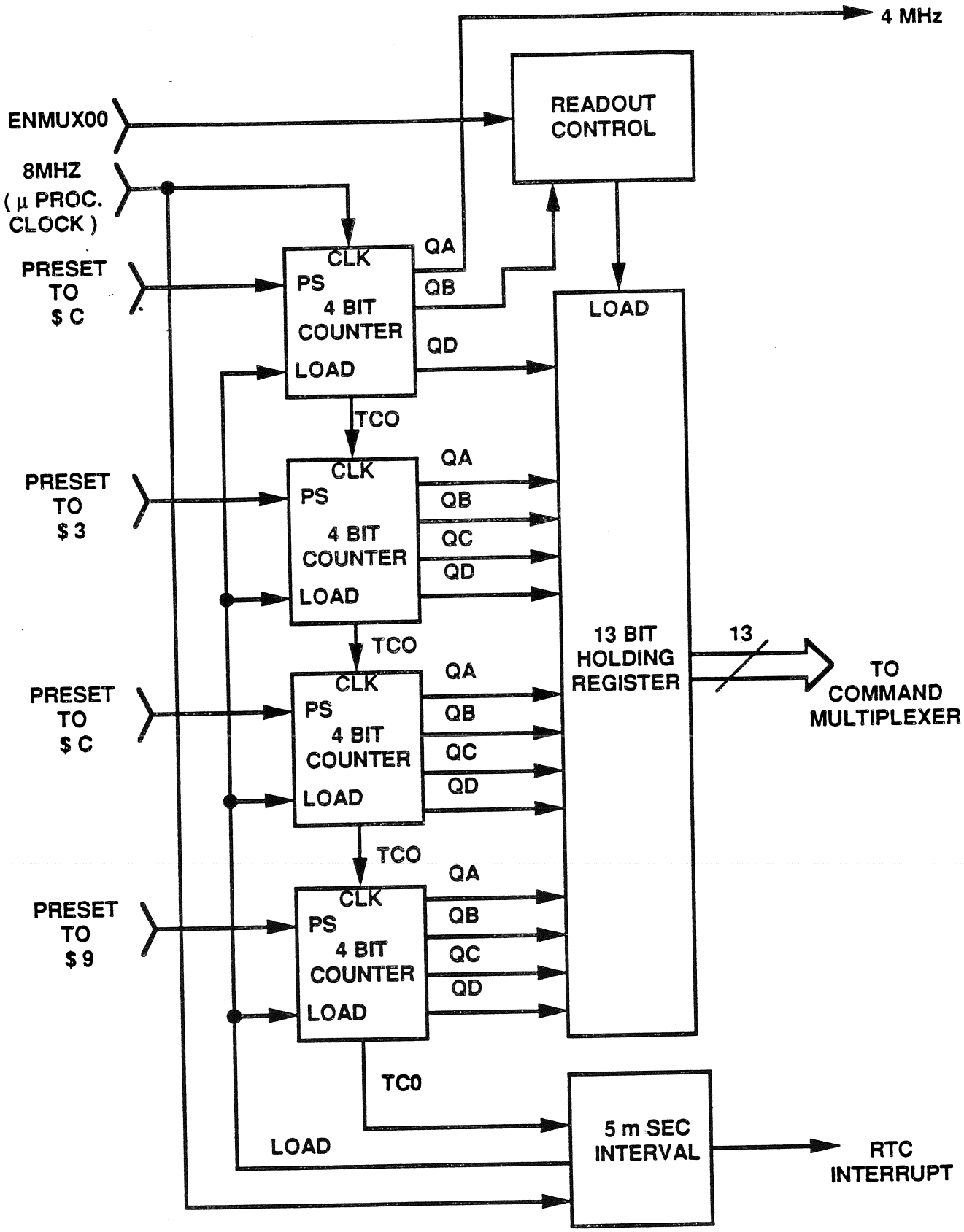
The real time clocks requirements are:

- o The counter must be a 13 bit down counter
- o Must generate an interrupt pulse at 5 millisecond intervals.
- o Must be clocked from the DCU clock
- o All 13 bits must be readable by software on a non-destructive and non-interfering basics.

Figure 3-17 is a block diagram of the real time clock (RTC) counter. The RTC uses the DCU clock (8 MHz).The RTC provides a timing reference interrupt at intervals of 5 msec and clock to the Watch Dog Timer 1 (WDT 1). The RTC is actually a 16 bit counter that is initialized to 9C3C (HEX); it counts down to 0000 at an 8 MHz rate. The 13 MSBs of the counters output are reframed at a 4 MHz rate. The 13 MSBs can be read by the microprocessor without disturbing the count; the reframe function is inhibited during a read cycle.

3.3.3.2.4 I/O Decoder Part 2

The I/O Decode Part 2 located on CIE2 performs the function of controlling the tie in of the command data mux with common data bus and the tie in of the common data bus (COMDBXX) with the number one processor data bus (1DATXX).



REAL TIME COUNTER BLOCK DIAGRAM

FIGURE 3 - 17

Table 3-3

CATEGORY	SIGNAL	FUNCTION	PRIORITY	NOTES (HEX)	ADDRESS
Power Interrupts	**Reset**	Reset System at Power On	8	2	800000
	PFI	Power Failure Interrupt	7		000100
	PRI	Power Recovery Interrupt	6		000104
Disqualifying Failures	**SCPI**	SCP Error Interrupt	5	1,3	000108
	WDTH1	WDT #1 HALT Interrupt	4	1	00010C
	WDTH2	WDT #2 HALT Interrupt	4	1	000110
	SEII	Servo Error Interrupt	4	1,4	000114
Timing	**TRI**	Timing Reference Int.	3	1	000118
Alternate	**RCFI1**	Redundant DCU Failure Interrupt #1	2	1	00011C
Channel	**RCFI2**	Redundant DCU Failure Interrupt #2	2	1	000120
Failure	**ADPFI1**	Alternate DCU in PFI	1	1	000124

Note 1: These interrupts are individually maskable external to the MC68000. Upon removal of the mask the status of the interrupt must be accessible to software.

Note 2: The "RESET" system upon initial "Power On" is <u>not</u> a normal user defined interrupt. The application of this signal shall be accompanied by an address being jammed onto the bus forcing the PC to start execution in PROM.

Note 3: When a SCP miscompare occurs, hardware shall immediately time out WDT and issue an interrupt.

Note 4: If any of the 12 servoactuator issues a servoactuator interrupt the SEII shall be triggered. To isolate the error a word shall contain an indication of which servoactuator originated the signal. The status of the Servo Error Interrupts is shown in Table VIII, Input Word 7 of DSHG8977A1.

3.3.3.3 Computer Interface Electronics No. 3 (CIE-3)

The Computer Interface Electronics Number 3 schematic is found on drawing 34069268 and the assembly drawing number is 34069270. The functions contained by CIE 3 are:

- o Input Electronics Dual Port Memory No. 2.
- o Vehicle Recorder Dual Port Memory No. 2.
- o Watch Dog Timer No. 1.

3.3.3.3.1 Input Electronics Dual Port Memory No. 2

Input Electronics Dual Port Memory No. 2 provides the same function as IE DPM No. 1 defined in 3.3.3.1.2 except that IE DPM No. 2 interfaces with SCP processor No. 2 instead of No. 1. The block diagram of the input electronics dual port memory No. 2 is shown in Figure 3-14.

3.3.3.3.1.1 IEDPM Address

The memory address to be used for data access is selected using a multiplexer controlled by the memory control logic; the address inputs are the eight DCU address bits (2ADROII to 2ADRI81) or the eight IE address bits (2IEDMAII to 2IEDMA81).

3.3.3.3.1.2 Data Source/Destination Routing

A DCU write or IE memory access initiation enables data to the memory. An IE access enables data from the IE (2IDMOO1 to 2IDM151) through tri-state buffers onto the common I/O memory pins. A DCU access enables the DCU data (2DATOO1 to 2DAT151) through a tri-state bi-directional buffer to the memory when the IE data select is inactive. A read access by the DCU reverses the direction of the tri-state bi-directional buffer enabling data from the memory on to the DCU data bus. Control signals for this logic are generated from the memory access control signals.

3.3.3.3.1.3 Memory Access Control Signals

The RDPM2 Memory Access Control Signal logic generates the timing of the read enable (IEM0EO), the write strobe (IEMWEO) and the memory chip select (IEMCSO) for IE memory access.

The memory is selected when the IE access, IECS21, is active or when a Micro Processor (µP) request, PIECS21, and µP address strobe are active. A memory write is generated when the IE requests a write or when the µP requests a write function and the µP memory access enable is active. Data from the memory is enabled when the IE data enable is not active, and the µP requests a read or when the µP access is not active.

3.3.3.3.2 Vehicle Recorder Dual Port Memory No. 2 (RDPM2)

The Vehicle Recorder Dual Port Memory No. 2 function is the same as RDPM1, on CIE1, except that it takes data from SCP processor No. 2 instead of No. 1 and send its data to recorder channel B and processor No. 2.

3.3.3.3.2.1 Memory Address Selection

The RDPM2 address to be used for data access is selected using a multiplexer controlled by the memory control logic; the address inputs are the seven DCU address bits (2ADRO11 to 2ADRO71), or the seven VRC address bits, (-VRCMA1 to -VRCMA7).

3.3.3.3.2.2 Data Source/Destination Routing

Data from the DCU to the memory is selected when the DCU has initiated a memory access that is a write operation. The data enabled onto the memory common I/O pins is the DCU data on inputs 2DATOO1 to 2DAT151 from bi-directional drivers. A DCU read enables data from the memory through the bi-directional drivers onto the DCU data bus if the VRC data select is not active; a VRC read enables data from the memory onto the VRC data bus, VRC-DOO1 to VRC-D151. The control signals for this logic are generated from the memory access controls signal.

3.3.3.3.2.3 Memory Access Control Signals

The Memory Access Control Signal logic generates the read enable (VRM0E20), write strobe (VRMWE20) and memory chip select (VRMCS20) to access the VRC Dual Port Memory using signals generated off card.

The memory is selected when VRMCS20 is received by the card. The memory write signal is generated when the uP requests a write function and the uP memory access enable is active. Data from the memory is enabled when the IE data enable is not active, and the uP requests a read or when the uP access is not active.

3.3.3.3.4 Watch Dog Timer

The function of the Watch Dog Timer (WDT) is to act as an independent monitor of the operation of the controller processor and software. The Watch Dog Timer must be periodically reset or it will time out. When a watch dog timer times out it shuts the channel it is monitoring is shut down. For safety and redundancy sake there are two watch dog timers per channel in the SSMEC. The SSMEC requirements for the Watch Dog Timer WDT are:

- o Two WDT's for redundancy
- o 18 ± 3 Msec time out period
- o Fast timeout via self checking pair error
- o Independent software set and reset commands
- o Independent timing sources
- o Initialized to timeout state at power turn on

The block diagram for the WDT is shown in Figure 3-18.

3.3.3.3.4.1 Watch Dog Timer 1

The Watch Dog Timer 1 circuitry consists of a timing counter and the logic to control it. The control signals enable the time out counter, set, or reset it.

3.3.3.3.4.2 Watch Dog Timer Set

An immediate time out, or error indication, XZWDT10 (or any of the inverted versions of this signal) is generated when a master clear signal (MSTRCLRO) is received; if a DCU set command (SETWDT10) is generated; if an error in the address (1ADMCMP1) or data check (1DAMCMP1) is detected; or if the operational voltage is out of tolerance.

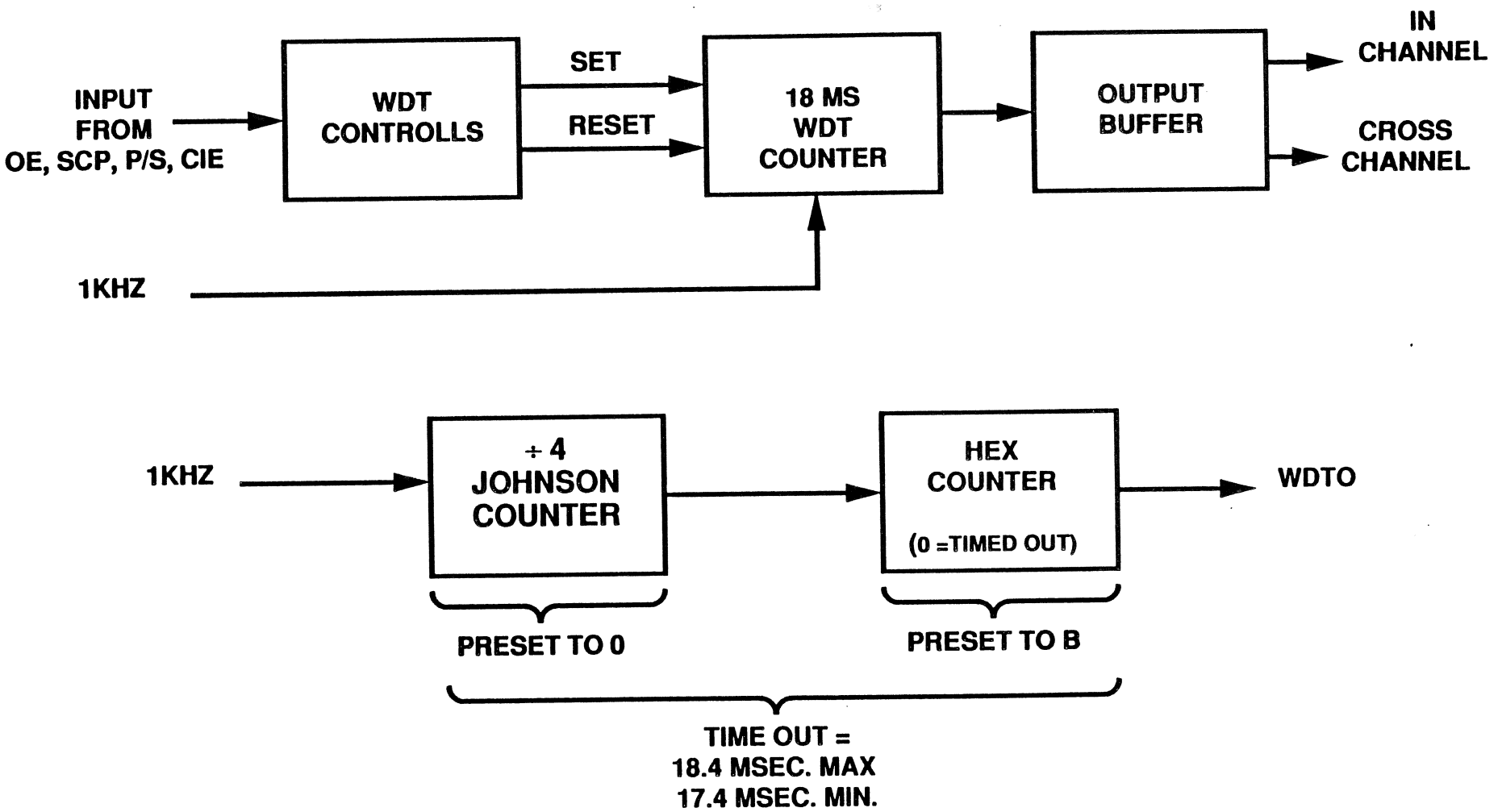
3.3.3.3.4.3 Watch Dog Timer Reset

The Watch Dog Timer is reset when a DCU generated reset command (RSTWDT10) occurs or when the GSE enables the reset with GINHWT10. The reset forces the counter into a count condition.

3.3.3.3.4.4 Counter Time Out

After the Watch Dog Timer is put into a reset state, it is enabled to count out an 18 ± 3 msec delay using the 0.977 KHz clock (WDTICLK1) generated by the real time clock circuitry.

This clock is divided by 4 and the resulting square wave is used to clock a counter that results in an 18 ms time out if no other counter controls are activated. To prohibit the counter from reaching a timeout condition, a reset command must be generated at intervals less than the timeout interval.



WATCH DOG TIMER
BLOCK DIAGRAM

FIGURE 3 - 18

3.3.3.3.5 Common Data Bus Buffering

Data from the Common Data bus, COMBOO1 to COMB151, is enabled through tri-state buffers onto the Processor No. 2 data bus 2DATXX when 2CDBENO is generated. 2CDBENO is a decoded function of the DCU address bits, address strobe, and read enable. The buffer for the cross channel OE drive (OEDXX) is also on CIE3.

3.3.3.4 Computer Interface Electronics No. 4 (CIE 4)

The Computer Interface Electronics No. 4 schematic is found in drawing 34069286 and the assembly drawing is found on 34069288.

The functions contained on CIE 4 are:

- o Vehicle Command Channel
- o High Byte Data Muxer
- o Watch Dog Timer No. 2
- o Frequency Divider

Because the vehicle command channels is on CIE 4, three CIE 4 printed wiring assemblies are used per controller. All three CIE 4 command channels are all read by channel A and channel B SCP computers and each is powered from a different independent power source.

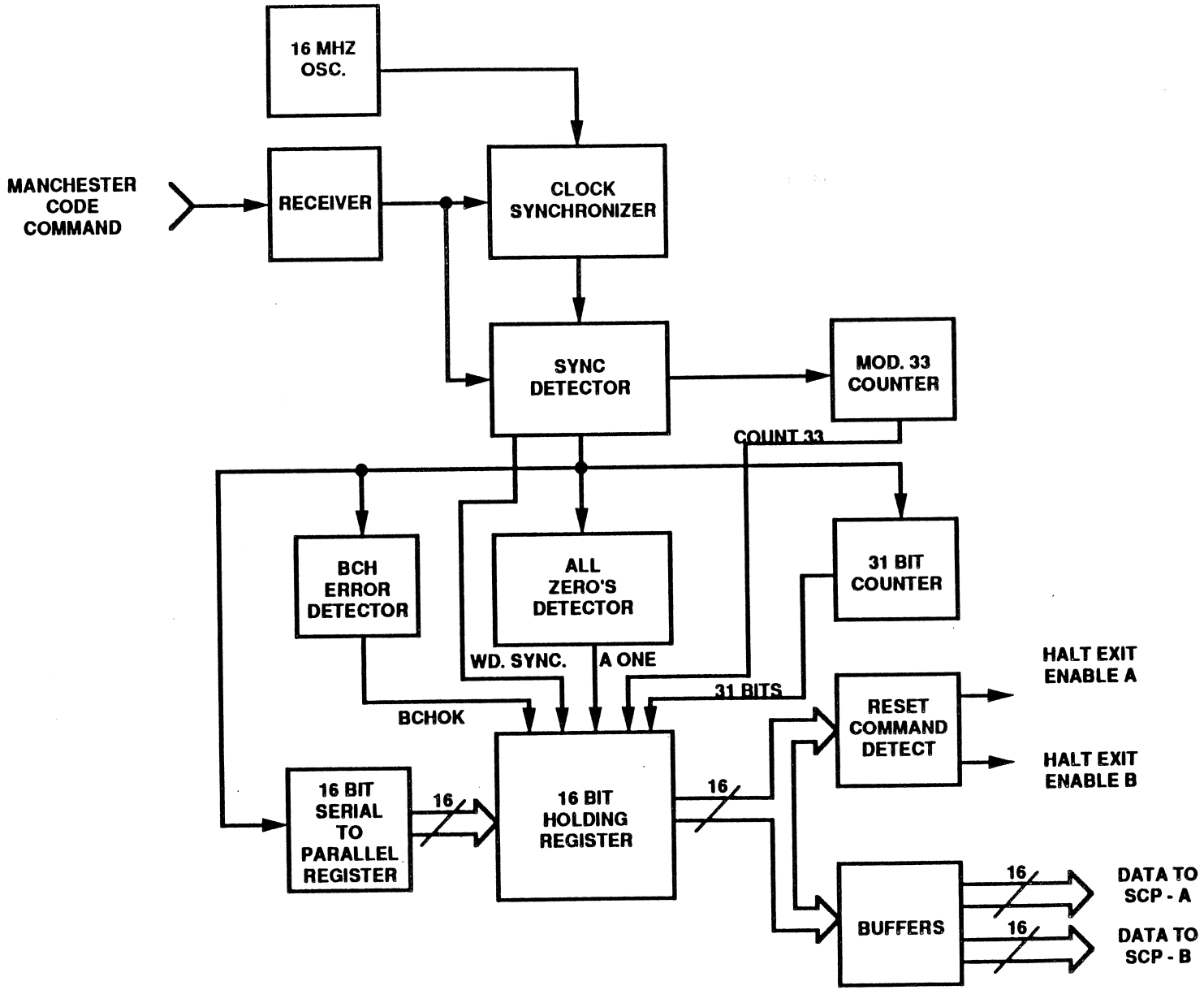
3.3.3.4.1 Vehicle Command Channel (VCC)

The Vehicle Command Channel is part of the vehicle/controller command interface. The controller command interface requirements are:

- o Three redundant serial channels
- o Manchester encoded
- o 1MHz bit rate
- o 33 bit words
  - 16 data bits
  - 15 BCH error detection bits
  - 2 sync bits
- o Error detection
  - Correct number of bits per word
  - No All "Zero" words
  - No BCH errors

The VCC receives 31 data bit serial words from the vehicle in Manchester form. Each word is verified, stripped of its check bits, and converted to parallel form.

The VCC is subdivided into functional modules, as shown in Figure 3-19. A functional description of these modules follows. Figures 19A and 19B show bit timing and word timing forVCC.



VIE COMMAND CHANNEL BLOCK DIAGRAM

FIGURE 3 - 19

3.3.3.4.1.1 Receiver and Clock Synchronizer

The receiver and clock synchronizer converts the differential Manchester input into a Manchester TTL data stream. When a rising or falling edge is detected in the Manchester serial data, a 4 bit serial shift register (U06) is preloaded with a binary 1111 whenU06-10 is asserted HI. When U06-10 is negated and the QB output is high, the register willbe enabled to shift the data right. The QA output is used to generate CLKOA/, while QA and QB generate CLKB. The QB output is inverted and fed back to the shift register as a serial input. This causes the register to loop through the states shown below:

QA	QB	
1	1	Preset
0	1	N/A
0	0	CLKB
1	0	CLKOA/

CLKOA and CLKAB are used by the sync detector to generate the VCCLKA1, VCCLKA2, CNTRCLK1, and WRDSYNC1 signals.

3.3.3.4.1.2 Sync Detector

The purpose of the sync detector is to recognize the occurrence of the sync pulse which separates data words, and to generate synchronizing signals. The sync detector receives serial data, CLKA1, and CLKBO from the receiver and clock synchronizer. VCCLKA20 and CTRBIT71 inputs come from the MOD 33 counter. CLKBO is used to sample the serial data twice during each bit time. If two logic low levels are followed by two logic high levels and the CTRBIT71 signal is asserted, indicating the end of a 31 bit word, then a sync pulse is recognized and SYNCRSTO and WRDSYNCO are asserted. SYNCRSTO is used by the all zeroes detector.

3.3.3.4.1.3 Modulo 33 Counter

There are 33 bit times in a data word cycle. These contain three different types of data: 16 bits of Manchester encoded data, 15 bits of error-detecting code (also in Manchester form) and two sync bits. The function of the modulo 33 counter is to indicate the current position in this cycle. CTRBIT71 is output to the sync detector and CNT331 to the hold registers to indicate the end of the BCH bits. ENORS1 is asserted at the start of the BCH bits to tell the BCH error detector to enable its exclusive "ORs".

The VCSRCLK1 signal is sent to the storage and holding registers. It is enabled during the first 16 bits of serial, and clocks the serial data through a shift register into holding registers. The BCHCLK1 signal is enabled during the first 31 bit-times. It clocks first the data and then the BCH check bits into the BCH error detector for verification. VCCLKA1 and VCCLKA2 are inputs used to synchronize the operation of the modulo 33 counter to the Manchester data rate. CNTRCLRO is an input from the sync detector which clears the counter when a sync pulse is detected.

3.3.3.4.1.4 All Zeroes Detector and Bit Counter

The all zeroes detector receives serial Manchester encoded data from the sync detector. It changes this data into non-Manchester serial data and passes it on to the BCH error detector for verification. VCCLKA1 is used to sample the Manchester data at the middle of the first half of the bit cell to determine the polarity of the bit. BCHCLK1 is used to clock the data into the BCH error detector. The AONE1 signal is asserted when at least one logic one bit is detected in the data. "No message" words are all zeroes. It clocks the holding registers if a message is detected. The 31 bits signal is asserted to the BCH error detector, which gives the BCHOK1 signal at the end of the 31 bit period if the data has no errors. The SYNCRSTO signal is used to clear the counters at the end of each word.

3.3.3.4.1.5 Halt Exit Detection

There are two halt exit enable signals, one for each channel. - HEXAO is asserted when the message from the vehicle is 9E00 hex. Channel B halt exit enable, HEXBO, is asserted for a data word or 9FOO hex. A halt exit is enabled by the vehicle to restart the controller when it has halted due to an error.

3.3.3.4.1.6 16 Bit Serial to Parallel Register

This register receives serial data from the zeroes detect and 31 bit counter. It receives the BCHOK1 signal from the BCH error detector. The data is shifted through two 8 bit shift registers. The data is latched into two 8 bit storage registers, to the output drivers and halt exit detector if all of the following conditions hold: 1) There were 33 bits in the word, 2) 31 of those were Manchester bits, 3) The BCHOK1 signal is asserted, and 4) the word is not a "no message" word. If the word is not a "no message" word and the BCHOK1 signal is not asserted, or if there are not exactly 33 bits in the word, the holding registers will be cleared.

3.3.3.4.1.7 BCH Error Detector

The BCH error detector accepts 16 bits of serial data and 15 serial BCH check bits from BINDAT1. It asserts the BCHOK1 signal if no error is detected. During the first 16 bit times of the 33 bit cycle, the data is shifted through two registers. During this time, the ENORS1 signal is not asserted, so the exclusive ors are not enabled. The registers act like regular shift registers. During the next 15 bit times, BCH bits are shifted into the registers, but the ENORS1 signal is asserted to enable selected bits to be toggled as they pass through the registers. ENORS1 enables the exclusive ors to toggle bits when bit 7 in the second register is high. When all 15 BCH bits have been shifted into the registers in this manner, the result at the Q outputs of the registers should be all zeroes. If so, no error has been detected and BCHOK1 is asserted.

3.3.3.4.2 High Byte Multiplexer

The high byte multiplexer routes data from the IE, OE, or CIE onto bits 8-15 of the common data bus or to the cross channel multiplexer of the alternate channel. Three address bits are provided from processor #1 for choosing data to be put on the common data bus. Three cross channel address bits are provided for selecting data to go to the cross channel multiplexer. The high byte multiplexer uses eight pairs of multiplexers. Each pair receives the same data. One of the pair will source the common data bus, and the other the lines to the cross channel multiplexer.

Two drivers are used for the address inputs. When N-MUX10 is asserted, signals 1ADRO21 - 1ADRO41 are used as inputs to the multiplexers to put eight bits of data on the common data bus. When X-MUX10Z is asserted, XCADRO21 - XCADRO41 choose eight bits of data to be put on a bus to the cross channel multiplexer. When neither N-MUX10or X-MUX10Z is asserted, the multiplexers have high impedence outputs. A hard-wired OR exists between the commond data bus outputs and the cross channel buffer inputs. When COMDBO81 - COMDB151 are in a high impedance state, the cross channel buffer may source them with data from the cross channel multiplexer of the alternate channel.

3.3.3.4.3 Cross Channel Buffer

When the common data bus has been put into a high impedance state, the cross channel buffer may put data from the alternate CIE channel onto it. MUXCLK1 is an input from CIE-1 which latches the data from the holding register through a three state driver and onto the common data bus. X-MUX10 and X-MUX20 are I/O address decode lines from processor #1 which enable the three state driver. They are decoded on CIE-1.

3.3.3.4.4 Status Register

The status register is used to latch the high byte of data from the common data bus to the multiplexer on the failure data recorder board. The register is loaded when LDSTATO is asserted. The register may be loaded and read under software control.

Figure 3-20 is a block diagram of the high byte mux, status register and cross channel buffer interconnect.

3.3.3.4.5 Watch Dog Timer 2

The Watch Dog Timer 2 (WDT2) circuitry consists of two functional blocks, WDT2 control and WDT2 timer/counter. When WDT2 "times out" it indicates a failure in channel A or B.

3.3.3.4.5.1 WDT2 Control

The control portion of the WDT2 circuitry provides set and reset signals. States of WDT2 control are shown in Table IV.

WDTSETO is asserted if an address or data miscompare occurs in processor #2, if a master clear signal, MSTRCLRO, is received, if a SETWDT2O command is decoded by CIE-1, if the OE asserts OECLR1, or if the voltage to the OE is too low. Any of these occurrences cause an immediate timed out condition.

WDTRSTO is asserted if a RSTWDT20 command is decoded by CIE-1 or if the GSE enables a reset. After WDT2 is reset, an 18 msec wait occurs before the timed out condition.

3.3.3.4.5.2 Watch Dog Timer/Counter

The WDT2 timer/counter provides the 18 msec delay between a WDT2 reset and the timed out state. The WDT2 counter receives a 1 KHz clock signal from the frequency divider. This is divided by four and used to clock the 4-bit counter, which counts from 11 to 15 and then to 0. If the counter reaches 0 before another WDTRSTO command is received, WDT2 has "timed out" and WDT2 will be asserted. See Table IV.

HIGH BIT MUX

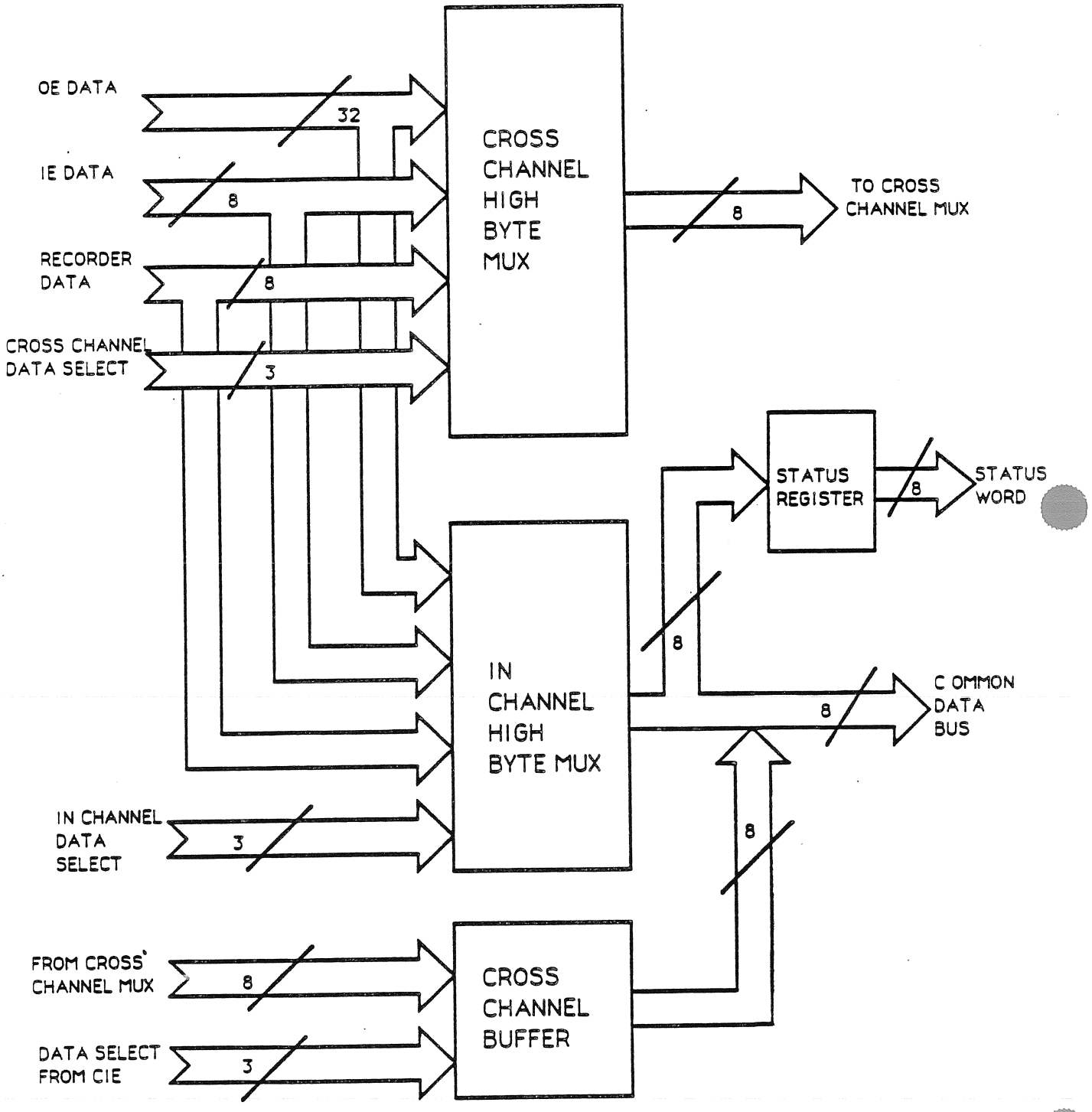


FIGURE 3-20

A self-checking pair indicator is also generated within the WDT2 circuitry. If a data miscompare (2DAMCMP1 asserted) or an address miscompare (2ADMCMP1 asserted) occurs, self-checking pair error (2SCPE1) is asserted.

3.3.3.4.6 Frequency Divider

The frequency divider divides the 16 MHz signal from the CIE4 oscillator to produce 1, 2, 128 and 512 KHz signals. Four 4-bit counters are used to divide the 16 MHz signal. The divided frequencies are sent through drivers and then used as shown in Table V.

3.3.3.5 Computer Interface Electronics No. 5 (CIE 5)

The Computer Interface Electronics No. 5 schematic is found on drawing 34069283. The Printed Wiring Assembly drawing is drawing 34069285. The functions contained on the CIE 5 assembly are:

- o Vehicle Recorder Channel
- o Low Byte Data Mux
- o Low Byte Status Register
- o Cross Channel Buffer

3.3.3.5.1 Vehicle Recorder Channel

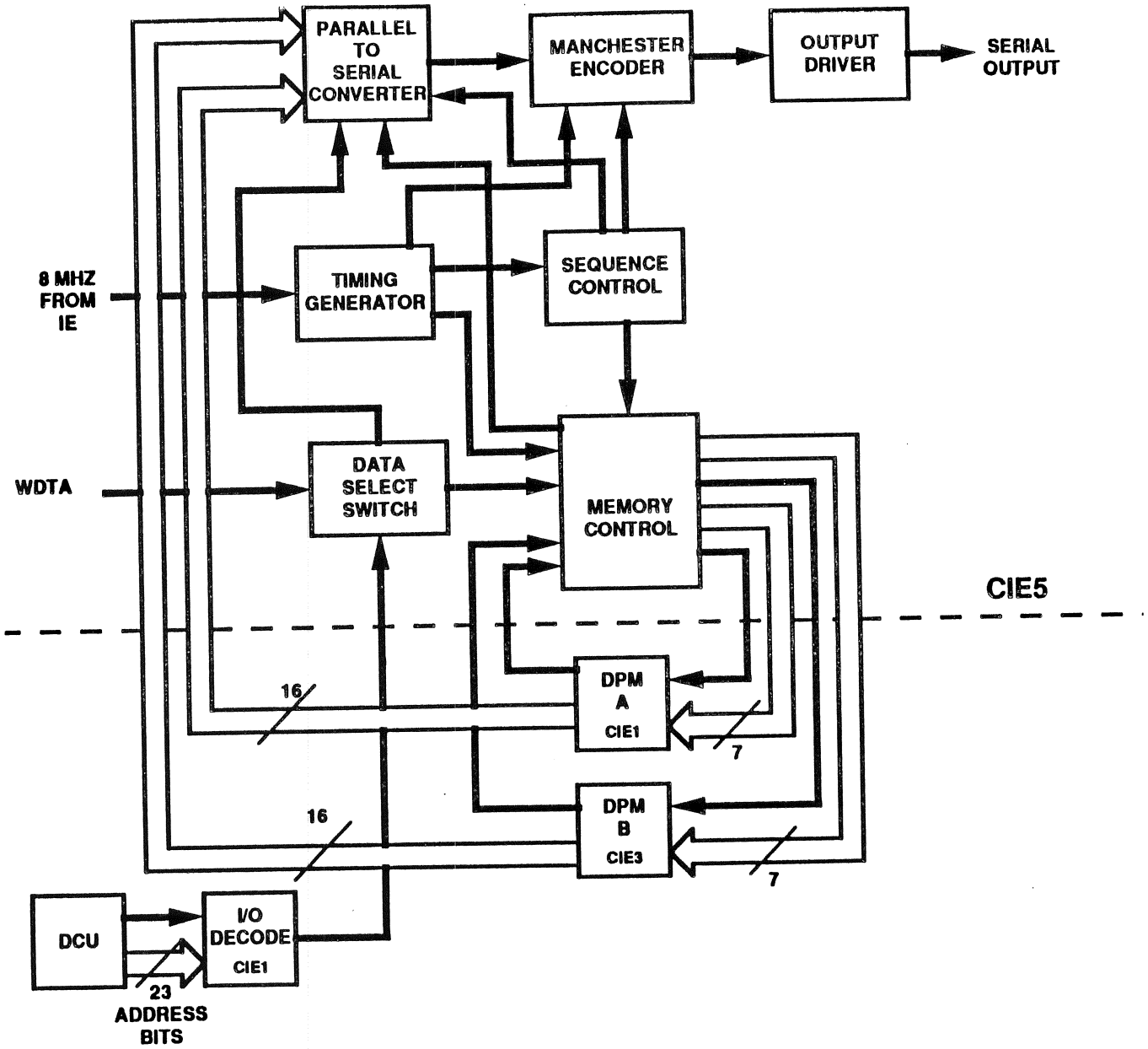
The vehicle recorder channel is part of Vehicle/Controller Interface. The recorder channel supplies data to the vehicle from either A or B channel controller electronics. The basic requirements of the vehicle recorder sub system are:

- o Two redundant serial channels
- o Manchester encoded
- o 1MHz bit rate
- o 19 bits per word
  - 16 data bits
  - 1 parity bit-odd
  - 2 sync bits

Figure 3-21 is the block diagram of one channel of the vehicle recorder if the channel shown in the diagram were channel A recorder, the input data would come from CIE 1-A and CIE 1-B. Channel B recorder's data would come from CIE 3-A and CIE 3-B. The I/O decode always comes from the inchannel CIE 1.

The VRC reads data from two 16-bit wide dual port memories. Only the low 128 locations of memory are used by the VRC. The contents of locations 0-127 of memory A or B is sent in a 128 word block to the vehicle, after being serialized, Manchester encoded (during which a parity bit and two sync bits are added) and amplified.

~~(118)~~



VIE RECORDER CHANNEL BLOCK DIAGRAM

FIGURE 3-

3.3.3.5.1.1 Data Select Switching

The purpose of the data select switching is to determine whether the data should be taken from channel A or channel B to be processed. Channel A inputs are used unless one or both of the Watch Dog Timers (-VRWDT11/Z2A-, -VRWDT21/Z3A- inputs) times out, or if DCU A issues a "switch-recorder-to-B" command. When B inputs are used, DCU B must issue a BINITV-0 command (820A2C hex) to put the circuit in a known state and initialize the address counter to zero. An initialize command before the transfer is complete will terminate the block transfer and reinitialize the circuit.

The data select switching generates the USEAIN signal. USEAIN is used by the multiplexer within the parallel to serial converter module to choose channel A or channel B data lines for processing. The data select switching also generates a data enable signal. This line is asserted when a data transfer acknowledge is received from memory, and causes data from the selected memory to be latched into the holding registers in the parallel to serial converter.

3.3.3.5.1.2 Parallel to Serial Converter

The parallel to serial converter module chooses the data from either channel A or channel B, stores it in a holding register, serializes it, and send it to the Manchester encoder module. The data is multiplexed from channel A or channel B depending on whether or not the USEAIN signal is asserted. When an acknowledge signal is received from memory, the data is latched into the holding registers. From there, it is converted into serial form by the shift registers and sent to the Manchester encoder at a frequency of 1 MHz. The shift registers are clocked by RSFTCLK, provided by the timing generator. The CLEARO input signal, when asserted, clears the shift registers' output to zero.

3.3.3.5.1.3 Manchester Encoder

The Manchester encoder accepts the serial data from the parallel to serial converter, encodes it in Manchester form, appends a parity bit and two sync bits, and sends the resulting word to output drivers. A Manchester code is a binary coding system whereby ones and zeroes are denoted by a voltage transition rather than by a voltage level. Voltage transitions occur at or near the midpoint of each bit time. A logic one is formed by a low to high transition, and a logic zero by a high to low transition.

The order of transmission is 16 data bits, with MSB first, followed by a bit for maintaining odd parity. The 17-bit data words are separated from each other by two consecutive synchronizing bit times which form a sync pulse. The first half of the pulse will be at a logic one level, the second at a logic zero. The rate of serial transmission is 1 MHz. The Manchester encoded data is sent to two different output drivers for transmission to the vehicle.

3.3.3.5.1.4 Memory Control and Address Counter

The memory control module has four states. These are indicated by the states of two flip-flops. Most of the time the memory control is either requesting data (state (1,0)) or awaiting the serial transfer of Manchester data to the vehicle (1,1). The other two states are a wait- to-send-next-memory-request (0,0) which synchronizes the end of the sync pulse to the memory request signal, and a data sent state (0,1) which occurs after the last data bit has been serially transmitted.

3.3.3.5.1.5 Memory Control and Address Counter (Continued)

The memory control module contains an address counter which uses two four-bit counters for addressing the dual port memories. When the INIT command is issued, both counters are set to zero by sequence control. Each address 0-127 will be put on the channel A and channel B address buses and held there until the contents of that address has been fetched from the appropriate memory and a data transfer acknowledge is received, on the leading edge of VRT18. The high bit in the upper counter is not used as an address bit. When the address counter reaches 128, the MSB of the upper counter (VDTCMPLT) is used to signal the sequence control that the entire block of data has been processed.

3.3.3.5.1.6 VRC Timing Generator

The VRC timing generator consists of two synchronous 4-bit counters, a shift register and a flip-flop. All are clocked by the 8MHz input.

The outputs QB and QC of one 4-bit counter are "picked off" to obtain 2 MHz and 1 MHz pulses for use by the Manchester encoder, parallel to serial converter, and memory control modules. The high bit of output is not used, but the carry bit enables the other counter, which generates a single pulse every 18 microseconds from its ripple carry output. This carry bit is then used as an input to shift register, which shifts it to the QA, QB, and QC outputs on successive bit times to create three 1-microsecond pulses, one each on lines VR161, VR171 and VRT181. The trailing edge of VR161 coincides with the leading edge of VR171, etc. VR161, VR171, and VRT181 are used to create a 19-bit cycle for the serial data. The 19-bit cells accommodate 16 bits of data, one parity bit, and the sync pulse (two bit times). The parity bit is generated while VR161 is asserted, the sync pulse while VR171 and VRT181 are asserted. RSFTCLK is enabled between the trailing edge of VRT181 and the leading edge of VR161. It clocks the shift register in the parallel to serial converter, producing the serial data.

The timing generator also contains a flip-flop, the Q0 output of which is used to increment the address counter. The Q1 output is used to enable the operation of the shift registers in the parallel to serial converter. The CLEAR0 signal clears the counters and shift registers to 0.

3.3.3.5.1.7 Sequence Control

The sequence control module, like memory control, has four states. These four states control the timing of the transmission of 128-word blocks. When an INIT command is received, the sequence control enters state (1,0). This state is unstable, so on the next leading edge of the 1 MHz clock, the state changes to (1,1). During this state, also unstable, the address counter is cleared and the XMITDAT signal is asserted. XMITDAT enables serial transmission of data to the vehicle and enables the shift registers of the parallel to serial converter. VRC clear on power up circuitry has been added to the sequence control logic to prevent an extra VDT from being transmitted.

3.3.3.5.2 Low Byte Multiplexer (MUX)

Figure 3-22 is a block diagram of the low byte mux, status register and cross channel buffer interconnect.

The low byte multiplexer routes data from the IE, OE, or CIE onto the common data bus or to the cross channel multiplexer of the alternate channel. Three address bits from the DCU are provided to the low byte multiplexer for choosing data to be put on the common data bus. Three cross channel address bits are provided for selecting data to go to the cross channel multiplexer. The low byte multiplexer uses 8 pairs of multiplexers.

Each pair of multiplexers receives the same data. One multiplexer of the pair sources lines of the common data bus; the other multiplexer sources lines that go to the cross channel multiplexer. Two drivers are used for the address inputs. When N-MUX10 is asserted, signals 1ADRO21 and 1ADRO41 are used as inputs to the multiplexers to put 8 bits of data on the common data bus. When X-MUX10Z is asserted, XCADRO2 to XCADRO4 choose 8 bits of data to be put on a bus to the cross channel multiplexer. When neither N-MUX10 or X-MUX10Z is asserted, the multiplexers have high impedence outputs. A hard wired "OR" exists between the common data bus outputs and the cross channel buffer inputs. When COMDB001 to COMDB071 are in a high impedance state, the cross channel buffer may source them with data from the cross channel multiplexer of the alternate channel.

3.3.3.5.3 Cross Channel Buffer

When the common data bus has been put into a high impedance state, the cross channel buffer may put data from the alternate CIE channel onto it. MUXCLK1 is an input from CIE1 which latches the data from the holding register through a three-state driver and onto the common data bus. X-MUX10 and ENXCMX20 are I/O address decode lines from the DCU (alternate channel). The decoding takes place on CIE1.

3.3.3.5.4 Status Register

The status register is used to latch data from the common data bus to the multiplexer on the FDR board. The register is loaded when LDSTAT0 is asserted. The register may be loaded and read under software control. The status register hold the low eight bits of the status word. The high eight bits of the status word are held in a register on CIE4.

LOW BYTE MUX

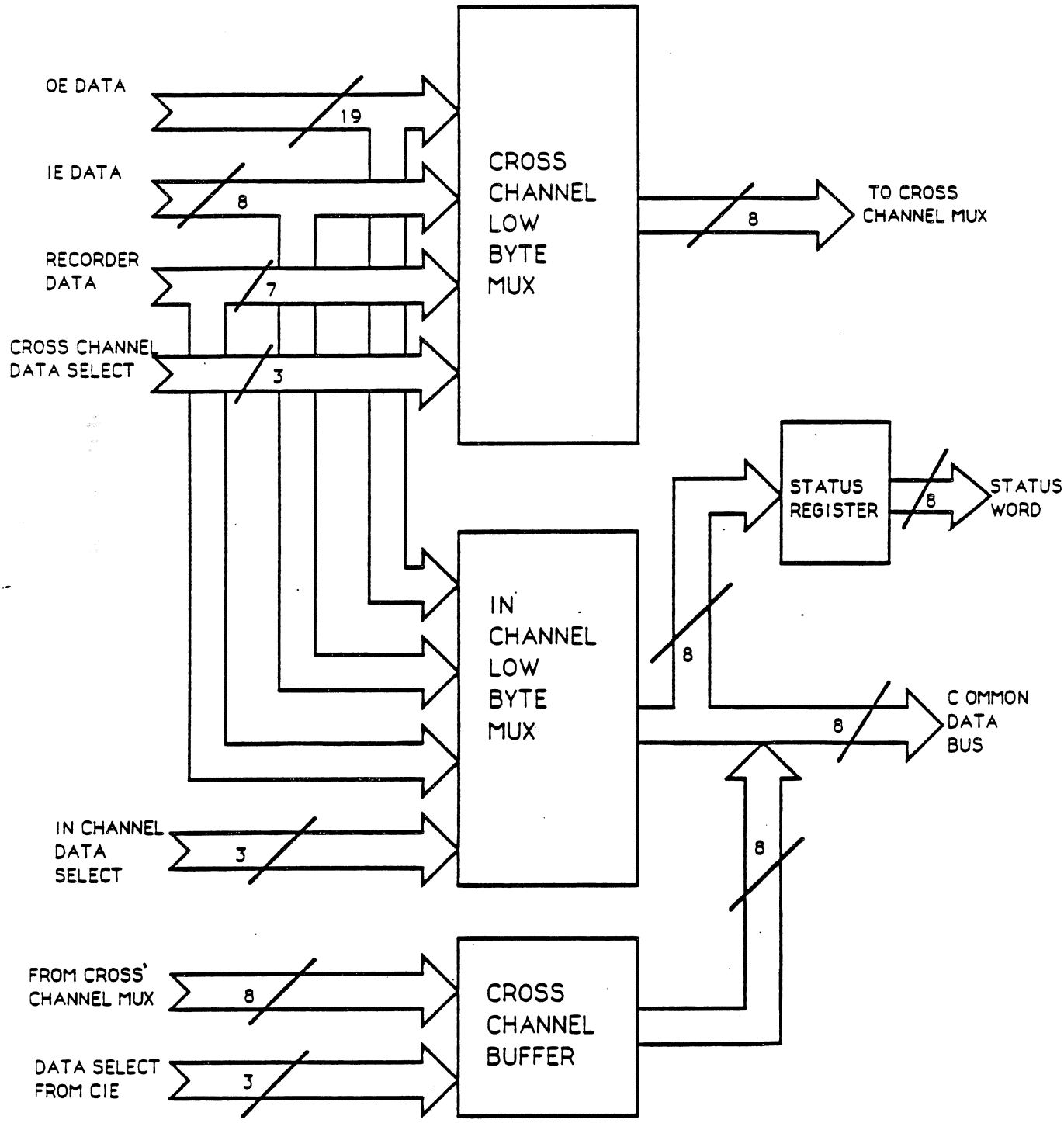


FIGURE 3-22

3.3.3.6 Computer Interface Electronics No. 6 (CIE6)

Computer interface electronics No. 6 schematic is on drawing 34069280 and the Printed Wiring Assembly (PWA) is on drawing 34069282. The CIE6 PWA contains the following controller functions:

- o Failure data recorder
- o I/O decode logic part 2
- o Status register buffer

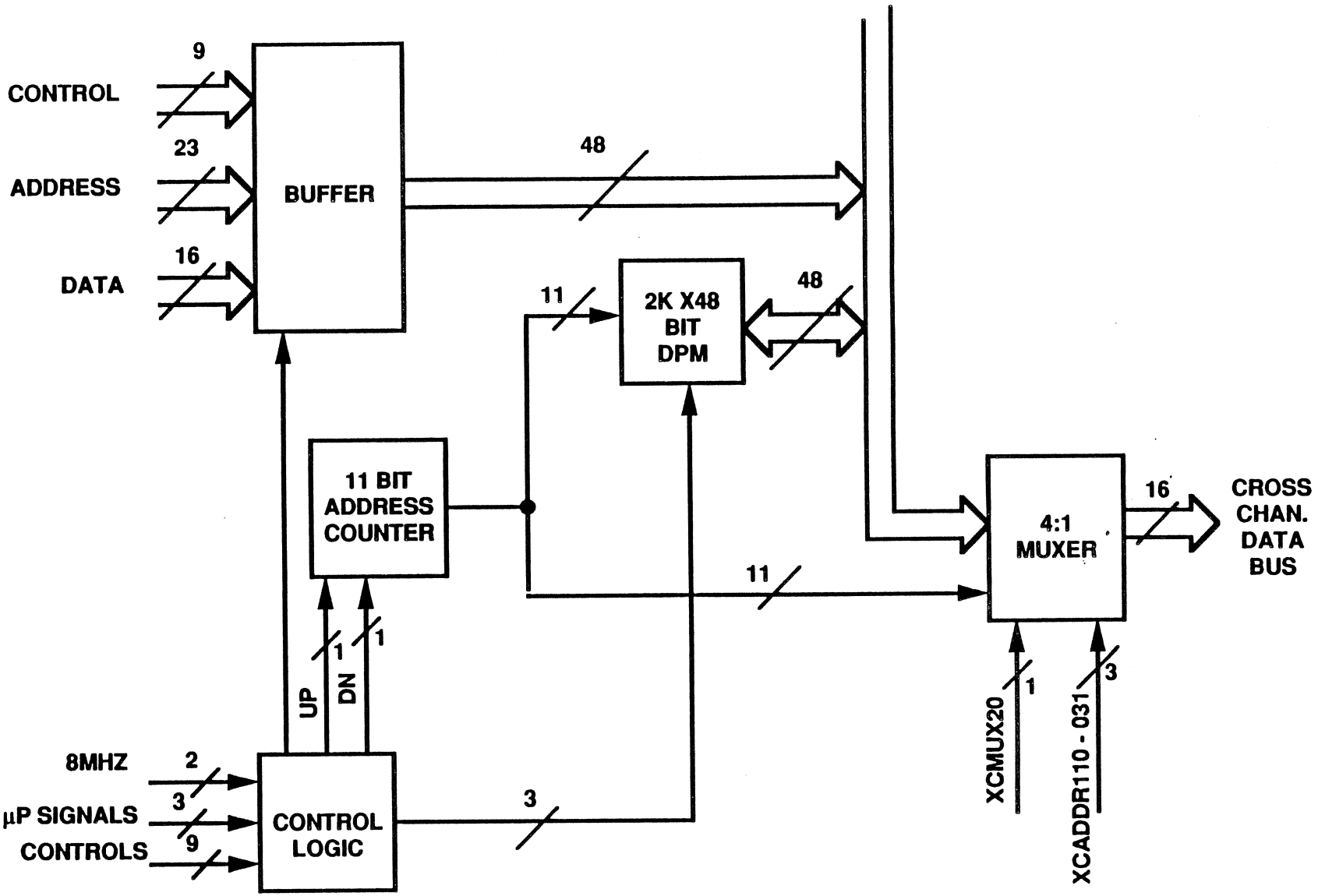
3.3.3.6.1 Failure Data Recorder (FDR)

The failure data recorder occupies a majority of the real estate on CIE6. The FDR's requirements are:

- o Provide storage for 2048, 48-bit words
- o Records all bus cycles of the No. 2 Microprocessor (monitor).
- o Inhibited writing for:
  - SCP error
  - Software command
  - Master Clear
  - GSE command
- o Enabled writing by:
  - Software command
  - GSE command
- o Provide battery hold-up same as main memory
- o Enable readout only by cross channel multiplexer

The Failure Data Recorder (FDR) stores DCU generated data into its memory on a continuous basis under control of internally generated signals. A Write signal generated by the FDR control logic loads data broadside into the 48-bit wide memory. The Write signal can increment an 11-bit memory address counter. During the record time, data from the DCU is enabled via tri-state buffers onto the memory bus of a memory device having common I/O pins. Upon detection of an error condition by circuitry on other cards, the contents of the memory are frozen. The data is then accessed by the cross channel computer, one 16-bit word at a time, in reverse order from storage by down counting the memory address counter using appropriately generated signals. The tri-state buffers are disabled and the memory outputs are enabled to access the data for formatting.

A block diagram of the FDR is shown in Figure 3-23.



FAILURE DATA RECORDER BLOCK DIAGRAM

FIGURE 3 - 23

3.3.3.6.1.1 Memory Address Generation

The address for the 2K memory, FRAD001 to FRAD101 is generated by three cascaded 4-bit up/down counters. The signals CASB0, 2LDSTRB0 and 2UDSTRB0 are gated together and used as the up-count clock. DECXFM0 is used for the down-count control occurring during memory readout. GRSTFM0 is used to initiate the card memory address generator for test purposes. The output of the address generation is buffered before being used as memory addresses. These addresses form part of the data enabled onto the cross channel data bus.

3.3.3.6.1.2 Input Data Buffering

Data from the DCU microprocessor is enabled through tri-state transparent latches onto the common I/O pins of the memory devices during the memory write sequence when WRINH1 is low, while the output of the memory devices are disabled by a high on FDROE0. Input data is latched by the DATEN1 signal.

3.3.3.6.1.3 FDR Memory Operation

The FDR Memory Devices use the address generated on card to access data for writing or reading. Data from the input latches are written into memory when the Write controls occur; in addition, the memory output is disabled and the memory chips are enabled when MEMSAVE1 is low. Data, address, and the other control signals must be applied so as to meet the timing requirements of the memory device.

The data and addresses applied to the memory device must be stable (and memory output disabled) prior to application of the Write control signals. Data is read from the memory devices when they are enabled (chip select active) and output enable is active (low). During a Read operation, the data input latches must be in their tri-state mode; data will be valid on the data pins within the maximum access time from stable address and control signal application.

3.3.3.6.1.4 Data Format/Bus Source Logic

The data stored in the FDR prior to an error condition detection is retrieved for analysis by the cross-channel DCU. Once the FDR memories have been accessed, control is provided to format the data from the memories and the on-card-generated memory address. In addition, the data is reformatted from parallel 48-bit stored word to six 16-bit words (the size of the data bus). Two select (address) bits are provided to the 4 to 1 multiplexers to provide the formatting function. These bits cycle through all binary combinations once for each 48-bit word read from (stored in) the FDR memory to generate four 16-bit words.

3.3.3.6.1.5 Power

FDR power is separate from the +5VDC logic power used for other functions of this board. The logic power can be removed and restored without affecting information stored in the FDR. However, the MEMSAVE1 signal must be asserted prior to power removal and negated after power restoration to protect FDR contents from alterations during +5VDC logic transitions. The FDR power (+5VOMEM) is diode "OR"ed on the board with two mutually exclusive external battery sources (GSEBATPW and 3V6BATPW).

3.3.3.6.2 I/O Decode Logic Part 2

The I/O Decode Logic Part 2 uses the three low order address bits from processor No. 2 and three decoded signals (ENGP40, ENGP50, ENGP60) from CIE1 to produce fifteen control signals for in channel use. The I/O decode logic also buffers the sixteen data bits (2DATXX) from processor No. 2 for use in driving data to the cross channel's output electronics.

3.3.3.6.3 Status Register Buffer

The Status Register Buffer is mechanized in two 16-bit buffers. Both 16-bit buffers have the 16-bit status register located on CIE4 and CIE5 as their input. One tri-state buffers output is directed to the common data bus (COMDBXX) by in channel control signals ASELO, NCMUX20 and 2ADRO11. The other tri-state output buffer's output is directed to the cross channel data bus by cross channel control signals XCMUX20, XCA31, XCA21 and XCADRO11 along with in channel signal ASEL0. Figure 3-24 is a block diagram of the status register buffer.

3.3.4 Input Electronics (IE)

The SSMEC Block II Input Electronic's primary function is to interface with the engine sensors analog signals and to convert these signals to digital words. The IE's secondary function is to convert controller internal analog signal to digital word for self test purposes.

In order to achieve its objective the IE must control:

- o The sequencing of the measurements
- o The storage of the measured data into predefined locations
- o Self test of the measurement devices and standards

Block II items to be measured are:

- o 27 temperature sensors
- o 36 pressure sensors
- o 4 flow sensors
- o 6 speed sensors
- o 12 RVDT position sensors
- o 15 LVDT position sensors
- o 6 vibration sensors
- o 6 igniter monitors
- o 44 Built In Test (B.I.T) signals/channel

Figure 3-25 is a simplified block diagram of the input electronics measurement system.

Table XII of DSHG8977A1 defines all of the addresses for input electronics measurements.

STATUS REGISTER BUFFER

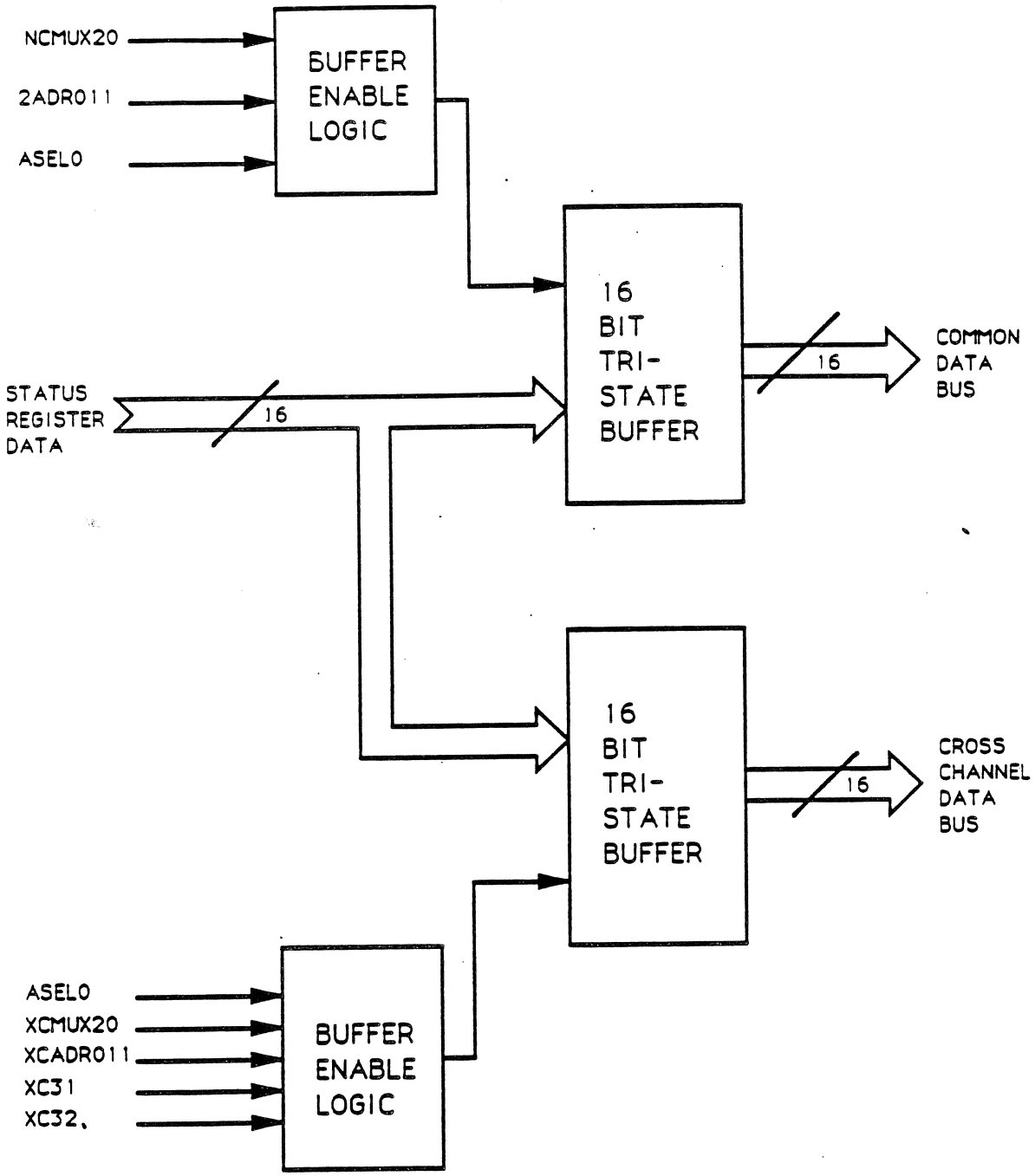
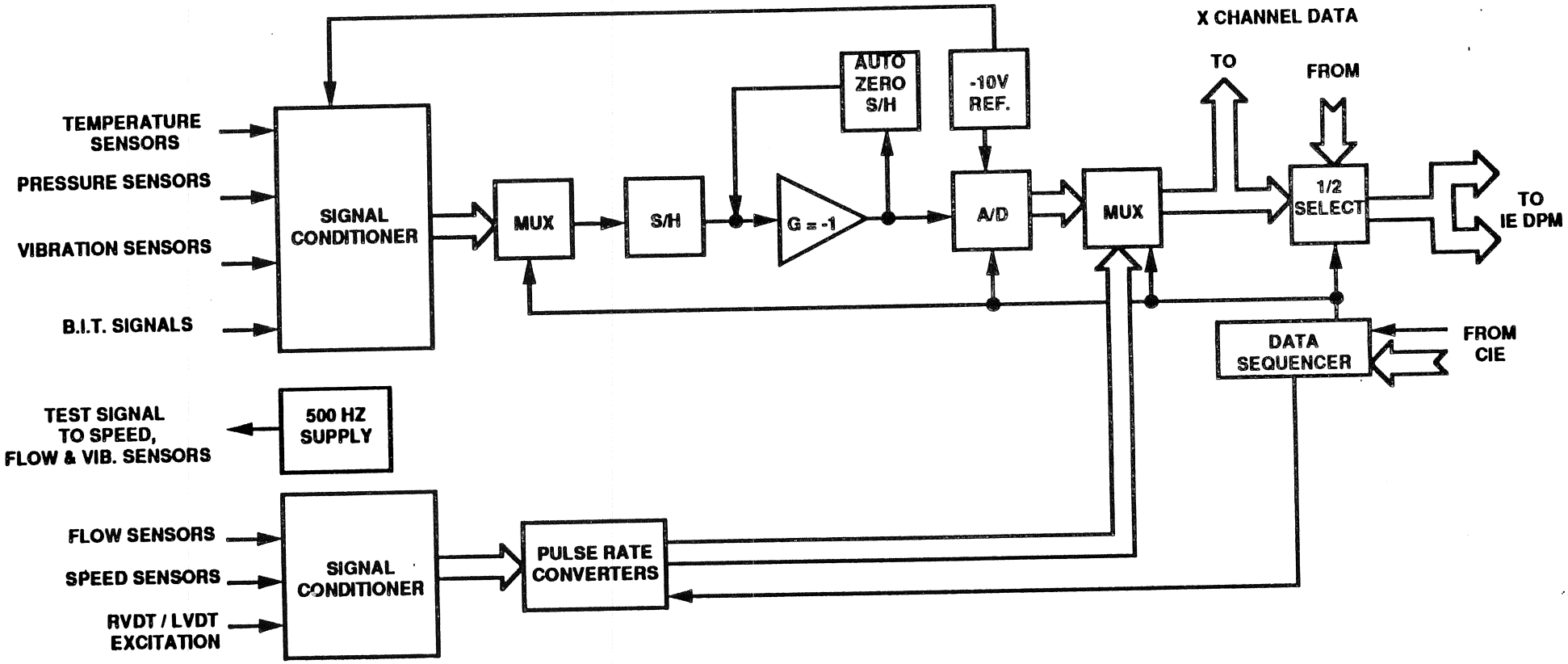


FIGURE 3-24



INPUT ELECTRONICS BLOCK DIAGRAM

FIGURE 25

3.3.4.1 Input Electronics No. 1 (IE1)

The Input Electronics Printed Wiring Assembly No. 1 provides the interface between the thermal sensor elements and the controller's analog to digital conversion system. The assembly is composed of:

- o 15 bridge networks
- o 24/1 differential multiplexer
- o 25.83 V/V gain, temperature amplifier
- o Mux control logic
- o Out of range logic
- o Sensor check logic and loads

The assembly must, in addition to handling the normal engine operational interface, also support two additional interfaces. These interfaces are:

- o Propellant drop mode - in this mode T3 and T4 are routed around the temperature amplifier to the high level mux and all other temperatures maintain their normal routing.

- o Sensor check mode - In this mode the bridges and sensors are checked by paralleling one leg of the bridge with a known resistance that will cause the converted output to go to 50% of nominal full scale.

Figure 3-26 and 3-27 are block diagrams of IE1. The schematic for IE1 is drawing No. 34076193 and the assembly drawing is 34076195.

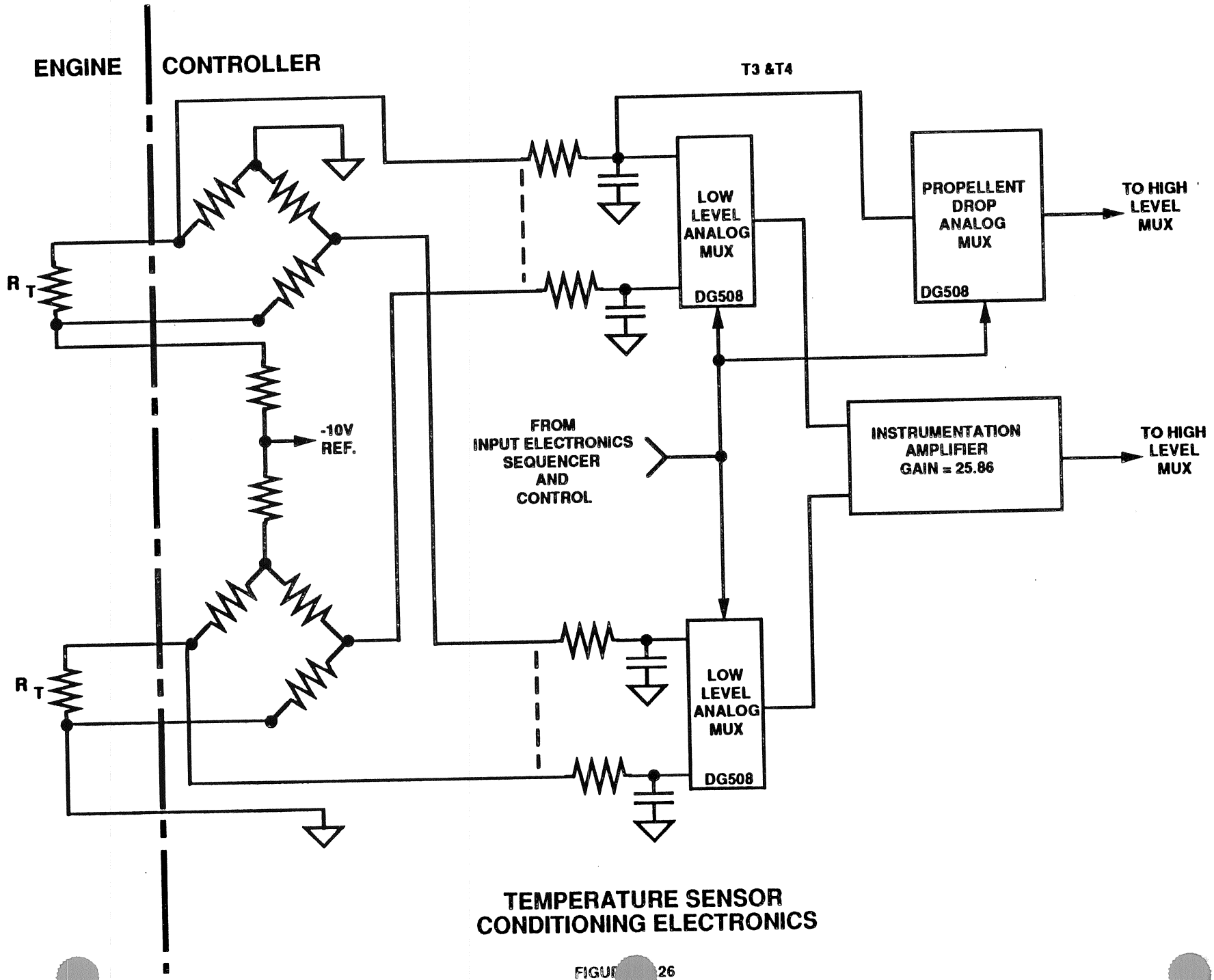
3.3.4.1.1 Bridge

There are five bridge types in the SSMEC Block II Controller. The five bridge types are shown in Figures 3-28, 3-29 and 3-30. The Differences in the bridges are due to the system requirements that:

- o The sensors have different R_O values and/or ranges of measurement for a given R_O value.

- o A short or an open on any sensor or excitation line must cause the bridge output to be outside the normal range of readings for that bridge.

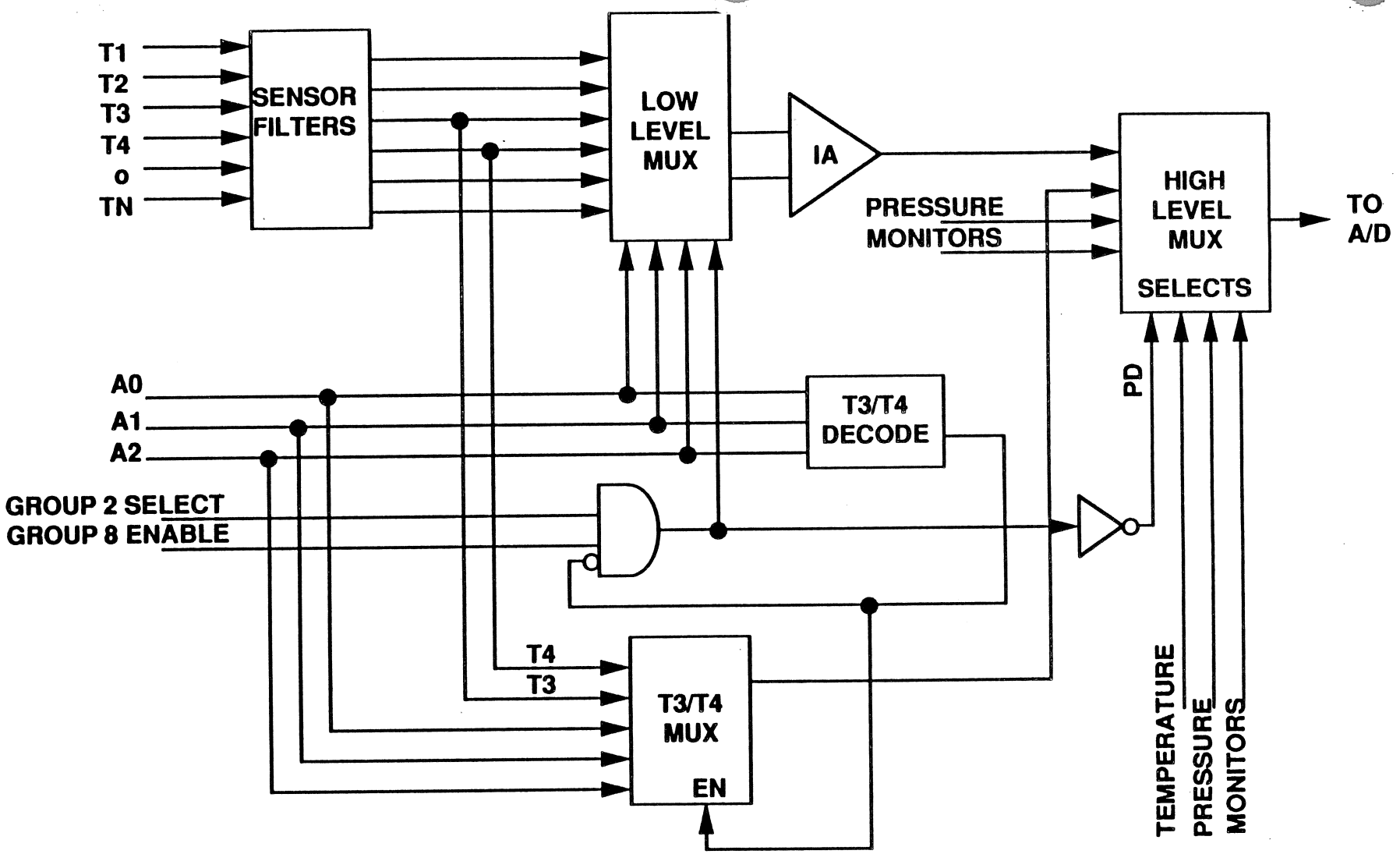
- o One bridge type shall have a variable configuration such that it can be used for any other bridge configuration or as the input for a thermal couple amplifier. Figure 3-30 shows the variable configuration.



(132)

TEMPERATURE SENSOR CONDITIONING ELECTRONICS

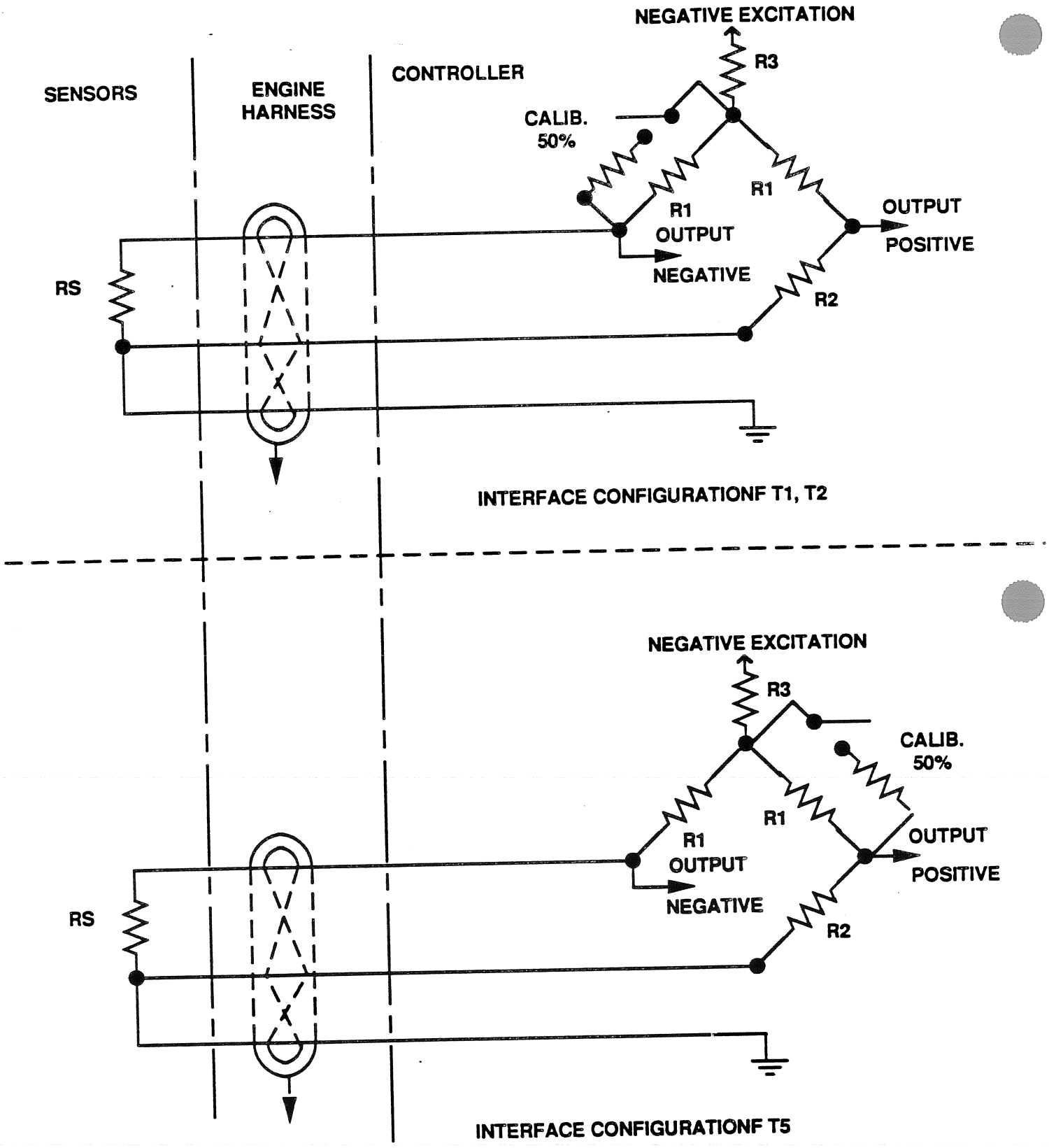
FIGURE 26



(133)

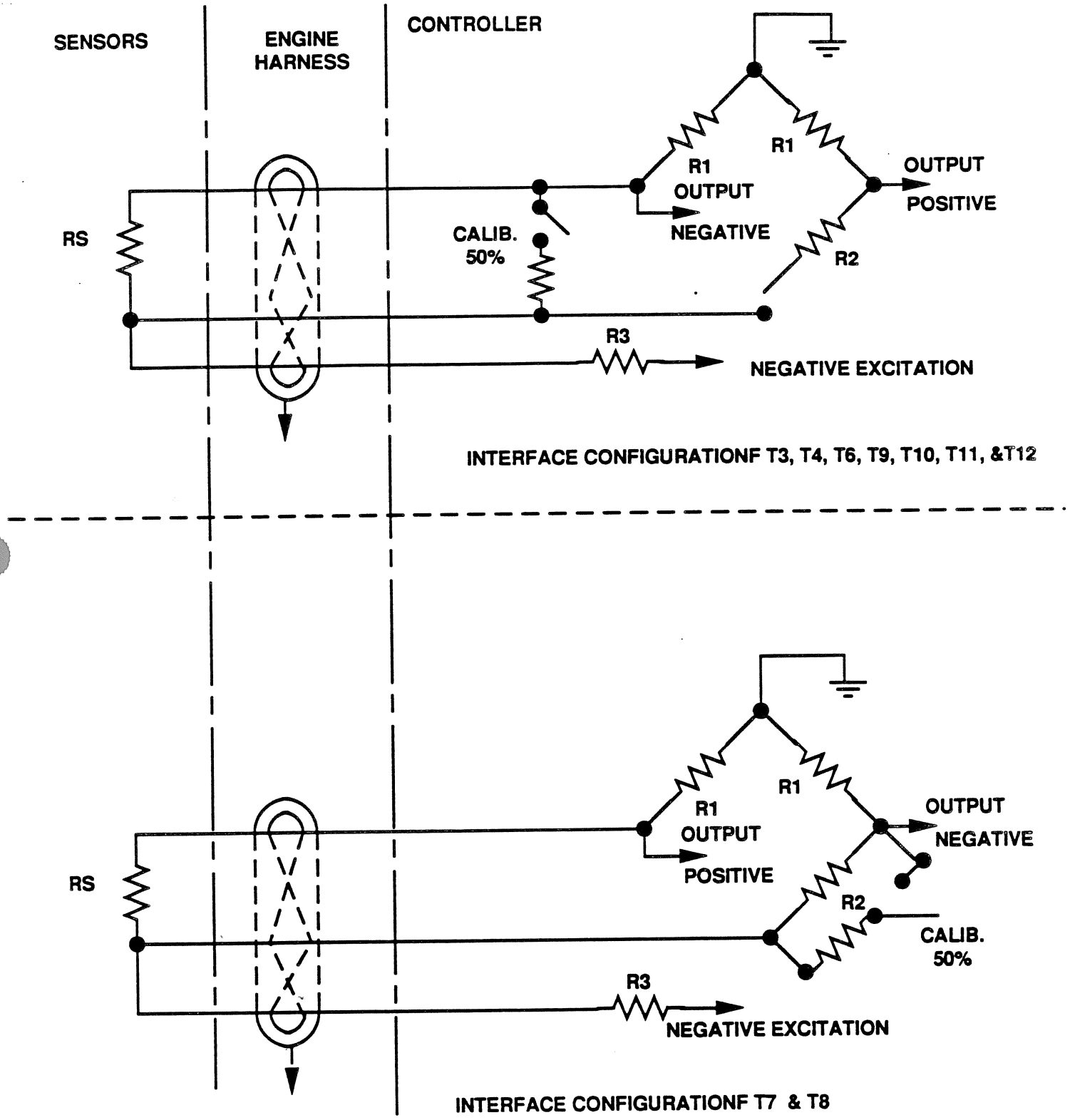
GROUP 2 TEMPERATURE SENSOR PROCESSING (PROPELLANT DROP MODE)

FIGURE 3 - 27



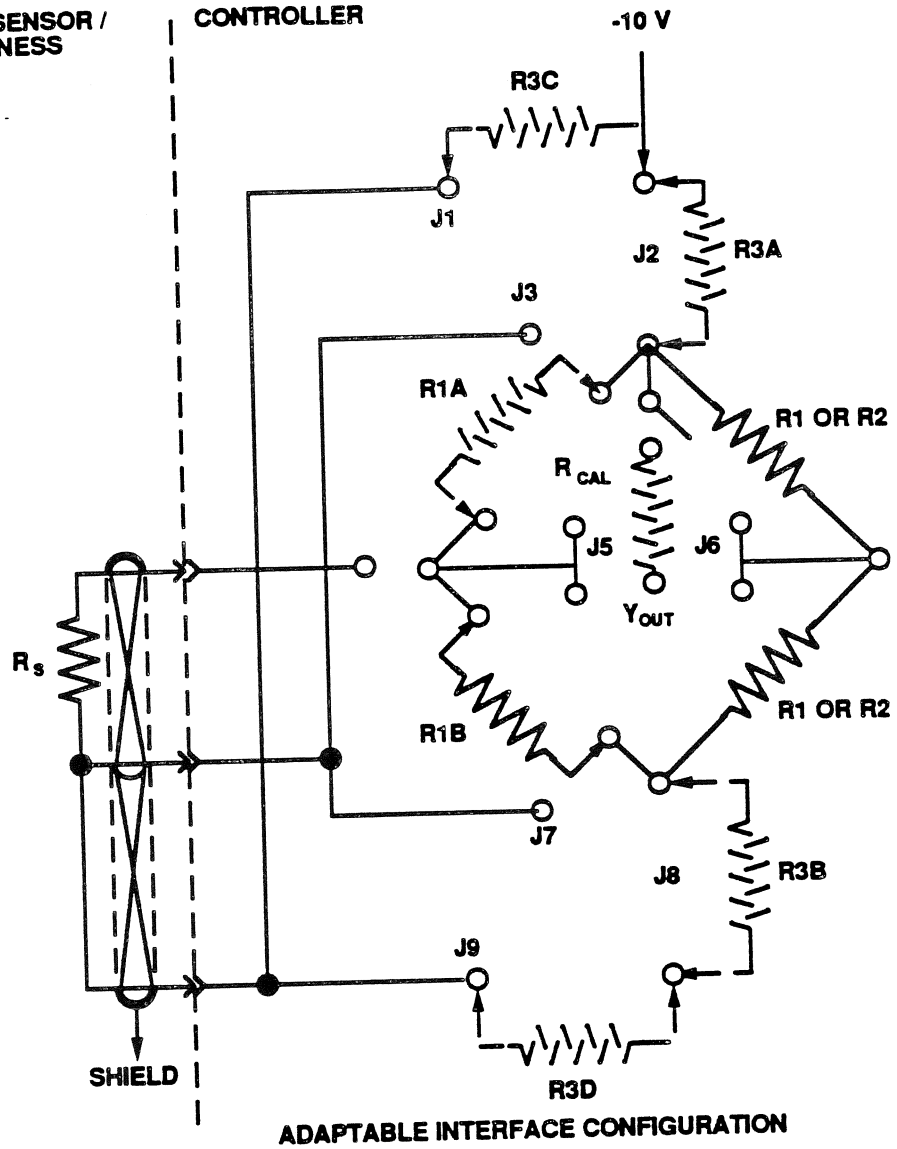
TEMPERATURE SENSORS TO BRIDGE INTERFACE

FIGURE 3 - 28



TEMPERATURE SENSORS TO BRIDGE INTERFACE

FIGURE 3 - 29



ADAPTABLE INTERFACE CONFIGURATION

T14 INTERFACE CONFIGURATION

R1	R1A	R1B	R2	R3A	R3B	R3C	R3D	R CAL
X		X	X			X		X

J1	J2	J3	J4	J5	J6	J7	J8	J9
		X	X	X			X	

T13, T15 INTERFACE CONFIGURATION

R1	R1A	RT1B	R2	R3A	R3B	R3C	R3D	R CAL
X	X		X	X				X

J1	J2	J3	J4	J5	J6	J7	J8	J9
			X	X		X		X

X DESIGNATES RESISTOR AND JUMPER LOCATION AND CONFIGURATION

ADAPTABLE SENSOR TO BRIDGE INTERFACE CONFIGURATION

FIGURE 3 - 30

Another feature of the bridges is that the excitation voltage used on the bridges is the same excitation voltage used for the A/D reference. This removes the excitation as an error source since the A/D would track the variations of the excitation voltage.

3.3.4.1.2 24-1 Differential Multiplexer (Mux)

The 24-1 Mux is subdivided into 3 groups (8,9,10) of 8 differential signals. The design of this mux is such that when temperatures are being read, the readings always start with group 8 and go straight through to group 10. This should be done to insure that the auto zero circuit is updated and that the A/D self checks for temperature can be made.

3.3.4.1.3 Temperature Amplifier

The temperature amplifier is a differential input instrumentation with a gain of 25.83 V/V. The amplifier has both offset compensation and common mode gain compensation built-in.

3.3.4.1.4 Mux Control Logic

The IE1 Control Logic takes control signals from IE4 and IE5 and turns them into groups 8,9 and 10 Mux Enables, Sensors Check 1 and 2 signals; the Propellant Dump signals; and the High Level Mux on IE2 Enable. Sensors Check 1 enables the testing of the sensors 50% reading and Sensors Check 2 enables the Propellant Dump test. For either sensors check to be enabled both the A channel and the B channel must both command the same sensors check before the check can be run.

3.3.4.1.5 Out of Range Logic

The out of range logic is simply a double pole switch on IE1 that grounds the inputs to the temperature amplifier any time IE2 detects the input to the A/D out of range (±5V). The switch is enabled by a signal from IE2.

3.3.4.1.6 Sensor Check Load

The Sensor Check Load is a resistor in series with a switch that when closed parallels the resistor with one leg of the bridge. The location of the resistor (calib) for each bridge type is shown in Figures 3-28, 3-29 and 3-30. The switch is enabled by the sensors check one signal.

3.3.4.1.7 Thermal Couple Interface

Bridge inputs T13, T14 and T15 are designed such that they can be used to support the use of either R.T.D. or thermocouple sensors. The R.T.D. connections are shown in Figures 3-28, 3-29, 3-30. Figure 3-31 shows the connection for thermocouple sensors. IE1 has current limited ±15V voltage sources that are brought out of the controller for use by the thermocouple signal conditioner. The 10K ohm load and test switch for testing a thermocouple signal conditioner are also on IE1.

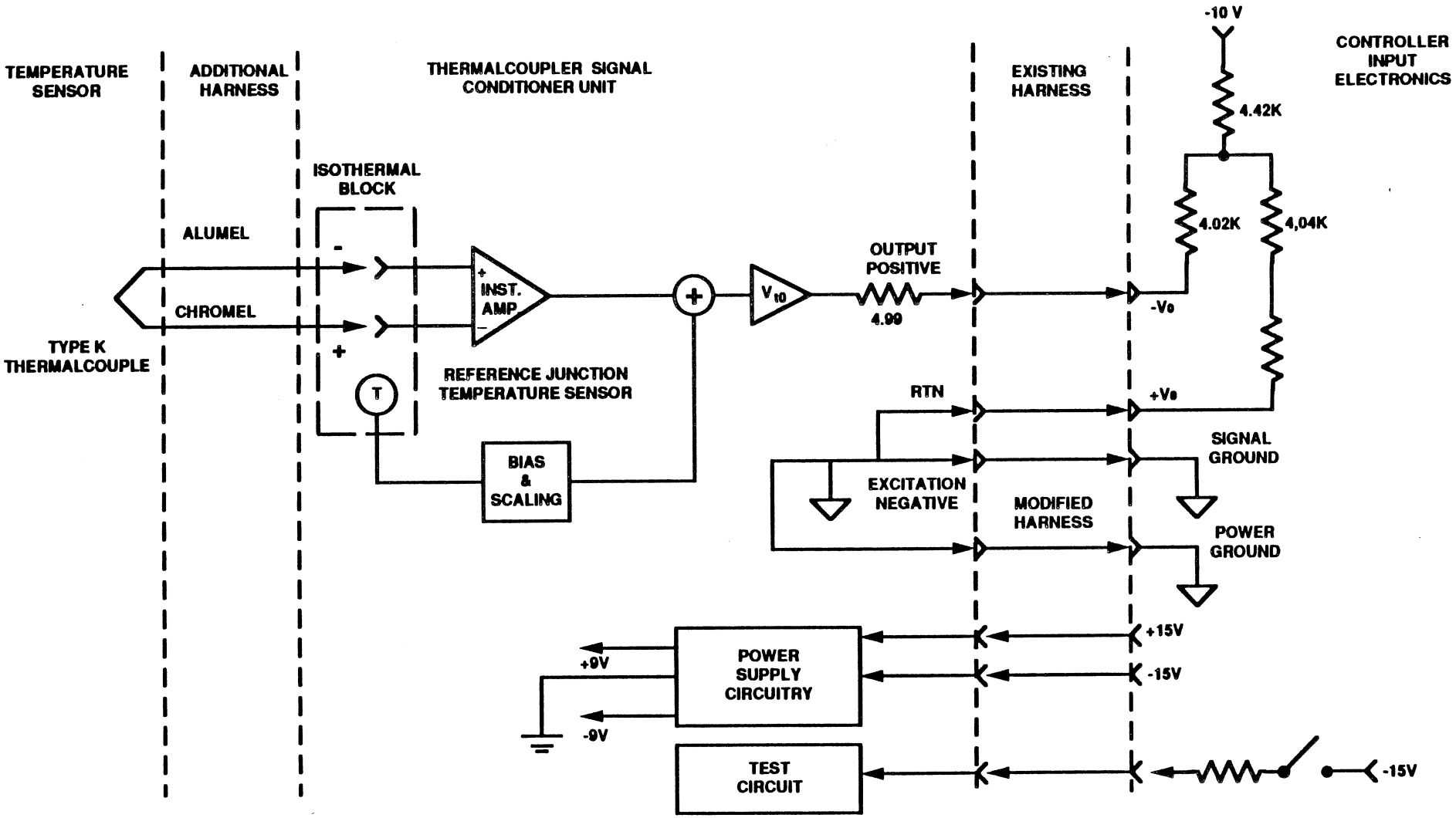
3.3.4.2 Input Electronics No. 2 (IE2)

Input Electronics No. 2, shown in Figure 3-32, primary function is to interface the pressure sensing elements of the engine with the controller. Secondary functions are to convert the analog signals from the temperature sensors, pressure sensors and Built In Test (B.I.T.) into 12-bit digital words and to supply the excitation voltage to the temperature and pressure sensors. The IE2 assembly, 34069252, whose schematic is 34069250 contains the following functions:

- o 32/1 differential pressure multiplexer
- o 150.33 V/V,gain amplifier
- o 4 to 1 high level multiplexer
- o Auto zero/track and hold
- o A/D converter
- o Over range detector
- o -10 volt reference
- o Sensor test circuit

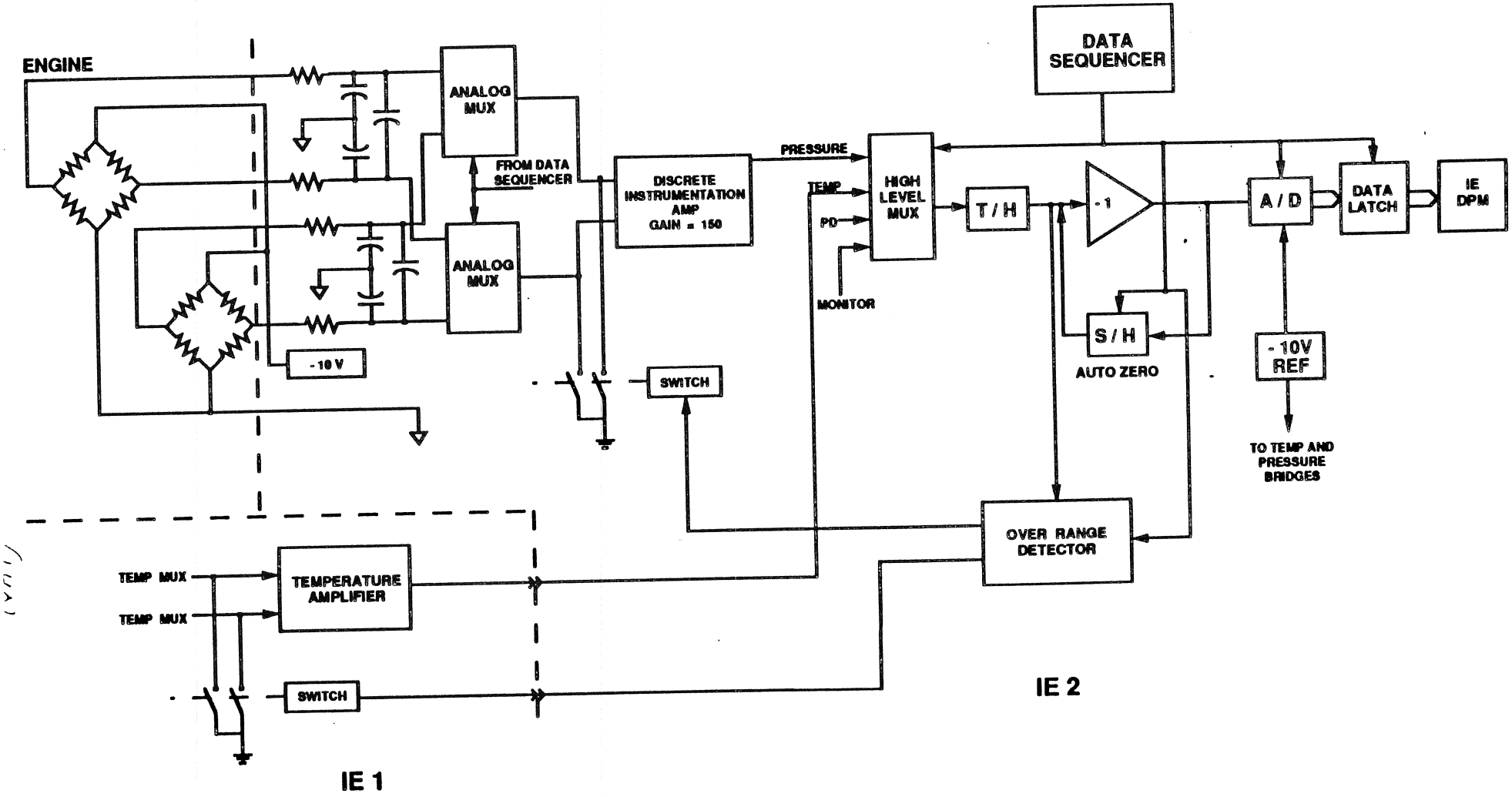
3.3.4.2.1 32/1 Differential Multiplexer

Up to 19 Pressure Sensor Outputs are sent to each IE2 PWA. On the IE2 PWA each of these outputs is routed a low pass anti-aliasing filter to a specific input of the 32 to 1 differential multiplexer. The differential output of this pressure mux is sent to the pressure amplifier. Which input is selected by the Mux to be sent to the amplifier is controlled by the IE Address and Control Logic. This logic selects one of eight sensors from one of four groups (12, 13, 14, 15). When reading any pressures the conversions should always start with Group 12 and sequence to Group 15. This is done in order to null out offsets and to self-test the measurement system. Figure 3-33 is the diagram of a typical pressure sensor.



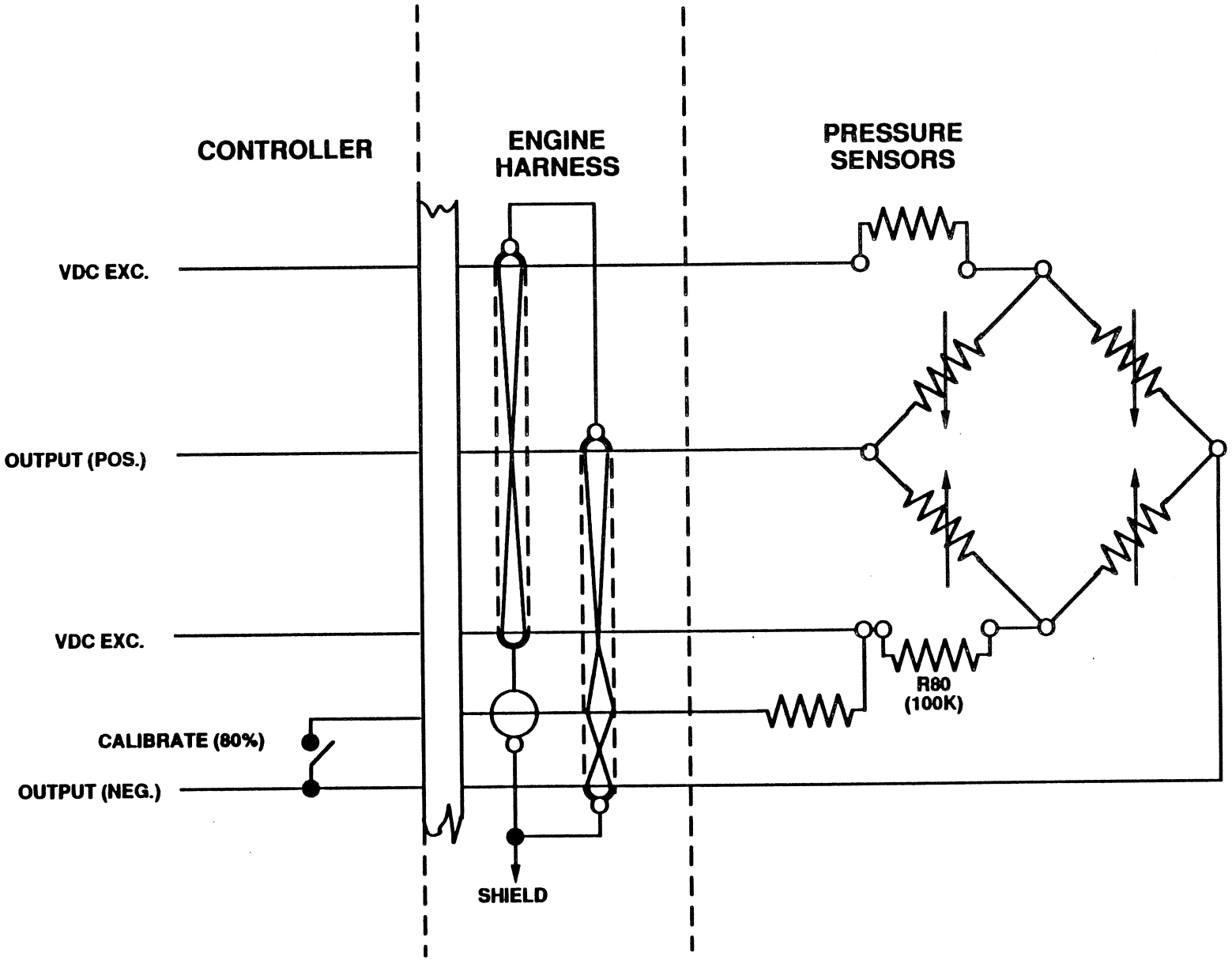
CONTROLLER TO THERMOCOUPLE TEMPERATURE SENSOR INTERFACE

FIGURE 3 - 31



INPUT ELECTRONICS No 2

FIGURE 3 - 32



PRESSURE SENSOR INTERFACE

FIGURE 3 - 33

3.3.4.2.2 Sensor Test Circuit

The Pressure Sensor Test (calibration) circuit function is similar to the temperature sensor. It is enabled by channel A and B Sensor Check One signals and places a resistor in parallel with one leg of the pressure bridge. In the pressure system the switch is on IE2 and the resistor is in the pressure sensor (Ref. Figure 3-33).

3.3.4.2.3 Pressure Amplifier

The Pressure Amplifier is an instrumentation amplifier with a gain of 150.33 V/V. The input to the amplifier is connected to the output of the 32/1 mux and the amplifier output is connected to the Hi Level Mux Pressure Input.

3.3.4.2.4 4/1 Hi Level Mux

The 4/1 Hi Level Mux is used to select either the Pressure amplifier output, the Temperature amplifier output, the Propellant Drop Mux or the Monitor Mux output for conversion by the A/D converter. The input to be converted is selected by control logic on IE4/5 and IE1. The output of the Hi Level Mux goes to the input of the Track and Hold amplifier.

3.3.4.2.5 Auto Zero Track and Hold

The Track and Hold portion of the conversion electronics tracks the output of the Hi Level Mux until the ADHOL0 signal is asserted by the IE Control Logic. When ADHOL0 is asserted, the Track and Hold circuit holds the value of the voltage on its input at the time of assertion on its output. Regardless of input variation the output is held until ADHOL0 is negated. The output of the Track and Hold circuit is routed to the Auto Zero Sum Amp and the Over Range Detector.

The Auto Zero circuit consists of a Sample and Hold circuit, an Analog Switch, and an Inverting Sum Amp. The output of the Inverting Sum Amp goes to the A/D converter input and the input to the Auto Zero Sample and Hold circuit.

The Sample and Hold tracks the output of the Sum Amp until AZROENA0 is asserted. When AZROENA0 is asserted the Sample and Hold circuit holds the value of the voltage on the Sum Amp's output on the Sample and Hold's output and it also closes a switch which connectors the Sample and Hold output to the Summing Network on the input to the Sum Amp. This condition remains as long as AZROENA0 is asserted.

When AZROENA0 is negated the sum amp will act as a simple inverter. AZROENA0 is asserted after the measurement of the first word in Group 9 or Group 12 and it is negated after the last measurement in Group 10 or Group 15. Groups 9 and 10 are temperature measurements and Group 12 through 15 are the pressure measurements. The first measurement in the temperature and pressure groups is ground, and any voltage out of the Sum Amp when reading ground is due to system offsets. Feeding the inverse of these offsets back to the Sum Amp input will zero out the offset for subsequent readings as long as AZROENA0 is asserted.

3.3.4.2.6 A/D Converter

The Block II A/D Converter is a 12-bit A/D converter that has a conversion range of ±5VDC. The output is in "2"s complement.

Hex Output		Input Voltage
7FF	=	+4.9976
000	=	0.0000
800	=	-5.0000

The A/D converters output is put on the 16-bit data bus in the three most significant hex digits. The lease significant digit is forced to a hex eight. Therefore, the data bus reading for the analog signals will be:

Input Voltage	Data Bus
+4.9976	7FF8
0.0000	0008
-5.0000	8008

3.3.4.2.7 Minus Reference

The -10V Reference supply is an extremely accurate and stable voltage source the initial set requirements are -10.000 ± .001VDC. The -10V DC is the reference for the A/D converter and the excitation for the temperature and pressure sensors.

3.3.4.2.8 Over Range Detector

The Input Electronics has an Over Range detector on the temperature and pressure readings. Opens on the sensor lines or shorts of the excitation voltage to a sensor line will drive the temperature or pressure measurement paths beyond the maximum measurement range. When this happens without an Over Range circuit the next reading in the sequence is corrupted.

The Over Range circuit protects the temperature and pressure readings by monitoring the input of the Sum Amp. Any time the Sum Amp input exceeds ±5V on a temperature or pressure reading the Over Range circuit is activated and ADHOLD0 is asserted. Activating the Over Range circuit enables a switch to ground on either the Temperature or Pressure amplifier's differential input lines depending whether temperature or pressures are being read. Grounding the input to the amplifier zero's the enabled sensor input lines from sensor input to Track and Hold amplifier, which prevents circuit saturation. At the same time the A/D output indicates an over range because the Track/Hold amplifier output is holding the over range voltage. The Over Range circuit is released when ADHOLD0 is negated.

3.3.4.3.1 Monitor Mux

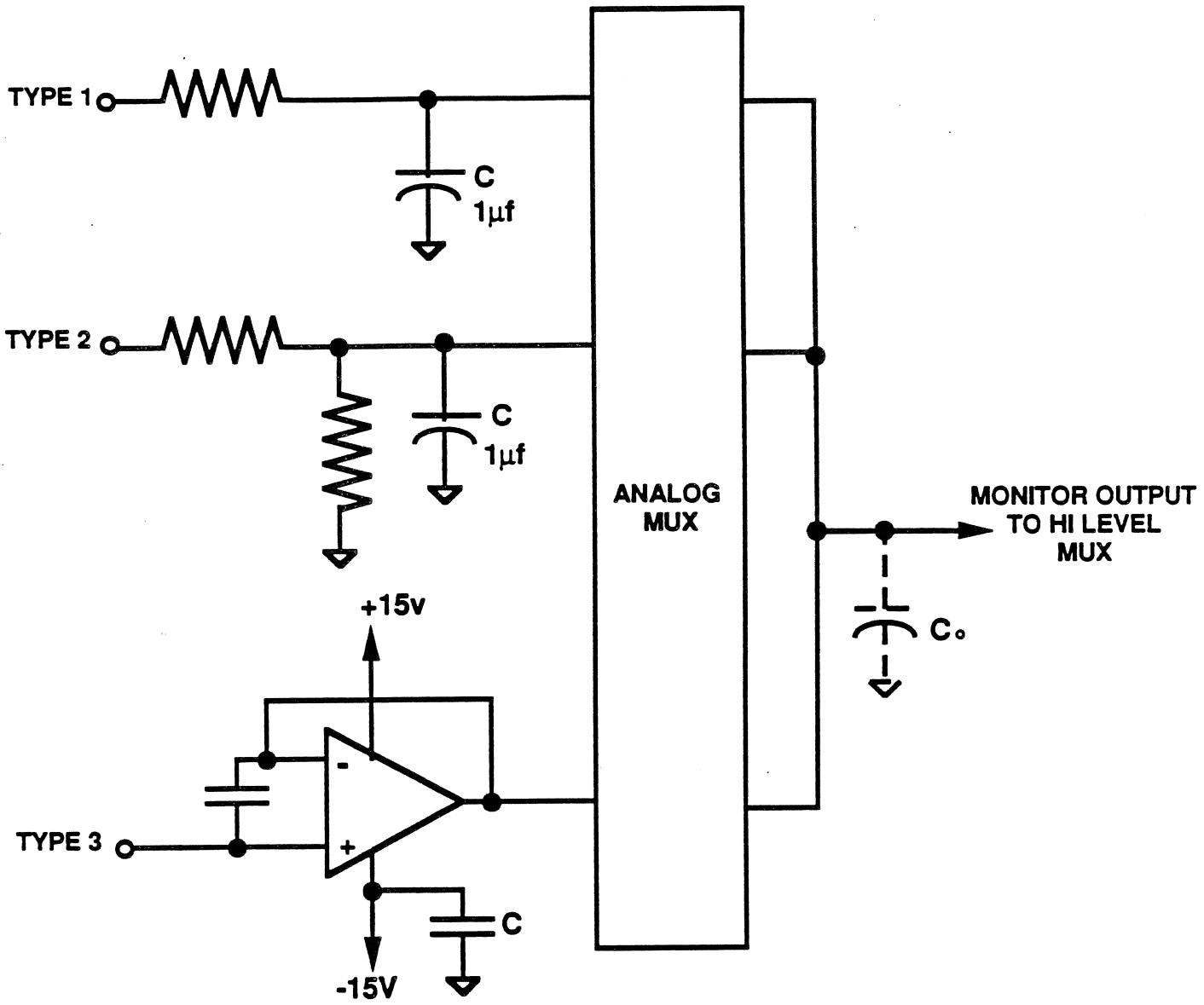
The Monitor Mux is a 56/1 non-differential input multiplexer. The Mux inputs Groups 1 through 7 into the Hi Level Mux on IE2. The types of signals handled by this Mux are:

- o Actuator positions
- o Valve positions
- o OE D/A outputs
- o All power supply voltages
- o Vibration Signal Processing Electronics (VSPE)

The input to the monitor Mux is through one of 3 types of input circuit shown in Figure 3-34. The input types are:

- o Type 1 - A simple low pass first order filter
- o Type 2 - A resistor divider network incorporating a low pass first order filter.
- o Type 3 - A unity gain fast slew rate amplifier

Type 2 inputs are used for all input signals whose amplitude fall outside the ranges of +0.5V to +4.5V or -0.5V to -4.5V. The resistor values are selected to form a divider that will place the signal within one or the other of these brackets. The capacitor is 1.0 microfarad so that it will be very large with respect to C_o the output capacitance of the Mux. C being very large with respect to C_o reduces the error caused by charge transfer between C and C_o.



BIT SIGNAL PROCESSING

FIGURE 3 -34

(69)

(145)

The Type 3 input is used for the D/A converter feedback. The system has a requirement for fast confirmation of the D/A setting which can be from 0 to +10 volts in magnitude. The divider used to put the feedback in the +0.5V to +4.5V range has high resistance to prevent loading the D/A converter. Because of the high source resistance the feedback had either timing or charge transfer problems when using a Type 2 input. The amplifier eliminated the problem by isolating the source from C_O and providing fast slew rates.

3.3.4.3.2 Pulse Rate Counter (PRC)

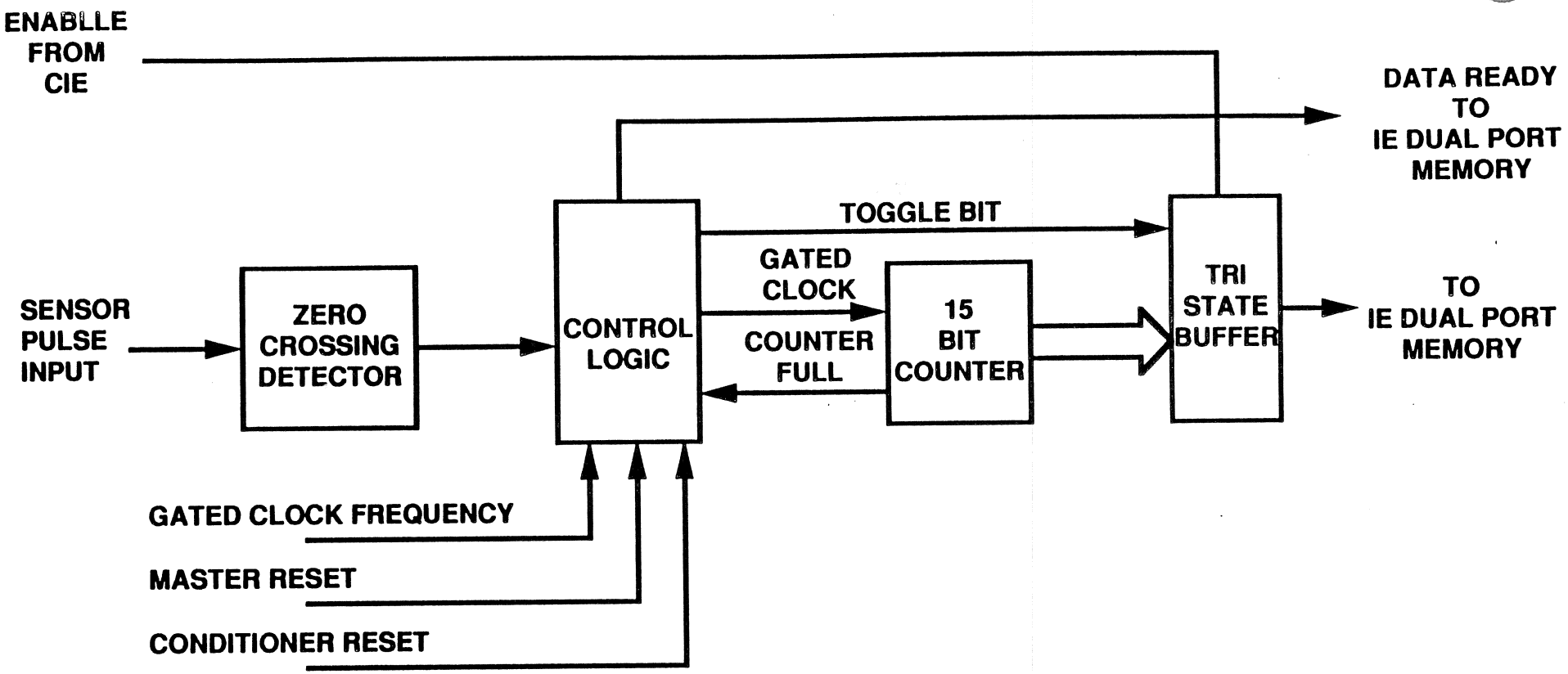
The IE3 PWA contains 2 flow rate counters that are driven by engine flow meters. The flow rate counters function similarly to the time interval counters in that they measure the time between pulses from the meter. The flow rate counters count a 666 KHz signal in a 15-bit binary counter. The counter counts the number of 666 KHz pulses between negative going edges of the flow meters output wave form. The pulse rate converter accuracy for the flow sensor data as:

- o ±0.19 Hz for frequencies from 12 Hz to 75 Hz
- o ±0.25 % of actual frequency from 75 Hz to 340 Hz

The pulse rate converter circuits have a simple first order low pass filter at their inputs. The break or corner frequency is 127 ± 32 Hz.

Pulse rate converter outputs are generated for sensor outputs greater than 75 mV peak. A comparator circuit is used for signal level detection.

The MSB (bit 16) of the flow reading is a toggle bit which changes state every time the counter contents are updated (stops a count sequence). Count sequences are stopped by the second pulse from the flow meter or a counter over flow. A new count sequence will not start until the current contents are read by the IE DPM. Figure 3-35 is a block diagram of the PRC.



NOTE:

THE GATED CLOCK FREQUENCY IS:

- o 666KHZ FOR FLOW MEASURMENTS
- o 500K HZ FOR SPEED MEASURMENTS
- o 2.0 M HZ FOR BIT MEASUREMENTS

SPEED/FLOW/BIT SIGNAL CONDITIONERS

FIGURE 3 - 35

3.3.4.3.3 500 Hz Supply

IE3 also contains a 500 Hz Power Supply, which produces a 500 Hz sine wave 1.22 VRMS. This signal is used to test other functions such as the PRC and accelerometers.

The 500 Hz circuitry takes the 2 KHz signal and divides it by 4 before sending the square wave to a shaping circuit that converts the signal into a 1.22 V_{RMS} sine wave with the following characteristics:

- o Amplitude - 1.22 VRMS ± 5%
- o Frequency - 500 Hz ± 5 Hz
- o Harmonic Contents - ≤ 6%
- o Current Limit - ≤ 25 milliamps

This Sine Wave output is controlled by two analog switches connected in series. To prevent a single point failure one switch is controlled by the in channel sensor check signal and powered with in-channel -15VDC while the other switch is controlled by the cross channel sensors check signal and is powered by cross channel -15VDC. Using this approach the only time the 500 Hz can be applied is when both channels -15VDC supplies are functioning. Figure 3-36 is a block diagram of the 500 Hz supply.

3.3.4.3.4 PRC Test

The flow PRC and flow meter windings are checked by injecting the 50[illegible] signal on to the winding of the flow sensor primary and monitoring the secondary windings output. Figure 3-37 shows the test setup for speed and/or flow.

3.3.4.4 Input Electronics No. 4

The Input Electronics No. 4 Printed Wiring Assembly (PWA) schematic 34069262 and Assembly 34069264 contain four functions:

- o 3 speed, Pulse Rate Counters (PRCs)
- o Speed/Flow clock generator
- o PRC to data sequencer interface
- o In-channel/cross-channel IE data Mux

500 HZ SUPPLY

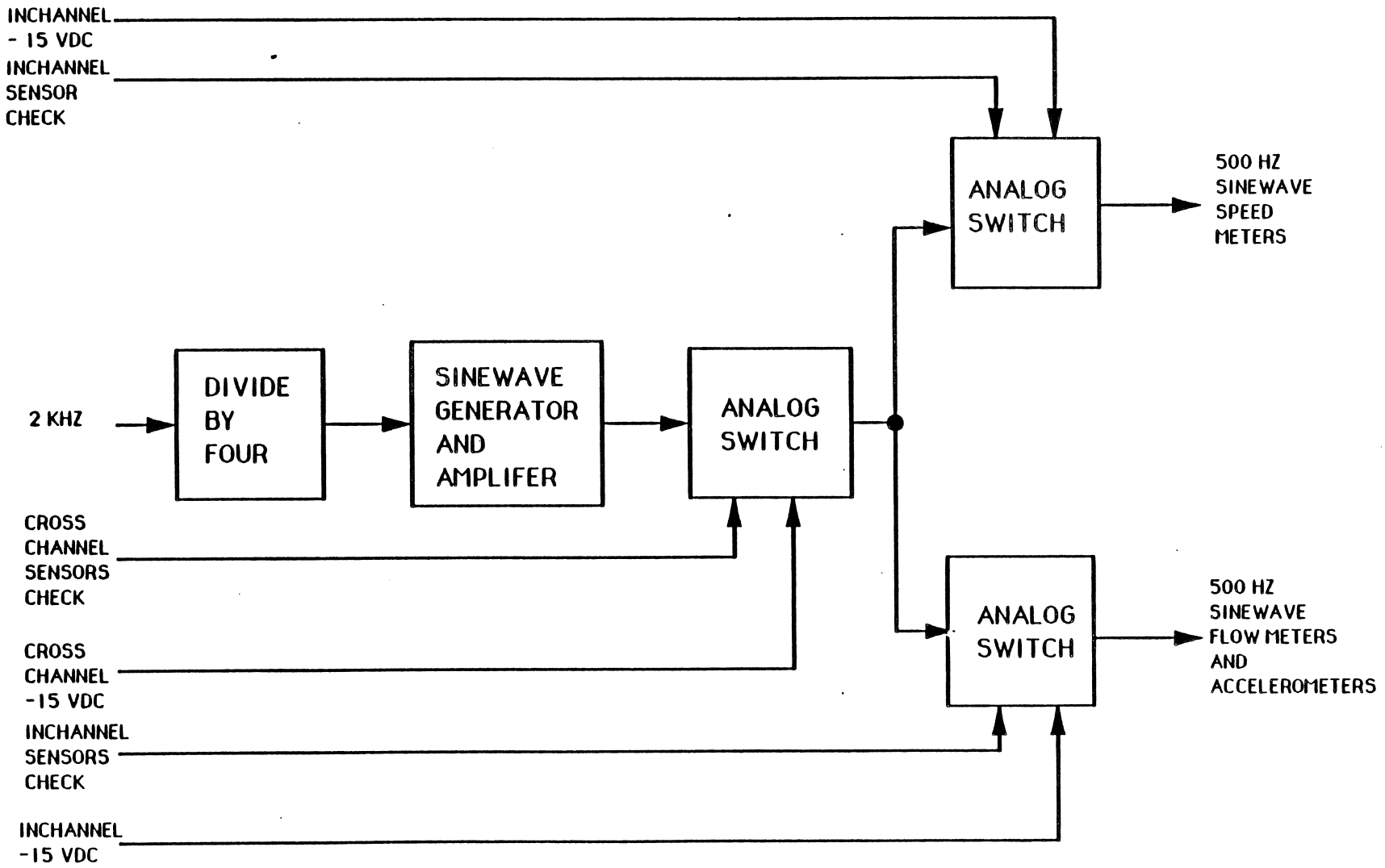
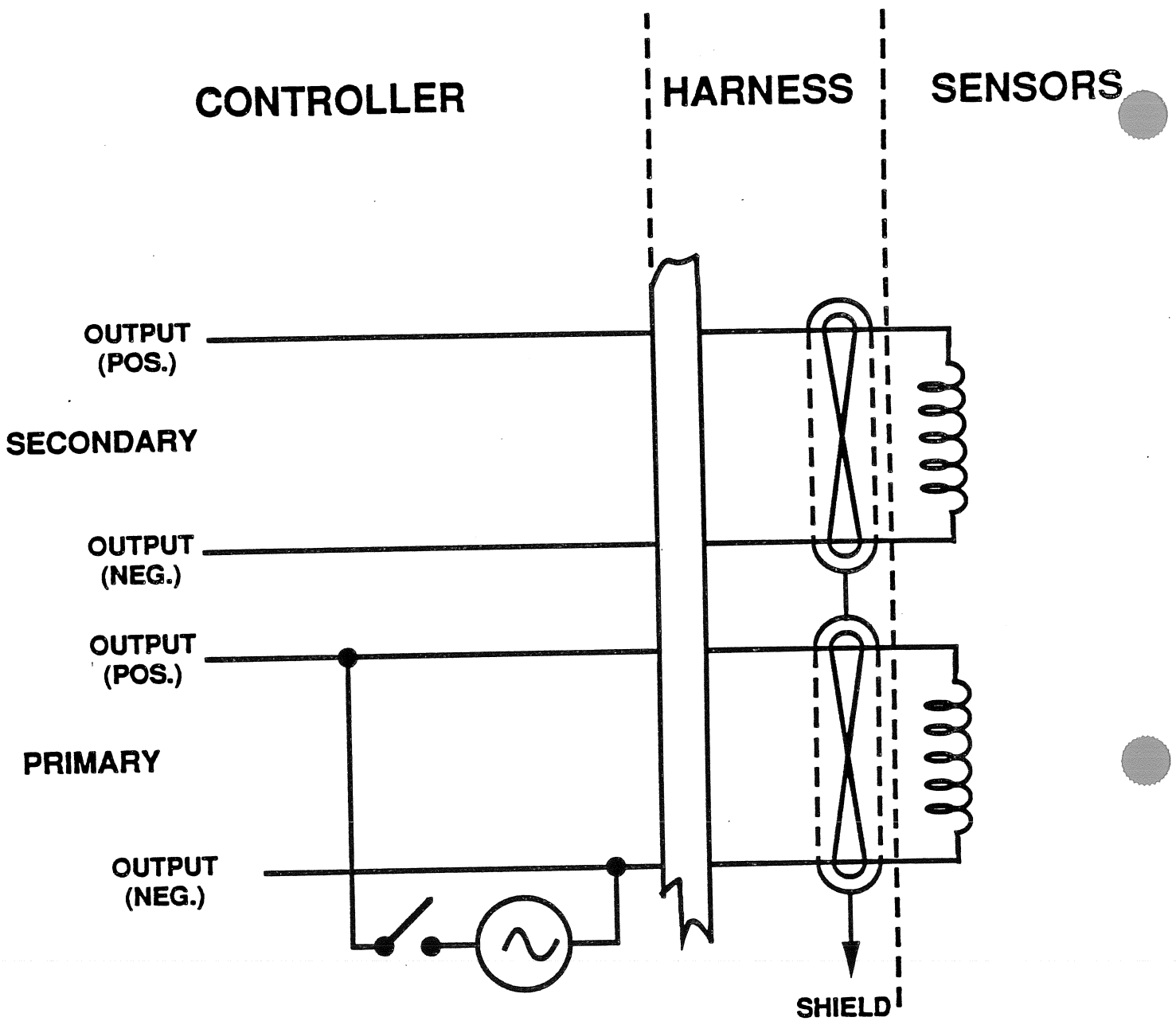


FIGURE 3-36



NOTE : POSITION OF SWITCH AND TEST SIGNAL GENERATOR CAN BE INTERCHANGED

DUAL FLOWRATE/SPEED SENSOR INTERFACE

FIGURE 3 -37

3.3.4.4.1 Speed Pulse Rate Counters (PRCs)

The Speed Pulse Rate Counters function very much like the flow counters on IE3. The basic block diagram is Figure 3-35. The differences between speed and flow are:

- o The speed period of measurement is 4-pulse periods instead of one.
- o The count frequency is 500 KHz instead of 666 KHz
- o The speed PRC's accuracy is:
  - ± 4.0 Hz from 60 Hz to 500 Hz
  - ± 1% of actual frequency from 500 to 3 KHz
- o The speed PRCs have first order lag filters with a break frequency of 1.4 KHz ± 350 Hz on their inputs.

3.3.4.4.1.1 PRC Test

The Speed PRC is tested just like the flow PRC. In sensors check one condition the 500 Hz supply is fed into primary winding of the speed sensor and the output is measured by the sensor secondary PRC.

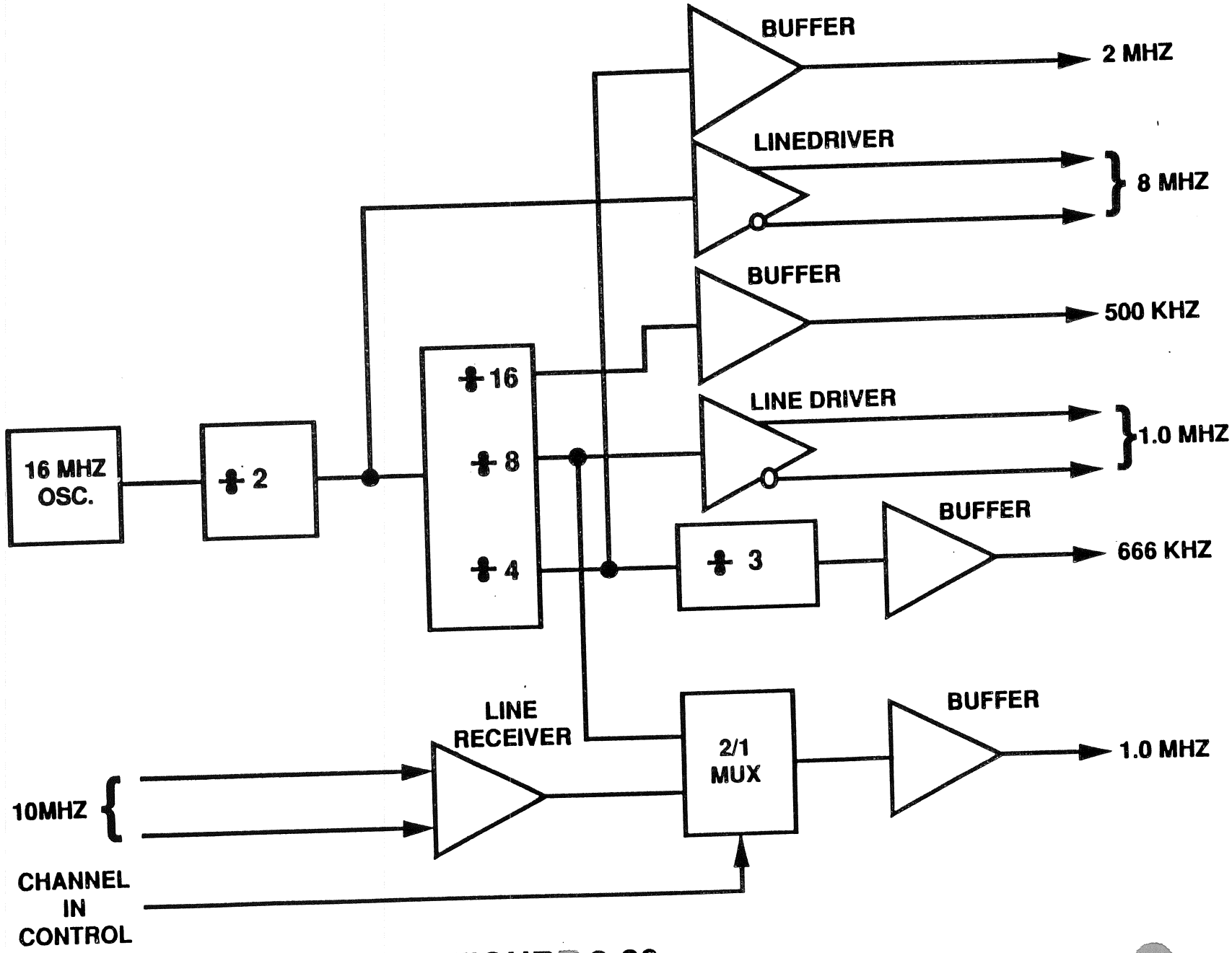
3.3.4.4.2 IE Clock Generator

The IE Clock Generator is designed to supply the clock to the in-channel and cross-channel sequence logic, the in-channel flow counters, and the in-channel speed counters. Figure 3-38 is a block diagram of the IE clock generator. The IE has its own independent 16 MHz oscillator which is divided down to 8 MHz, 2 MHz, 1 MHz, and 500 KHz. The 2 MHz is divided by 3 to yield the 666 KHz. The 500 KHz and 666 KHz are for use in the pulse rate counters. The 1 MHz is sent to a 2 to 1 mux input and to a line driver.

The line driver 1 MHz is sent to a line receiver on the cross-channel IE4. The line receiver on IE4 that goes to the 2 to 1 mux receives its signal from the cross-channel IE4. Whether the in-channel or the cross-channel 1 MHz drives the IE Sequence Logic depends on which IE4 is being looked at and the state of the channel A Watch Dog Timers.

If the Watch Dog Timers for channel A are enabled the IE1 MHz is derived from IE4-A for both channel A and B. If the IE-A Watch Dog Timer is timed-out, the 1 MHz from channel B drives both channels IE. The 8 MHz is sent to the CIE5 where it is used to clock out the vehicle recorder data.

IE CLOCK INTERTFACE



FIGUR 3-38

3.3.4.4.3 Pulse Rate Counter Interface Control

IE4 contains a portion of the PRC data sequence logic. Figure 3-39 is a block diagram of the IE4 portion of the sequencer. IEADD11 through IEADD31 are the IE address lines used to control the sequence along with PDTAENA0 from IE5. IEADD11 through IEADD31 select the PRC to be read and selects its data ready signal in the 8 to 1 select. The output of the 8 to 1 goes to IE5 to generate PDTAENA0 if the selected signal is true (asserted). PDTAENA0 being asserted initiates the selected PRCs output enable via a 3 to 8 decoder. The negation of PDTAENA0 enables a digital one shot that generates the reset to the selected PRC after it has been read.

3.3.4.4.4 IE In-Channel/Cross-Channel Data Mux

IE4 contains the logic for controlling the routing of data into the IEDPMs. Figure 3-40 is a block diagram of the IE in-channel and cross-channel data multiplexing. This multiplexer is responsible for directing the data from both A and B channels to the IE DPMs. The channel select signal is set up such that in channel A the in-channel data is loaded into even addresses while the cross-channel data is loaded in odd addresses and in channel B the in-channel data is loaded in odd addresses while the cross-channel data is in even addresses.

Data from the in-channel data latch not only goes to the one of two select it is also buffered and sent to the cross channel one of two select.

The transparent latch is used to stabilize data being loaded in the SCP IEDPMs. This was done to insure both DPMs contained the same data even while doing a write during power shut down.

3.3.4.5 Input Electronics No. 5 (IE5)

Input Electronics No. 5 is the heart and the brains of the SSMEC's Block II input electronics. IE5 controls the sequencing of data measurements and loading of data into the IE Dual Port Memory. Three types of data are loaded into the dual port memories and they are:

- o Analog to digital conversion (A/D) data
- o Pulse rate converter (PRC) data
- o Test words (TW) data

PRC DATA SEQUENCER INTERFACE

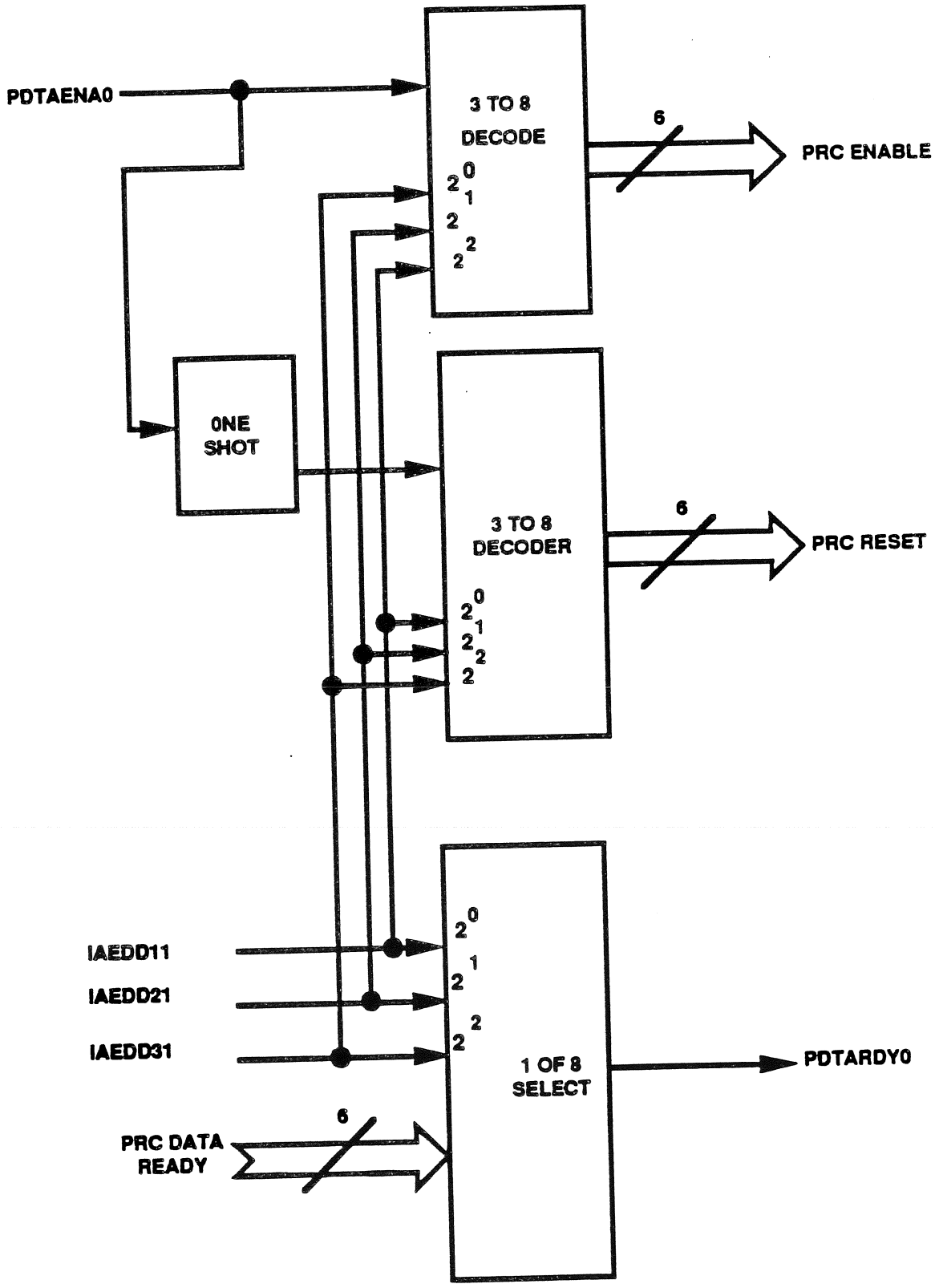


FIGURE 3-39

INCHANNEL / CROSS CHANNEL IE DATA MUX

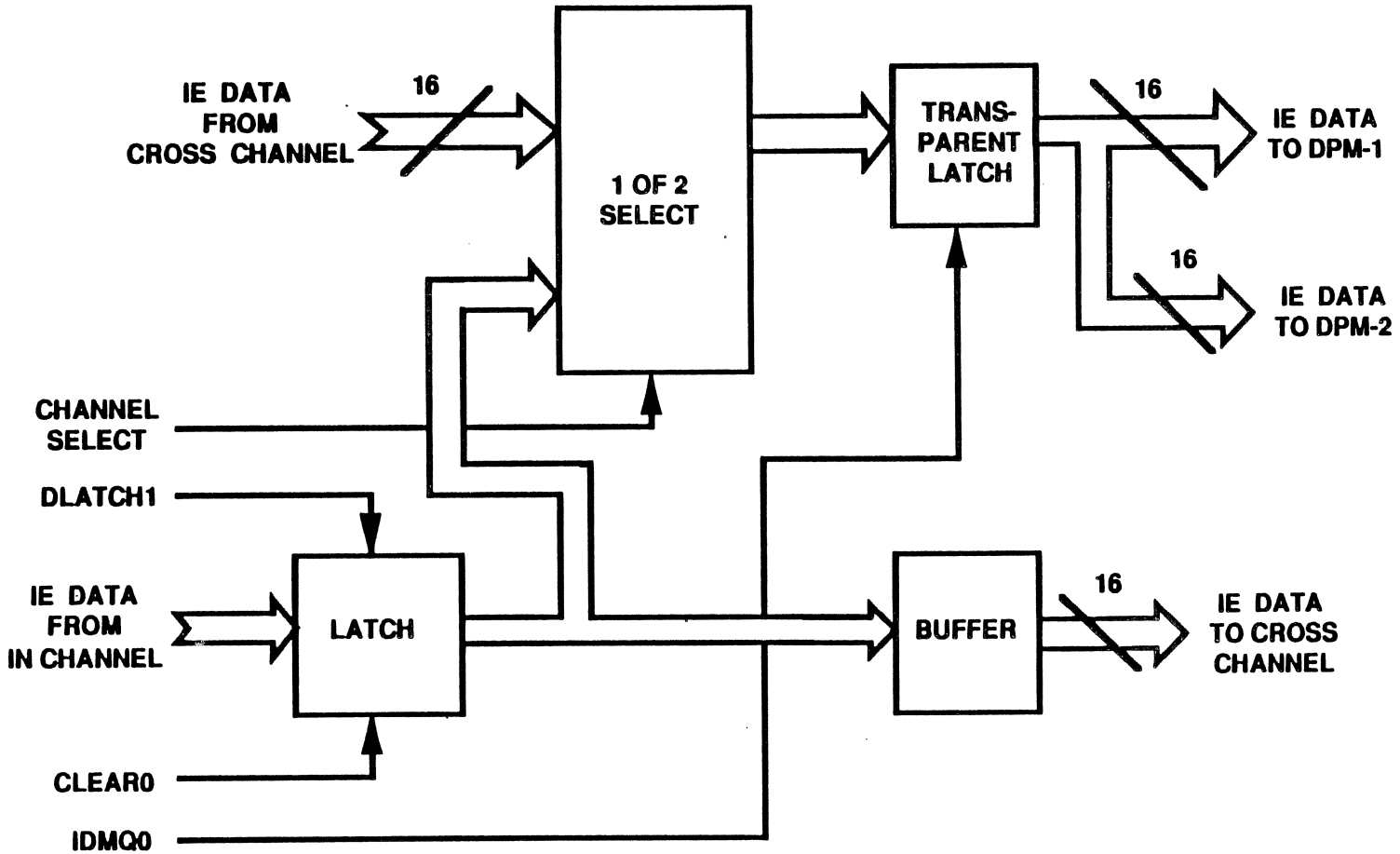


FIGURE 3-40

These three data types are all handled in 16 groups of 8 word(s) each per channel. The words in each group are alternately taken from channel A and channel B input measurement devices. Channel A being loaded into even addresses and channel B into odd addresses. Where A and B measurements are taken for the same function they are processed as pairs.

The function(s) contained on IE5 to do this task are:

- o Address Counter
- o Range Counter
- o Address Decoder
- o 50 Microsecond Timer
- o IE Function Control Signals
- o Dual Port Memory Interface

In addition to these functions IE5 also contains:

- o BIT Pulse Rate Converter (PRC)
- o Test Words
- o GSE Interface

The schematic for IE5 is 34069259 and the assembly drawing is 34069261.

3.3.4.5.1 IE Data Sequencer

Figure 3-41 is a block diagram of the entire data sequencer. All of the functions shown are not on IE5. The dual port memories are on CIE1 and CIE3 while the data latch, 1 of 2 select, transparent latch and cross channel buffer are on IE4. The IE Data Sequencer:

- o Receives IE DPM starting address and range from CIE
- o Receives start conversion signal from CIE
- o Decodes IE address and sets up IE data muxes
- o Supplies all control signals for 50 microseconds A/D conversion cycle and PRC control
- o Provides the handshake between the IE and the IE DPMs
- o Controls the flow of all IE in-channel and IE cross- channel data to the DPMs.

IE DATA SEQUENCER

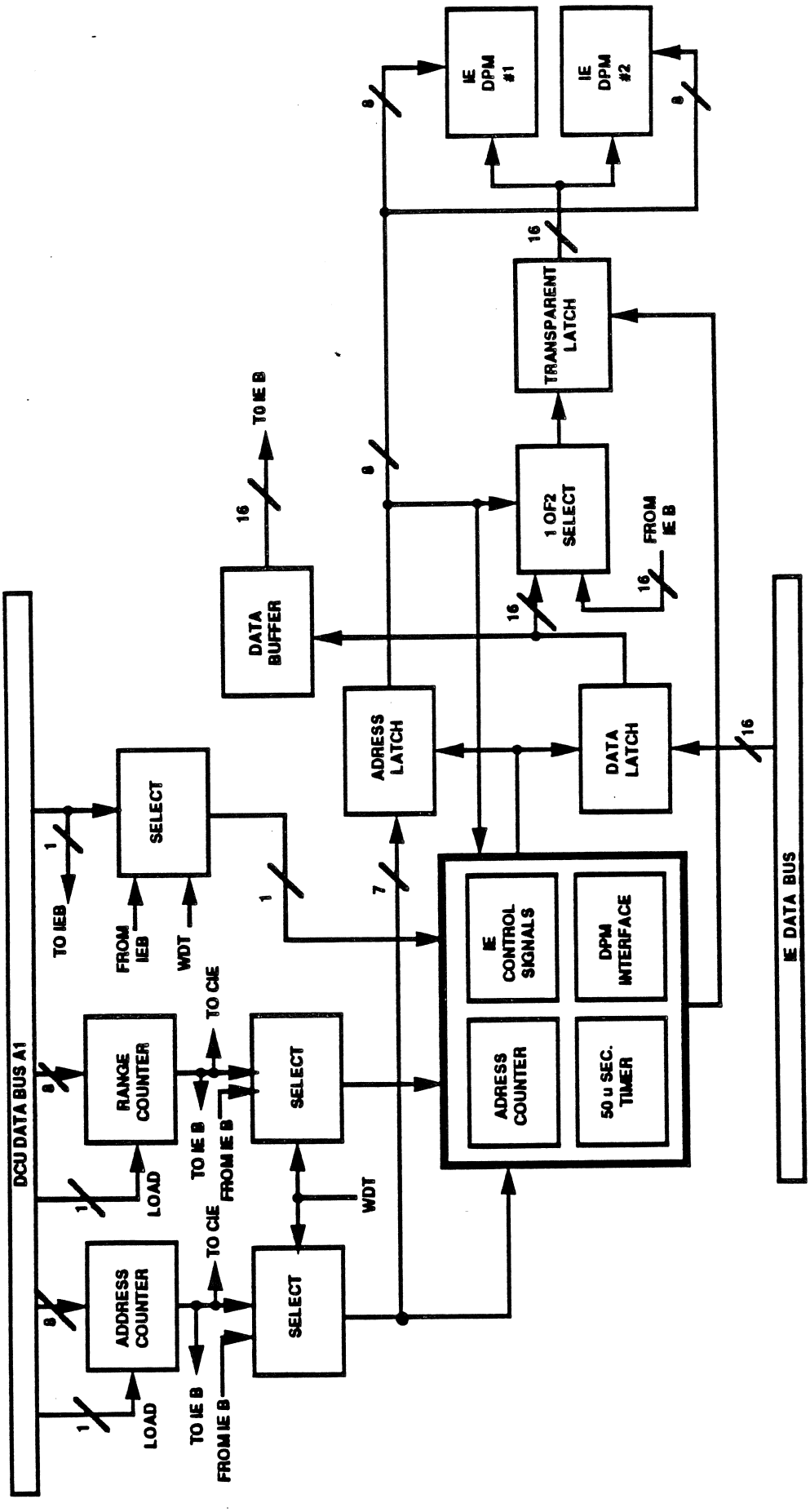


FIGURE 3-41

3.3.4.5.1.1 Address Counters

The IE Address Counter is loaded from the SCP's IEDATXX bus. The counter can be loaded with any address from 00_H to FF_H as a start address. Regardless of the start address loaded, the load will always start with an even address and load in both "A" and "B" words. For example start addresses FF_H will load FE_H and FF_H.

The output of the address counter is sent to two places. The places are the cross-channel one of two address select and the one of two in-channel address select. Which of the two sets of addresses is selected depends on the state of channel A's Watch Dog Timers (WDT) and whether the address counter is in channel A or channel B. As long as channel A's WDTs are not timed-out, the IE will use channel "A" address counter in both channel A and channel B. When either or both of A's WDTs time out, control of the IE switch to B and its address counter. A jumper to ground on the MIB at the channel B IE5 board location programs IE5-B's logic. The status of the IE address counter can be read by the processor from the CIE data muxes.

3.3.4.5.1.2 Range Counter

The Range Counter is a 7-bit counter that is loaded with the number of IE Function pairs to be processed. It is loaded by the LDIER0 signal with data contained on the bus defined by the IEDATOO1 to IEDATO61 signals.

The Range Counter is decremented every 50 microseconds. The 50-Microsecond Timer will stop 40.5 microseconds after the last cycle. This allows completion of the memory loading cycle. The Range Counter's content is equal to zero during the last cycle. The counter bus can be read by the processor from the CIE data muxes.

EOR0 is a stop signal generated after the last memory loading cycle or upon a memory load failure. It is sent to a 2 to 1 mux and to the other channel where it is muxed with XEOR0. CTRL0 selects the signal to use from the channel in control. The signal selected is ENDORNG0.

3.3.4.5.1.3 Address Decoder

The output of the 2 to 1 select mux discussed in the Address Counter goes to the address decoder. GPO1ENA1 to GP15ENA1 and TDECODE0 are the enable signals to each group in the IE. IEADD11 to IEADD31 are used to decode each pair of functions. Typically these signals are sent to 8 to 1 muxes along with the group enable signals. TDECODE0 is the first group decoded and is used to enable the Test Words.

The major difference exists between the types of functions in the IE. The A/D and TW functions are processed on a fixed-time basis. Data is processed and will be ready to be written to the DPMs at a specified time. In the case of the PRCs this is not true.

A PRC measures the period of an incoming signal. In the case of the Flow and Speed PRCs, the incoming signal will not be constant. Depending on the frequency of the signal, PRC data may or may not be ready to write to memory. Four possible situations exist when processing PRC data.

1. Channel A ready - Channel B ready
2. Channel A ready - Channel B not ready
3. Channel A not ready - Channel B ready
4. Channel A not ready - Channel B not ready

If the PRC data is not ready when it is addressed then the channel containing this data will be skipped. Both channels must be able to detect a not ready condition.

3.3.4.5.1.4 50-Microsecond Timer/Decoder

The 50-Microsecond Timer/Decoder is driven by a 1Mhz clock and generates the timing for the input electronics. This timer is started by command from the processor and continues to cycle in a 50-microsecond loop until a terminate signal is received. The terminate signal is caused by a processor command or the range counter counting down to zero. Every 50 microseconds a pair of input signals is processed. The 50-microsecond timers in both channels are clocked from the clock of the IE in control and started and stopped by the same signals from the IE in control. The 50-microsecond period is broken into 0.5 microsecond increments for use in deriving the IE control signals.

3.3.4.5.1.5 IE Function Control

The function control signals generated by the IE5 board are used to control processing of the 3 types of IE functions along with certain DPM and data functions.

The control signals are derived from the 50-Microsecond Timer/Decoder. These signals are used to generate the necessary function control signals used in the IE.

The A/D control signals consist of STCONV0, AZROENA0 and ADHOLD0 and IARST0. These signals are used to control processing of data associated with the Analog to Digital Converter.

The PRC and TW control signal is PDTAENA0/I3. This signal enables PRC and Test Word data onto the IE data bus.

The DPM and Data control signals consist of IDMRQ0, DLATCH1 and ADVCTR0. These signals control latching of address and data, requests to the DPMs, and clocking of the address and range counters.

3.3.4.5.1.6 DPM Interface

The DPM interface circuits are responsible for loading the data into the correct memory locations. The DPM interface determines the status of the A and B Ready signals and controls the LSB accordingly. It also sends the requests and receives the acknowledges to and from the DPMs.

ARDY1 and BRDY1 are the Ready signals from channel A and channel B. The state of the LSB, denoted ADRO1, is determined by the status of the Ready signals. ABSEL0 is a control signal that routes channel A data to memory when the LSB is a logic 0 and channel B data to memory when the LSB is a logic 1. REQUEST0 and IEDACK0/Z3 are Request and Acknowledge signals to and from the DPM's respectively.

Another Test Word is present in group 11. This Test Word is in a group of PRCs. It is a hardwired 11-00 pattern identical in both channels. Since it is in a group of PRCs, it is treated as a PRC and processed as such. Unlike a PRC, the Test Word data will always be ready.

3.3.4.5.3 Built In Test (BIT) Pulse Rate Counter (PRC)

The BIT PRC measures the period of the 2 KHz RVDT/LVDT excitation frequency. A counter is enabled for one period of the incoming 2 KHz frequency. The resulting counter output is the digital data tristated onto the IE data bus and eventually loaded into memory.

DMODX1 is the 2 KHz input to the PRC. IE2MHZ1 is the 2 MHz control logic and gated clock frequency. RDYTRC-1/13-- is a signal that is true when the data is ready. ENATRC-0 is a signal that enables the data onto the bus defined by IEDTA001 to IEDTA151. After data has been read, the RSTTRC-0/13-- signal will reset the BIT PRC to allow it to continue updating. 5PRC0FL0 is a signal used during the toggle-overflow test. This signal allows the counter to overflow and tests the toggle bit. The toggle bit is bit 15 of the PRC output. It is toggled each time the PRC updates.

The block diagram for the BIT PRC is the same as shown for speed and flow in Figure 3-35 in section 3.3.4.3.

3.3.4.5.4 Ground Support Equipment (GSE) Interface

The GSE Interface on IE5 consists of twelve differential line receivers that take twelve control signals from the ground support equipment and convert them to logic level signal. These signals are not part of the normal input electronics.

3.3.4.6 Input Electronics No. 6 (IE6)

Input Electronics Assembly No. 6 is called the Vibration Signal Processor Electronics (VSPE) assembly. This assembly is unique in that it is composed of six identical hybrid circuits and their supporting resistors and capacitors. The schematic for this assembly is 34069265 and the assembly drawing is 34069267.

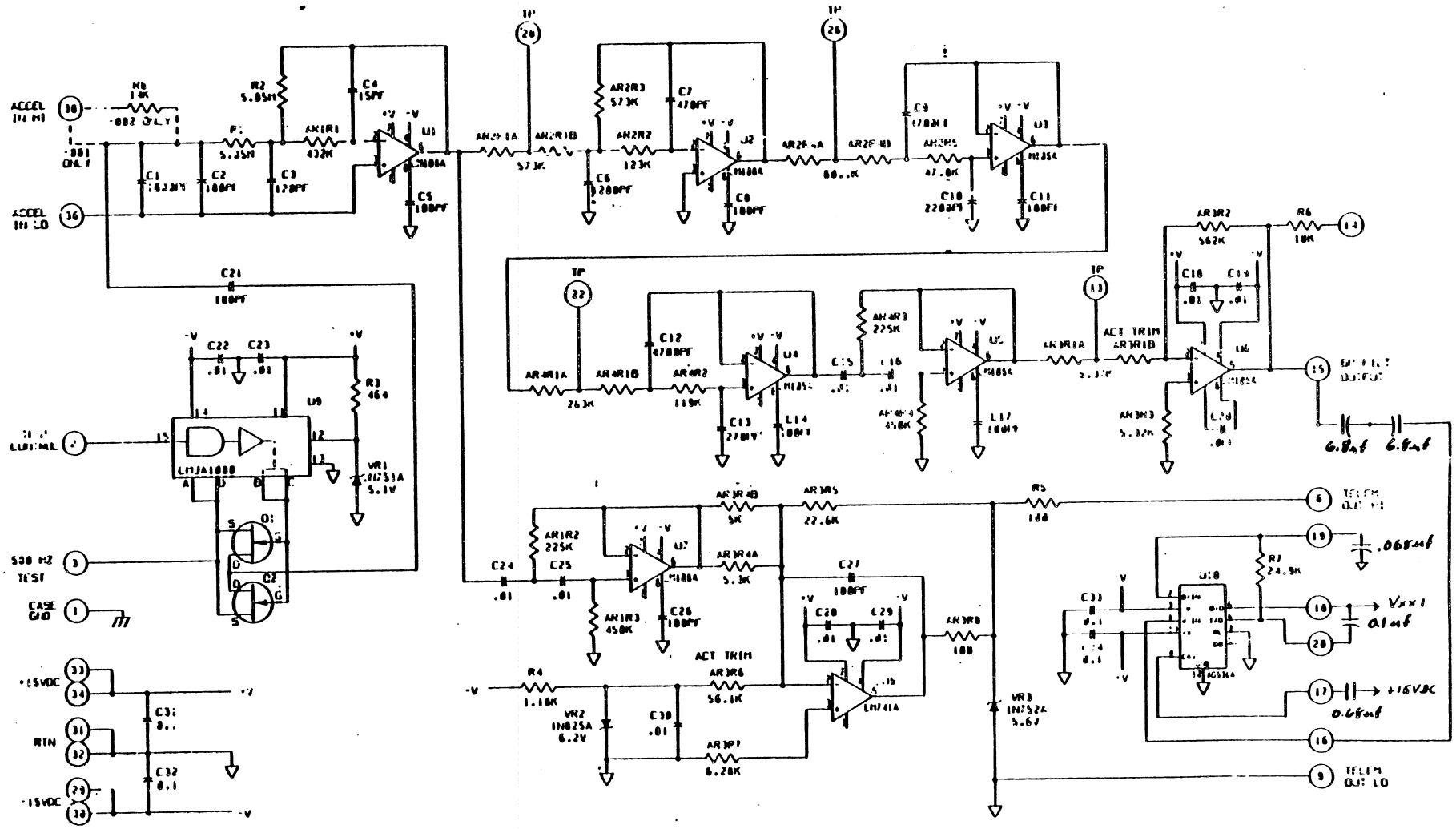
Figure 3-42 is a schematic diagram of the VSPE hybrid. All six hybrids on IE6 are exactly the same. The input from the engine sensor comes in on Pin 38 and 36. The signal is then filtered and amplified. U1 is a 2500Hz low pass filter and its output is split and sent to U7 and U2. U7 is a 50Hz high pass filter that, in turn, feeds an amplifier U8 that is biased about 2.5 Vdc and has its output limiter set at the +6.5V, -1V. The output of this part of the circuit is the telemetry output. The path taken by the output of U1 goes to a three-stage 800Hz low pass filter composed of U2, U3, and U4. The output of U4 is in turn set to U5, a 50 Hz high pass filter, and from there to an amplifier U6. The output of U6 is fed back into U10 which is an RMS to DC converter. The resulting DC output from U10 is sent to IE3 for input to the A/D converter.

Input pin 3 is the 500Hz test signal input from IE3 that can be switched into the input line to U1. The enabling of this test signal is controller by the Sensors Check One signal on pin 2. The 500Hz checks both the amplifier and the engine sensor.

How the vibration sensors are connected in the system is shown in Figure 3-43.

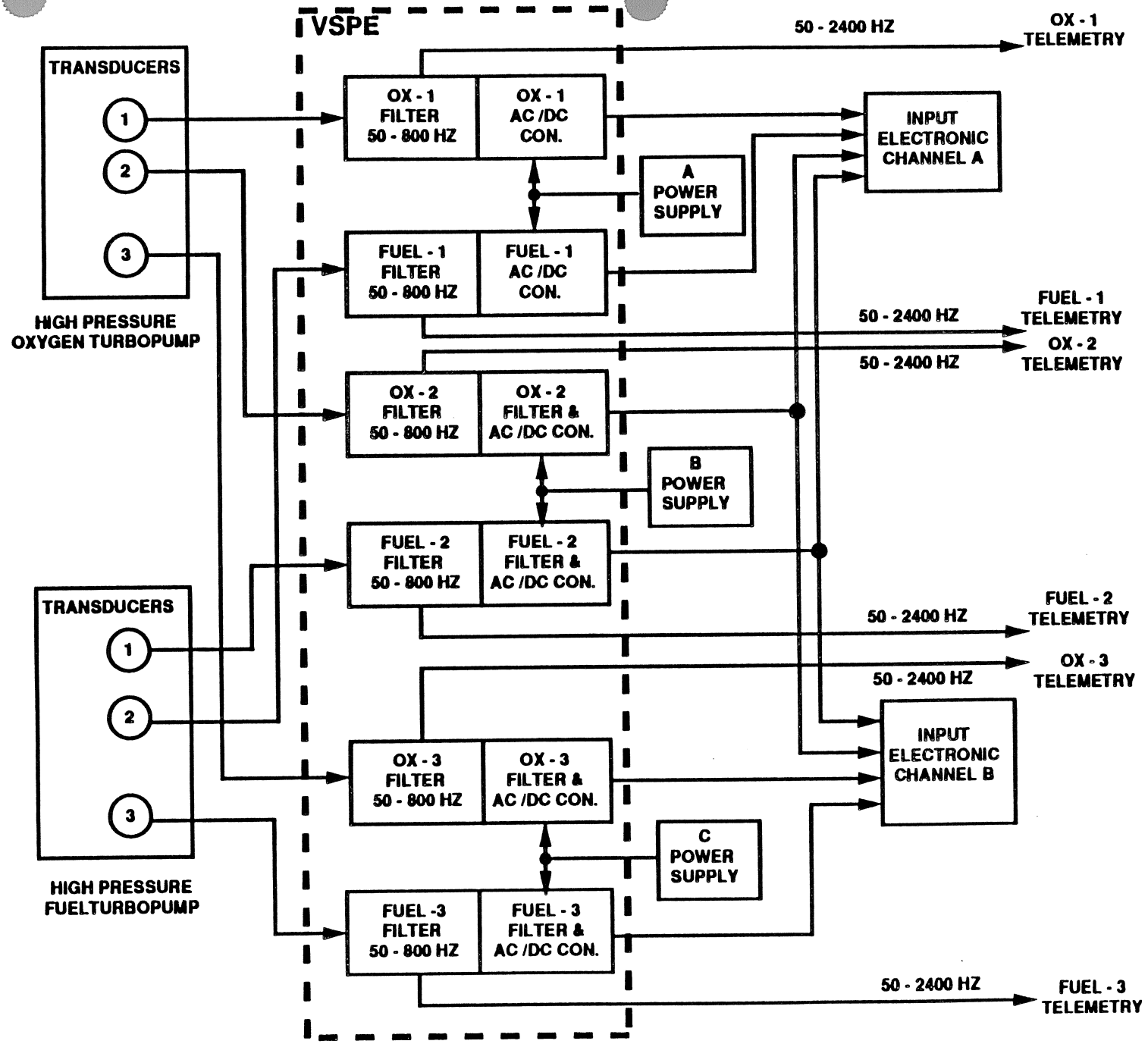
3.3.5 Output Electronics

The output electronics is that part of the SSME controller that actual controls what happens on the main engine. The output electronics sends control signals to the engine servo valve, servo switches, solenoids, and igniters. The OE also receives signals back from these devices which it converts to either digital bits or analog B.I.T. data.



VSPE HYBRID

FIGURE 3 -42



VIBRATION SIGNAL PROCESSING BLOCK DIAGRAM

FIGURE 3 - 43

The O.E. is designed such that it can receive commands from either channel A or channel B CIE, depending on the state of the watch dog timers. Channel A will control the output electronics as long as neither channel "A" watch dog timer is timed out. Channel "B" can control the output as long as either "A" watch dog timer is timed out and neither B watch dog timer is timed out. If at least one watch dog timer in each channel is timed out, the output electronics power safety switch will turn the power to the engine off so that neither output electronics can control the output.

The output electronics is composed of seven printed wiring assemblies. The seven assemblies are made up of 6 types, one of which, OE4/5, is used twice.

3.3.5.1 Output Electronics No. 1 (OE1)

Output Electronics No. 1 is the central control for the output electronics. OE1's schematic is 34069295 and its assembly drawing is 34069297. OE1 contains:

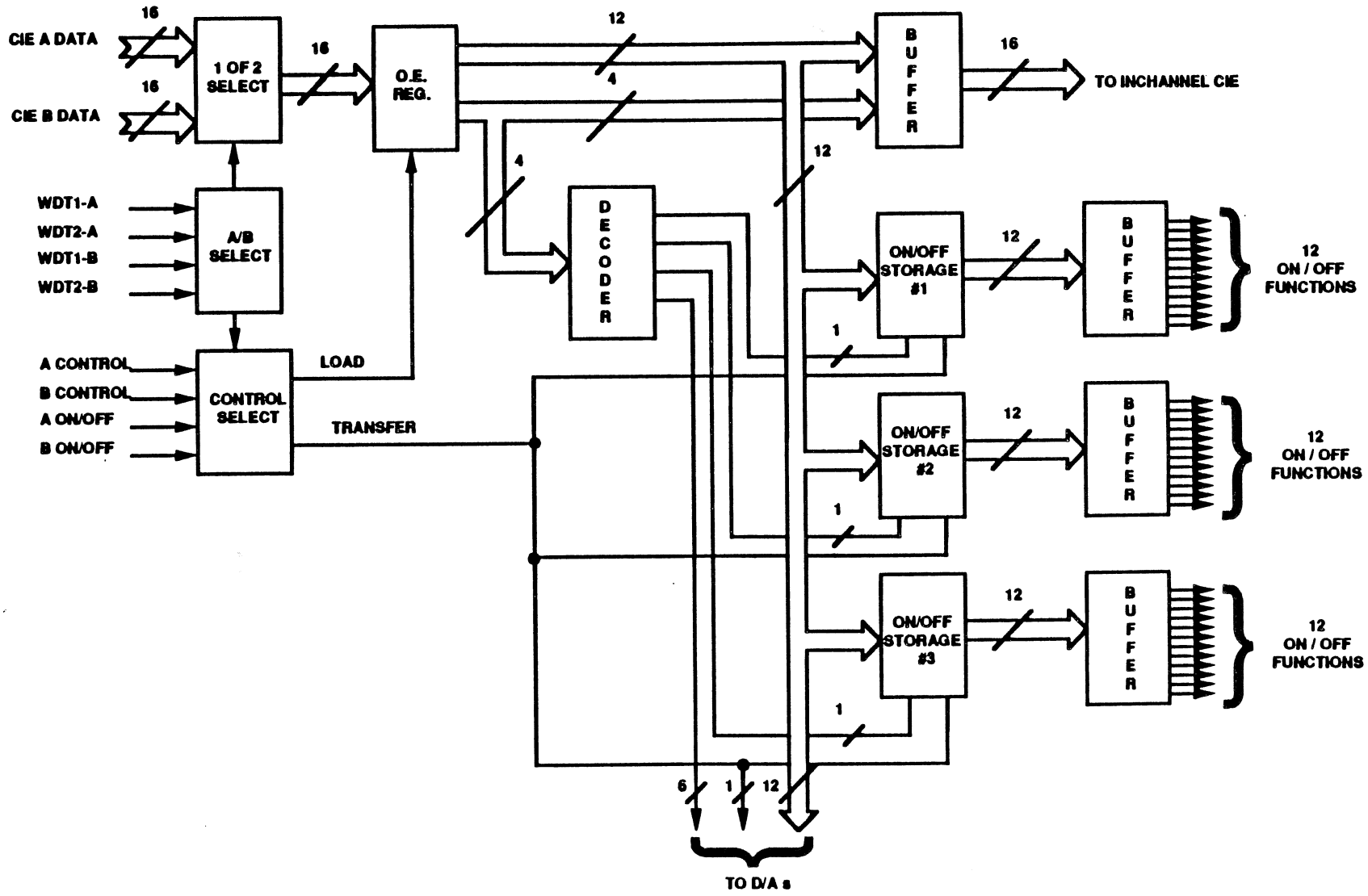
- o 1 of 2 Input Data Select MUX
- o A/B Select Logic
- o 16-bit OE Register
- o 3 - 12 bit ON/OFF Register and buffers
- o 6 - 12 bit D/A Converters
- o OE Address Decode Logic
- o RVDT excitation frequency source select
- o Output Electronics Voltage Monitor and Power Latch
- o 4 GSE Data Buffer
- o +28V Power Off Indicator

3.3.5.1.1 1 of 2 Input Data Select

Figure 3-44 is a block diagram of the 1 of 2 select, the input register and the ON/OFF registers. The 1 or 2 select receives a 16-bit data word from CIE-A and a 16-bit data word from CIE-B and it selects which word is to be transferred to the data register based on the state of WDT1-A, WDT2-A, WDT1-B and WDT2-B. CIE-A's data is transferred when WDT1-A and WDT2-A are not timed-out. If either WDT1-A or WDT2-A is timed-out, CIE-B's data will be transferred.

3.3.5.1.2 A/B Select

The A/B select of Figure 3-44 the selector will select the "A" data, "A" load command and the "A" transfer command as long as both "A" WDTs are not timed out. When either of A's WDTs time out, control and data shift to B.



BLOCK DIAGRAM OF O.E. ON/OFF REGISTER

FIGURE 3 - 44

3.3.5.1.3 OE Register

The OE Register is a 16-bit register that holds the OE command prior to it being transferred to ON/OFF registers or D/A converters. The register is loaded with the CIE in control's data by a load command from the CIE in control. The four least siginificant bits of the register are sent to a 1 of 16 decoder and to a buffer which is connected to the CIE input data mux. The twelve most significant bits of the register go to a buffer which is fed back to the CIE input data mux, to the three twelve-bit ON/OFF registers and to the six twelve-bit digital to analog converters.

3.3.5.1.4 Decoder

The OE Decoder takes the four least significant bits of the OE Register and decodes them into 16 control signals. The HEX decodes are:

HEX	Function
0	N/A
1	Solenoid Energize Test
2	Spare
3	Negative Command Actuator Test
4	Positive Command Actuator Test
5	On/off Register 3
6	On/off Register 2
7	On/off Register 1
8	N/A
9	D/A 6 (SPARE)
A	D/A 5 (OPOV)
B	D/A 4 (FPOV)
C	D/A 3 (CCV)
D	D/A 2 (MCV)
E	D/A 1 (MFV)
F	N/A

3.3.5.1.5 Buffers

The buffers take the output of the 36 bits in the three ON/OFF registers and send them out as 40 buffered signals. Five of these signals are open collector for cross channel signals.

3.3.5.1.6 Control Select

The control Select Logic uses the A/B select signals to determine which channels command and control signals will run the output electronics. The control will always be from the channel whose data is being used.

3.3.5.1.7 Voltage Monitor and Power Up Latch

Figure 3-45 is a block diagram of the OE voltage monitor and power up latch. The OE voltage monitor is a comparator that monitors the OE +5, +15 and -15 volts for undervoltage conditions. As long as all voltage remain good, the output of the monitor will be low. This low turns on Q5 which in turn turns on Q4 and Q3. Q3 turns on the power safety switch which enables the OE to control the valves, switches, solenoids and igniters, as long as the power up latch is on (open collector output HI). The safety switch can be turned off by:

- o Safety Switch Off command true,
- o Either Watch Dog Timer timing out,
- o Any of the three voltages going below limits,
- o Setting the undervoltage test circuit.

To turn the safety switch on you must:

- o Make the Safety Switch Off command false,
- o Have neither WDT timed out,
- o Reset the Undervoltage Test,
- o Make the Safety Switch On command true.

3.3.5.1.8 RVDT Excitation Frequency Source Select

The RVDT excitation frequency source select is a dual 1 of 4 mux controlled by the 2kHz ON/OFF signals from channel "A" and channel "B". The mux selects the frequency source for the RVDT excitation generator in accordance with the following table.

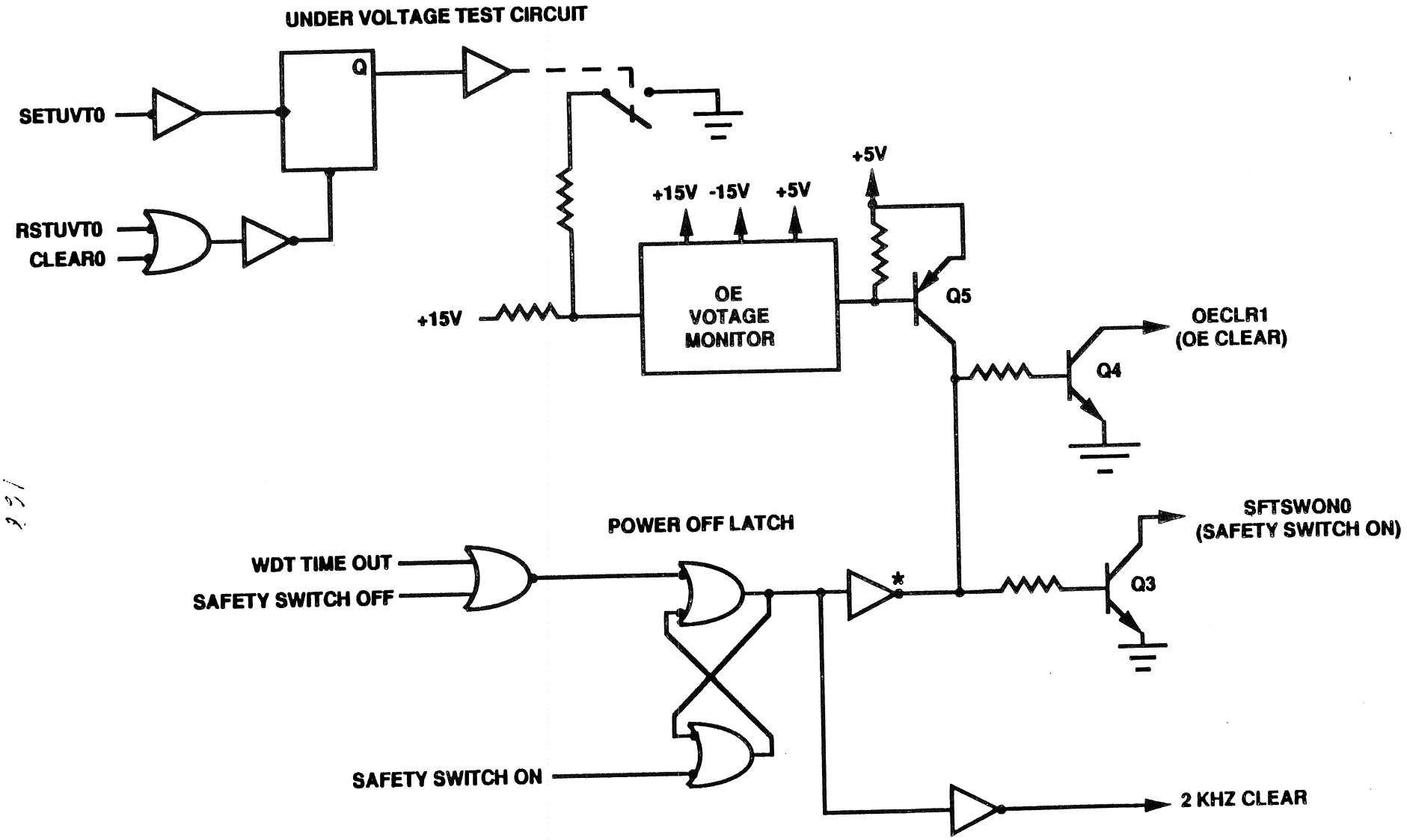
Input Cont		2kHz	128kHz	RVDT Excitation	
A	B	Source	Source	Ch A	Ch B
1	1	0	0	Off	Off
0	1	A	A	A	A
1	0	B	B	B	B
0	0	B	B	Off	B

The 2kHz ON/OFF signals also control which RVDT generator is enabled in accordance with the table.

3.3.5.1.9 Digital to Analog Converter (D/A)

OE1 contains six digital to analog converters which are the inputs to the six servo drivers. The 6 D/As are 12-bit converters with a 0 to 10V output. The value of the output voltage is dependent on the weighted value of the binary number loaded into the A/D register. Each A/D can be selectively loaded with the 12 MSBs of the OE register in accordance with the selection made by the 4 LSBs of the OE register (3.3.5.1.4).

VOTAGE MONITOR / POWER LATCH



* OPEN COLLECTOR

FIGURE 3-45

3.3.5.1.10 GSE Data Buffer

The GSE Data Buffer is simply a quad input digital differential line driver.

3.3.5.1.11 Power Off Indicator

The Power Off Indicator's function is to provide a means to determine if the +28VDC to the control or the +5V to the memory and processor have gone below limits while the 3-phase 115VAC 400Hz is off. Figure 3-46 is a block diagram of the Power Off Indicator. The Power Off Indicator is powered by a 5-volt regulator that is in turn powered by +15V derived from the +28VDC input power. The circuit is designed such that any time the +28VDC is truned on the Monitor Power On Clamp and the Monitor +5V undervoltage detector will cause 280K1 to be low indicating +28VDC has been off. The 280K1 can only be made high by a command from the processor when the Mon1528 +15VDC, the processor +5VDC, the memory +5VDC and the Mon 5VDC are at or above limits.

The 280K1 signal can be set low by applying +28VDC to the controller, any of the monitored voltages going low (+5V Mon, memory and processor and +15VDC Mon1528) and the Power Off Indicator Reset (POIRST) from the processor.

3.3.5.2 Output Electronics No. 2 and No. 7 (OE2 and OE7)

Output Electronics No. 2 contains six fail safe servo switch drivers and monitors, 6 solenoid drivers and monitors and the solenoid pull/hold voltage switch. The schematic for this assembly is 34069304 and the assembly drawing is 34069306.

Output Electronics No. 7 contains six fail operate servo switch drivers and monitors and seven solenoid drivers and monitors. The schematic for OE7 is 34069307 and the assembly is 34069309.

3.3.5.2.2 Solenoid Driver and Monitor

All of the solenoid drivers and monitors are the same. Figure 3-48 is a schematic of the Solenoid Driver and Monitor. This circuit also uses a MOSFET as a switch element. The input voltage is the SOLDRV which is either +29V/+24V or the +16V/8V. The circuit contains a current limiter. This limiter will prevent the switch current from exceeding 1 amp in case of a short-circuited load. It will not normally limit in the Hold mode due to the low hold voltage (+16V in A and +8V in B). In this mode the switch is saturated. The limiter and the 4N49 optical coupler are isolated from ground in order to prevent load inductance switching transients from affecting their operation. The optical coupler is used to control the gate to source voltage for turn ON/OFF. The emergency shutdown driver has a diode in series with its output to provide isolation to an additional external driver.

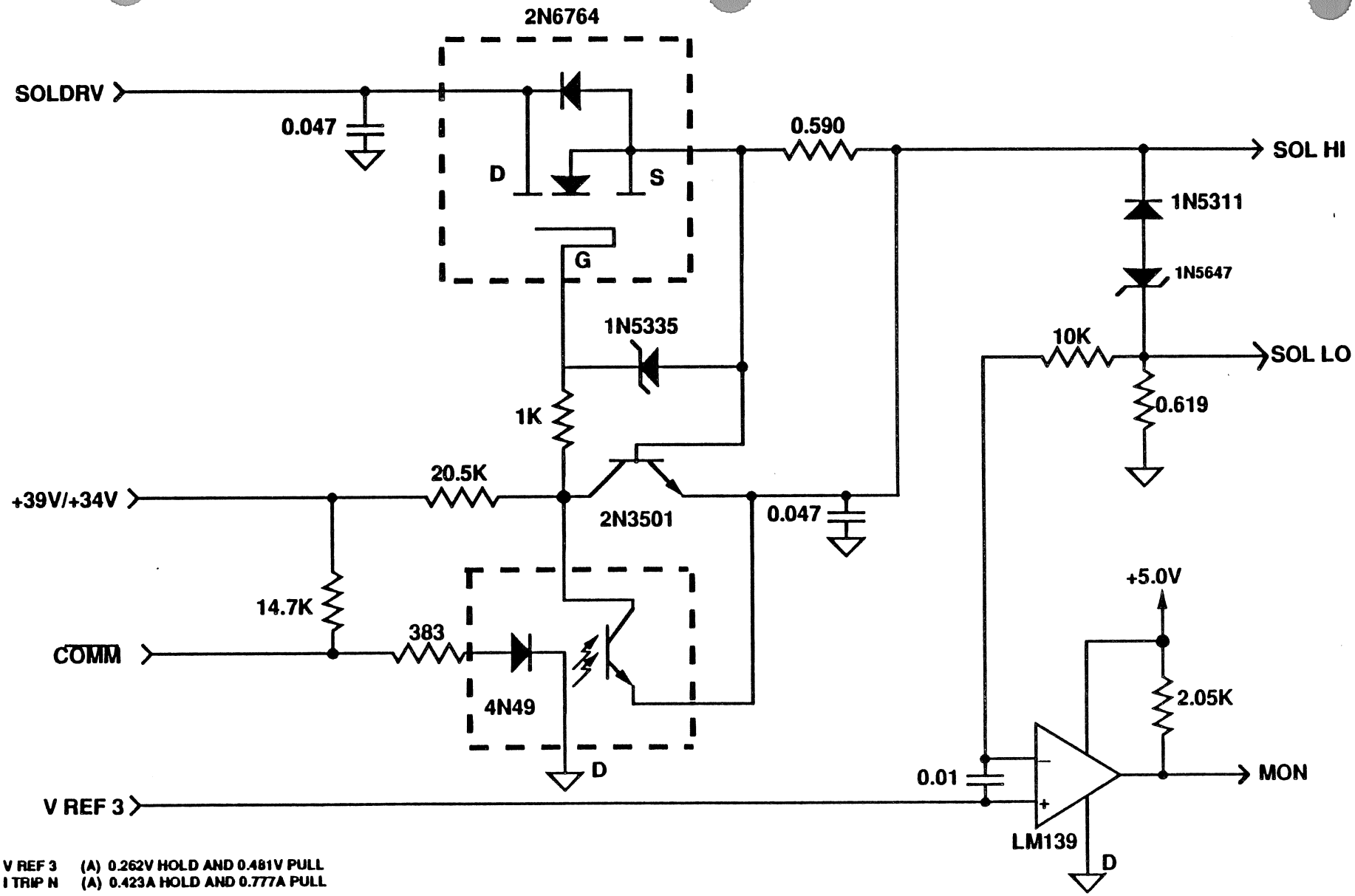
The diode network across the load provides fast solenoid drop-out by placing the zener in the current discharge path. This clamps the solenoid inductance reverse voltage at a high but safe level (45V max.) and minimizes the time required to reduce the solenoid current to its drop-out level.

The current monitor compares the IR drop across the .619 ohm sensing resistor to VRef. When the IR drop exceeds the reference level the monitor output will switch to a logic low level.

3.3.5.2.3 Servo Switch Driver and Monitor

The Servo Switch Driver and Monitor is the same for both the fail operate and the fail safe servos. Figure 3-49 is a schematic of the servo driver and monitor.

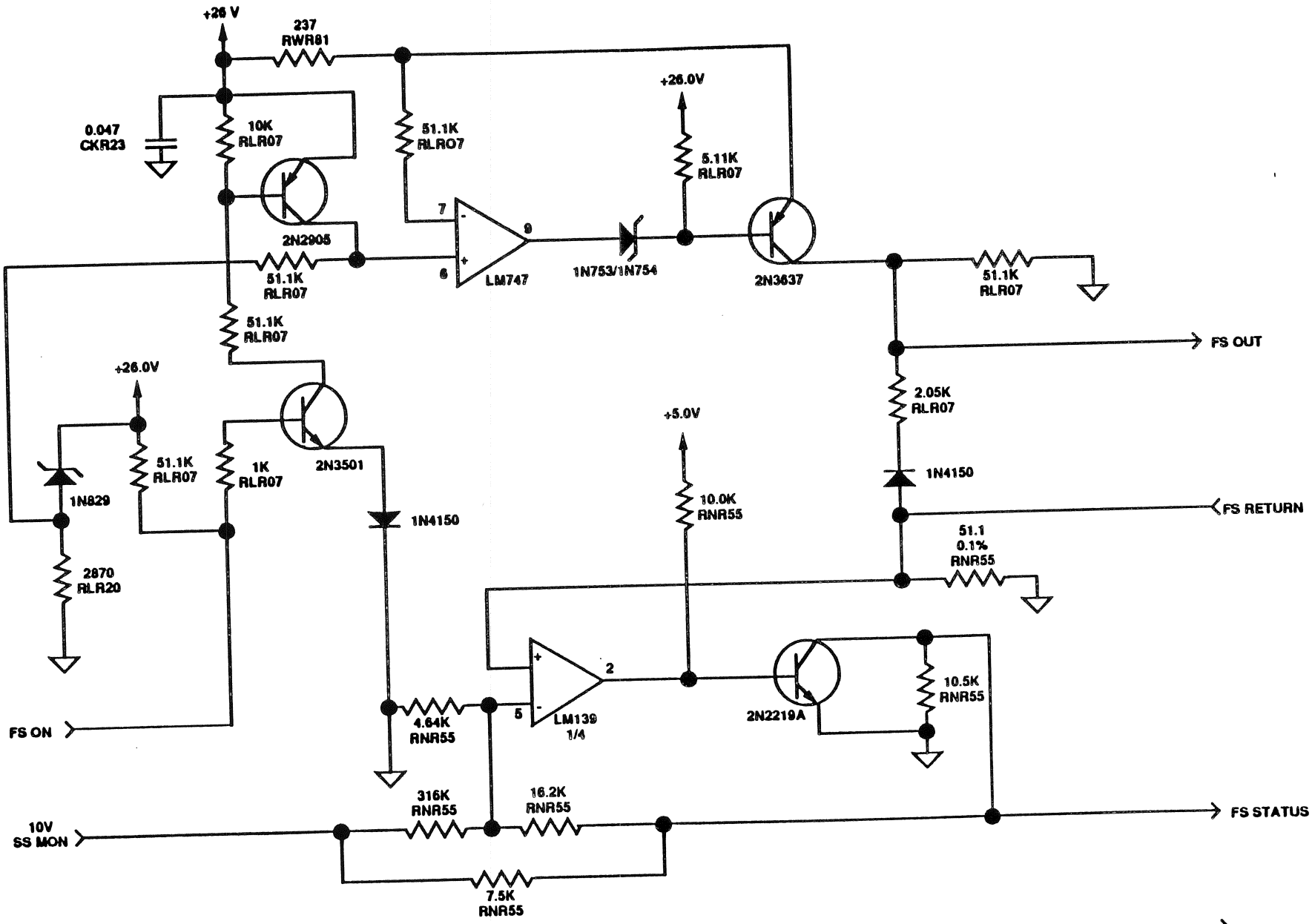
The circuit is an active current regulator located in series with the +26 voltage supply and Servo Switch. The regulated level is set by a reference voltage (+19.8V). This is -6.2 volt with respect to the +26V and is the input signal level to the amplifier. At null both the inverting and non-inverting amplifier inputs are equal and therefore there is 6.2-volt across the 237-ohm resistor and the controlled current is .026 amps. The circuit is turned on and off by command. The monitor portion of the circuit monitors current by using the voltage drop across the 51.1-ohm resistor. The circuit contains hysteresis that cycles the trip point between the Servo Switch minimum energization and maximum dropout level.



- V REF 3 (A) 0.262V HOLD AND 0.481V PULL
- I TRIP N (A) 0.423A HOLD AND 0.777A PULL
- V REF 3 (B) 0.167V HOLD AND 0.481V PULL
- I TRIP (B) 0.270A HOLD AND 0.777A PULL

SOLENOID DRIVER AND MONITOR

FIGURE 3 - 48



SERVOSWITCH DRIVER AND MONITOR

FIGURE 3 - 49

3.3.5.3 Output Electronics No. 3 (OE3)

Output Electronics No. 3 contains 8 demodulators for RVDT/LVDT feedback signals and a voltage reference source for the Output Electronics. The OE3 schematic is 34069292 and the assembly is 34069294.

3.3.5.3.1 Demodulator Circuit

Figure 3-50 is the block diagram of a typical RVDT/LVDT Demodulator. Seven of the demodulators are identical. One, the POGO-RIV, is different in that some of the resistors and capacitor values have been changed to obtain a different gain and filter frequency. The input signal is fed differentially into the first amplifier which is an impedence matching amplifier. The second amplifier is an inverter with unity gain that is used in conjunction with the analog switch to full wave rectify the input sine wave. The third amplifier is the filter amplifier that smooths the signal into a DC level.

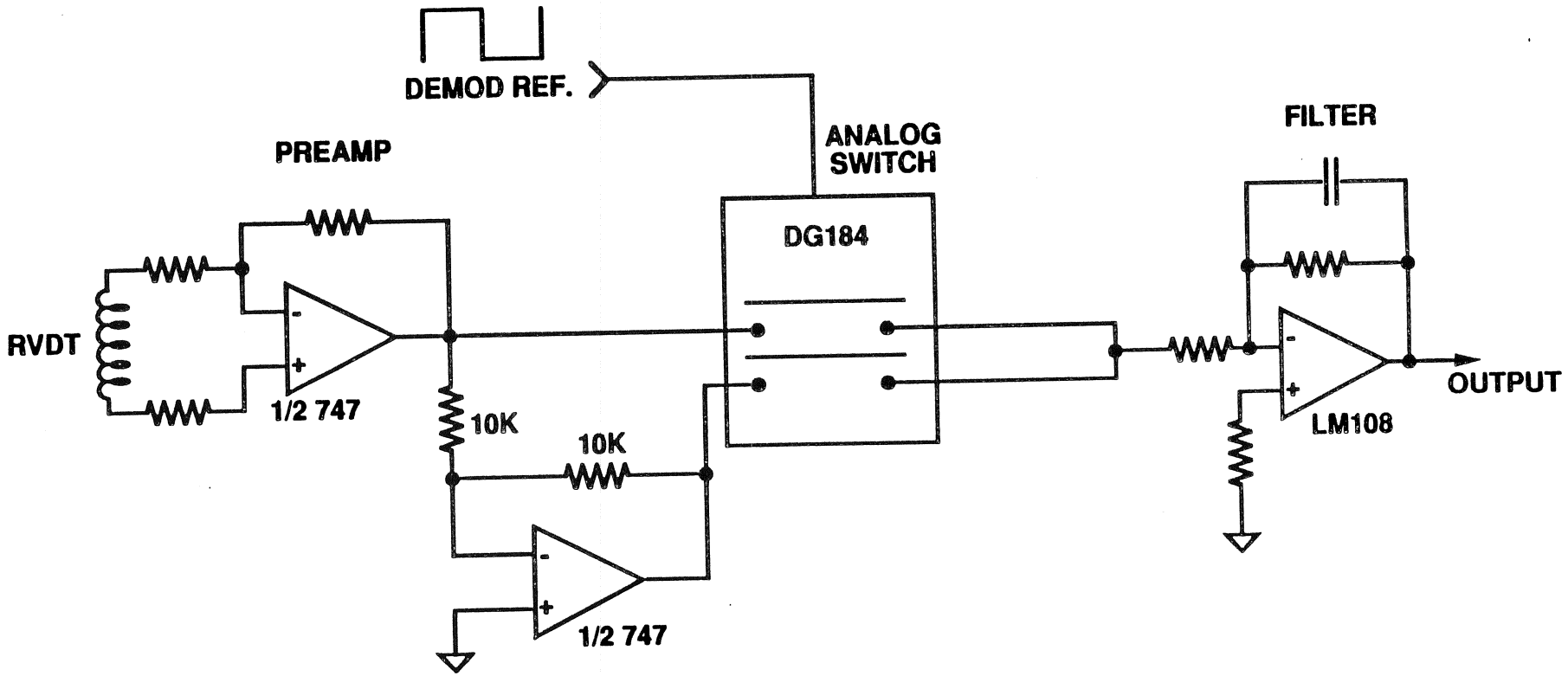
3.3.5.3.2 Reference Voltage Source

The Reference Voltage Source supplies reference voltages for both the IE and the OE. Figure 3-51 is a schematic of the Reference Voltage Source.

These voltages are obtained from a temperature compensated zener 1N829-1 utilized in a constant current amplifier configuration with an emitter follower start. This circuit also supplies the reference for the hold and/or pull voltages. When the circuit is used in B channel the three pin programming lines are connected together. When the circuit is used in A channel, the above lines are not connected. A logic signal switches the reference voltage from hold to pull test using the DG184 analog gate switch.

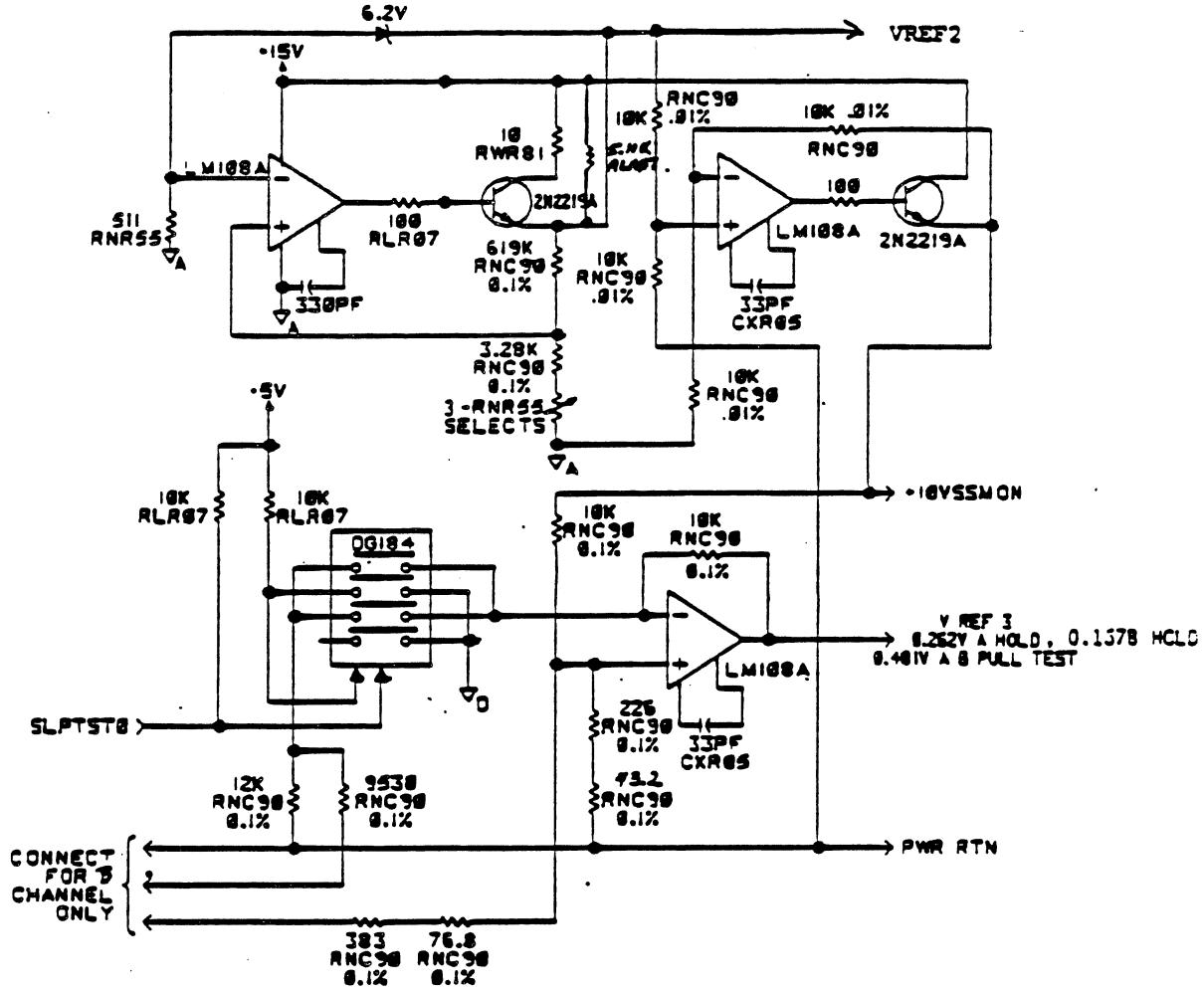
The voltages derived by the reference voltage source are:

MNemonic	Voltage	Application
VREF2	+10 VDC	Used as Precision reference in IE and OE
+10VSS MON	-10 VDC	Servo Switch Monitor Reference
VREF3	+0.481 VDC	Solenoid Monitor Pull Reference
VREF3	+0.262/ 0.167 VDC	Solenoid Monitor Hold Reference



2K Hz CARRIER SYNCHRONOUS-DEMODULATION

FIGURE 3-50



DECOUPLING NOT SHOWN FOR SIMPLICITY

VOLTAGE REFERENCE SOURCE

FIGURE 3-51

3.3.5.3.3 GSE Buffers

OE3 contains 41 differential line drivers used to send various controller logic level signals to the Ground Support Equipment (GSE).

3.3.5.4 Output Electronics No. 4/5

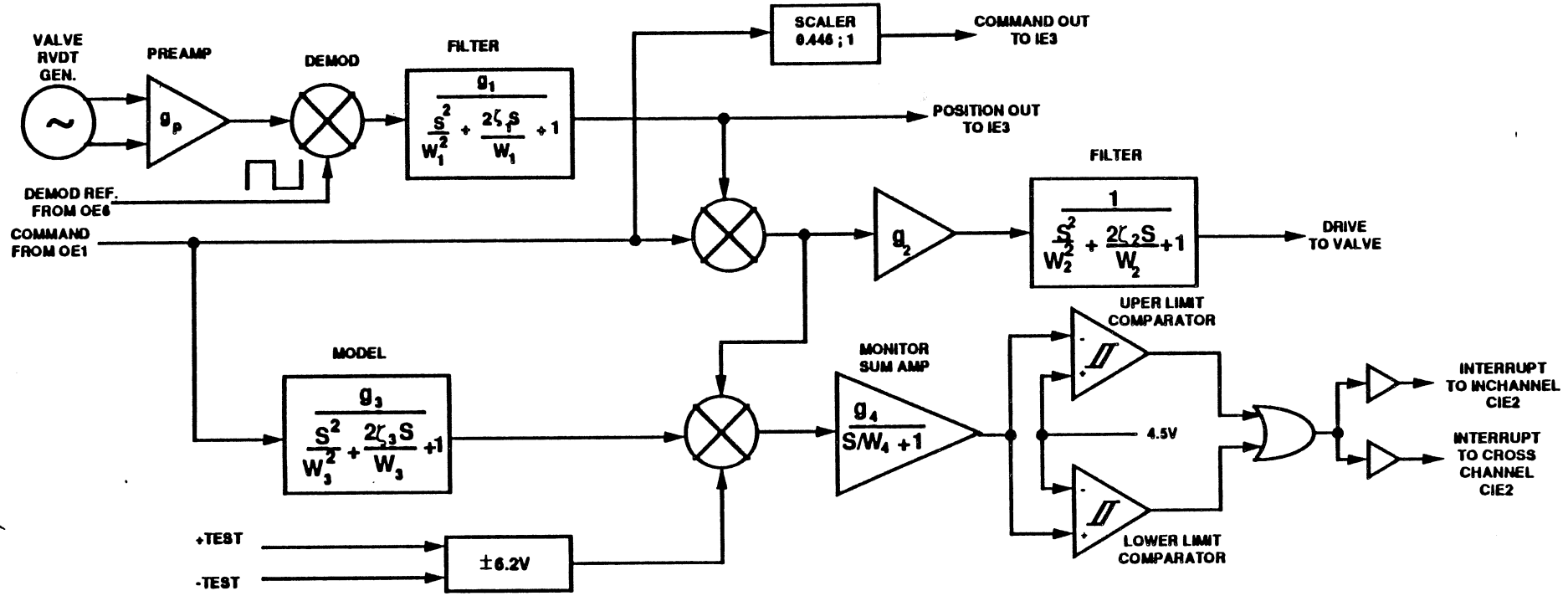
Output Electronics No. 4/5 is an electronics assembly that contains three servo actuator drivers and is used in two different assembly locations in each channel. The OE4/5's function is to:

- Provide closed loop actuator positioning in response to position command inputs from OE1 (D/A outputs).
- Provide monitoring of actuator response to command input.
- Provide RVDT position information to input electronics for A/D conversion.
- Provide a model of the valve.
- Compare valve position feedback to model generated position feedback and provide an alarm when preset differences are exceeded.
- Provide for self-test of comparators during pre-flight.

Each of the three drivers is composed of:

- A Summing Power Amp with filter
- RVDT preamp
- RVDT demod and filter
- Valve model
- Monitor Sum Amp
- Limits comparator
- Command feedback scaler

The schematic for OE4/5 is 34069298 and the assembly is 34069300. Figure 3-52 is the block diagram of one of the three channels of OE4/5's servo actuator drive.



$W_1 = 1500$ $\zeta_1 = 1$ $g_p = 2.369$ V/V

$W_2 = 5450$

$W_3 = 88$ $\zeta_2 = 0.7$ $g_1 = 2.276$VDC/VRMS

$W_4 = 19630$ $\zeta_3 = 1$ $g_2 = 0.0768$A/V

$g_3 = 1$V/V

$g_4 = -10$V/V (A); -6V/V (B)

SINGLE CHANNEL SERVOACTUATOR DRIVER AND MONITOR FUNCTIONAL DIAGRAM

FIGURE 3-52

3.3.5.4.1 Summing Power Amplifier

The Summing Power Amplifier is a linear current amplifier which drives the servo actuator with a summing network on its input. The summing network sums the filtered output of the RVDT demod with the input command.

3.3.5.4.2 RVDT Pre-Amp

The Pre-amplifier is a true differential amplifier and provides an AC gain of 2.369 V/V to the 2kHz RVDT carrier.

3.3.5.4.3 RVDT Demodulator and Filter

The Demodulator consists of a unity gain inverting amplifier and an analog switch. The switch is driven by a 2kHz square wave and provides the function of multiplying this square wave (considered unity magnitude) with the carrier. The gain of this stage is 0.900 VDC/Vrms.

The filter is a second order low pass filter which separates the DC portion of the demoded signal from the AC.

3.3.5.4.4 Valve Model

The Valve Model is a second order low pass filter which emulates the response of the servo actuator to the input command (D/A output). The output of the model is the idealized proportional response of the servo actuator.

3.3.5.4.5 Monitor Sum Amplifier

The Monitor Sum Amplifier sums the model output signal with the real position signal. Ideally the sum will be zero, indicating zero error in position. The gain of the summing amplifier is pin adjustable in order to provide for tripping the comparator on a 6% difference in return and model signal in channel A and 10% in channel B.

This stage is also used for testing the Limits Comparator. This is accomplished by the injection of a positive or negative signal which will trip the comparators.

3.3.5.4.6 Limit Comparator

The Limit Comparator is a dual comparator stage whose trip points are ±4.5VDC. The output is normally low and goes high when tripped. Each comparator has 0.5VDC of hysterisis. The tripping of the comparator generates a servovalve interrupt to both channels of the controller.

3.3.5.5 Output Electronics No. 6 (OE6)

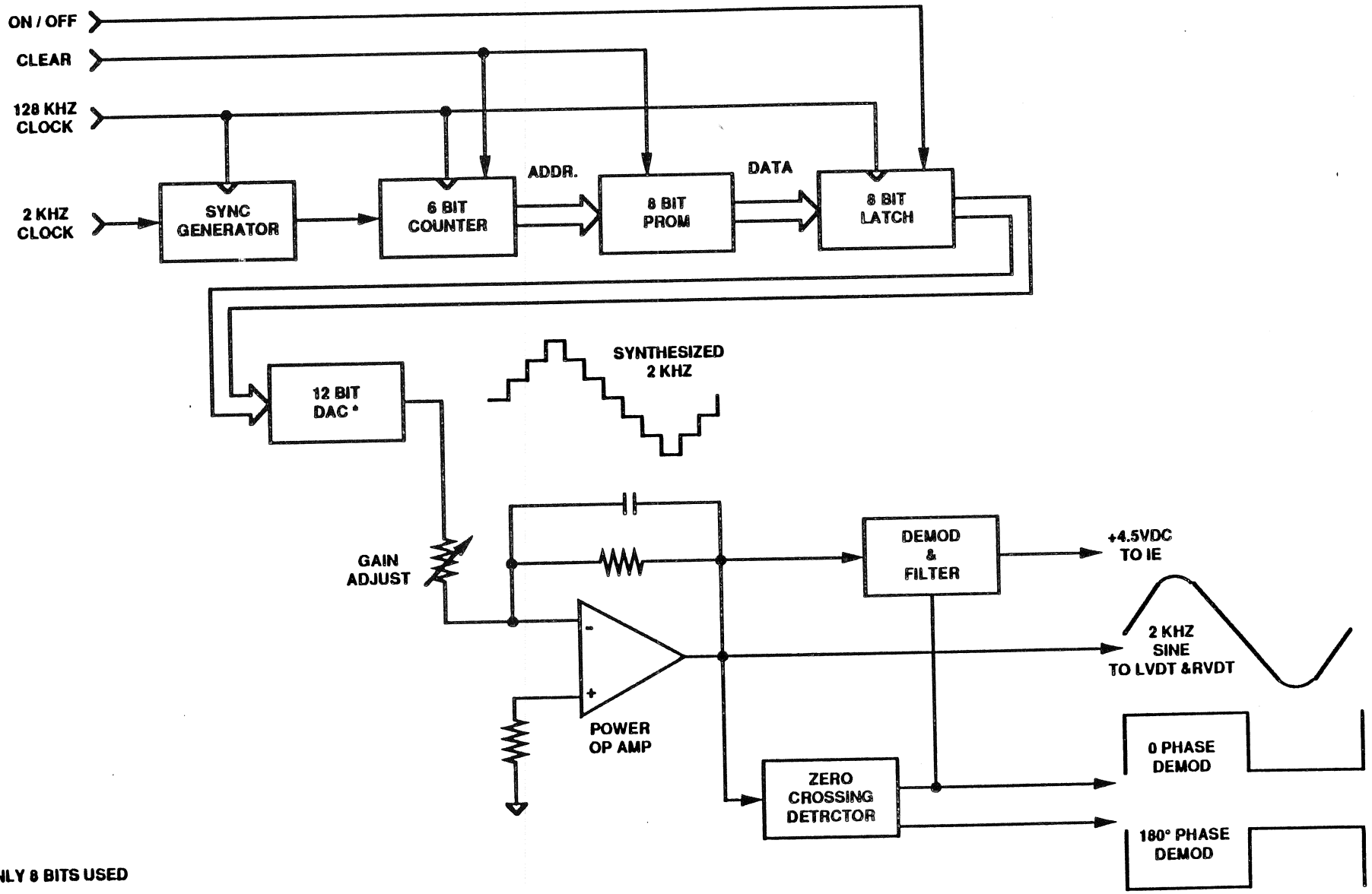
Output Electronics No. 6 (OE6) schematic is 34069301 and the assembly is 34069303. OE6 contains three functions and they are:

- o 2kHz generation - which provides
  - o 2kHz Sinewave
  - o 2kHz Square wave - logic level for carrier demodulation
  - o Two methods of turn off the 2kHz
  - o DC analog B.I.T. signals to IE for monitoring
- o Igniter Driver
  - o Provides signal drive to turn on 3 igniters
  - o Current limiting to the igniters
- o Igniter Monitor
  - o Indicates true when igniter pulses are within normal specification and false when they are not

3.3.5.5.1 2kHz Generator

The 2kHz Generator provides three 2kHz signals. One signal is a 2kHz sinewave with a 7Vrms amplitude which is used for for the 6 in-channel RVDT's and 8 in-channel LVDT's excitation. The other two outputs are 2kHz square waves, one of which is in phase with the 2kHz sinewave and the other is 180° out of phase with the 2kHz sinewave. The two square waves are used to demodulate the in-channel RVDT and LVDT signals. The 2kHz generator also puts out a DC signal that is the demodulated 2kHz sinewave (+4.5VDC nominally).

Figure 3-53 is a diagram of the 2kHz generator. The circuit uses 2 clock frequencies to synthesize a 2kHz wafevorm in the 64 steps. This is done using a counter, a PROM, a latch and a DAC. The counter provides 6-bit addresses to the PROM. These addresses rotate in an endless loop in order to provide 64 discrete addresses to the PROM.



* ONLY 8 BITS USED

2 KHZ GENERATOR

FIGURE 3 - 53

The PROM provides 64 different data words which represent the 64 discrete sinewave levels to be generated. The PROM has been pre-conditioned (blown) prior to installation to set the data words. The PROM outputs are stored in the latch. This latch is clocked at a 128kHz rate. This provides for a constant input to the DAC for 7.8 microseconds. This, in turn, causes the DAC to put out a constant voltage level equivalent to the 8 bit input for 7.8 microseconds. The output of the DAC is sent to the power OP amp where it is filtered and turned into a 2kHz sinewave. This output of the power amp is sent to two zero crossing detectors. These detectors generate the in-phase and 180^{o} out of phase demodulation square waves. The demod and filter is part of the B.I.T. circuitry on the 2kHz generator.

The ON/OFF control of the 2kHz is done using two separate inputs. The first is the clear line which clears the counter and sets the PROM address to 40_H. This address select is data that results in zero output from the DAC. The second ON/OFF control is done by clearing the 8-Bit Latch to 80_H which again results in zero output from the DAC. Actually, the DAC input for this condition is 800_H because it is a 12-bit DAC. The true output for this input is 1 LSB (4.9 millivolts DC), but is considered zero output since it represents a trivial offset current to the sinewave output.

The method by which this second ON/OFF signal is generated is not shown in Figure 1. There is a decoding involved. There is a bit (word 2 bit 8) in the OE1 ON/OFF Register which is used for software control of the 2kHz. The bit is cross-connected between the two OEs. The decoding is done by a 4-to-1 digital multiplexer using the following truth table:

2kHz Control

A Bit	B Bit	2kHz A	2kHz B	Clock Source
1	1	OFF	OFF	None
0	1	ON	ON	A
1	0	ON	ON	B
0	0	OFF	ON	B

3.3.5.5.2 Igniter Driver

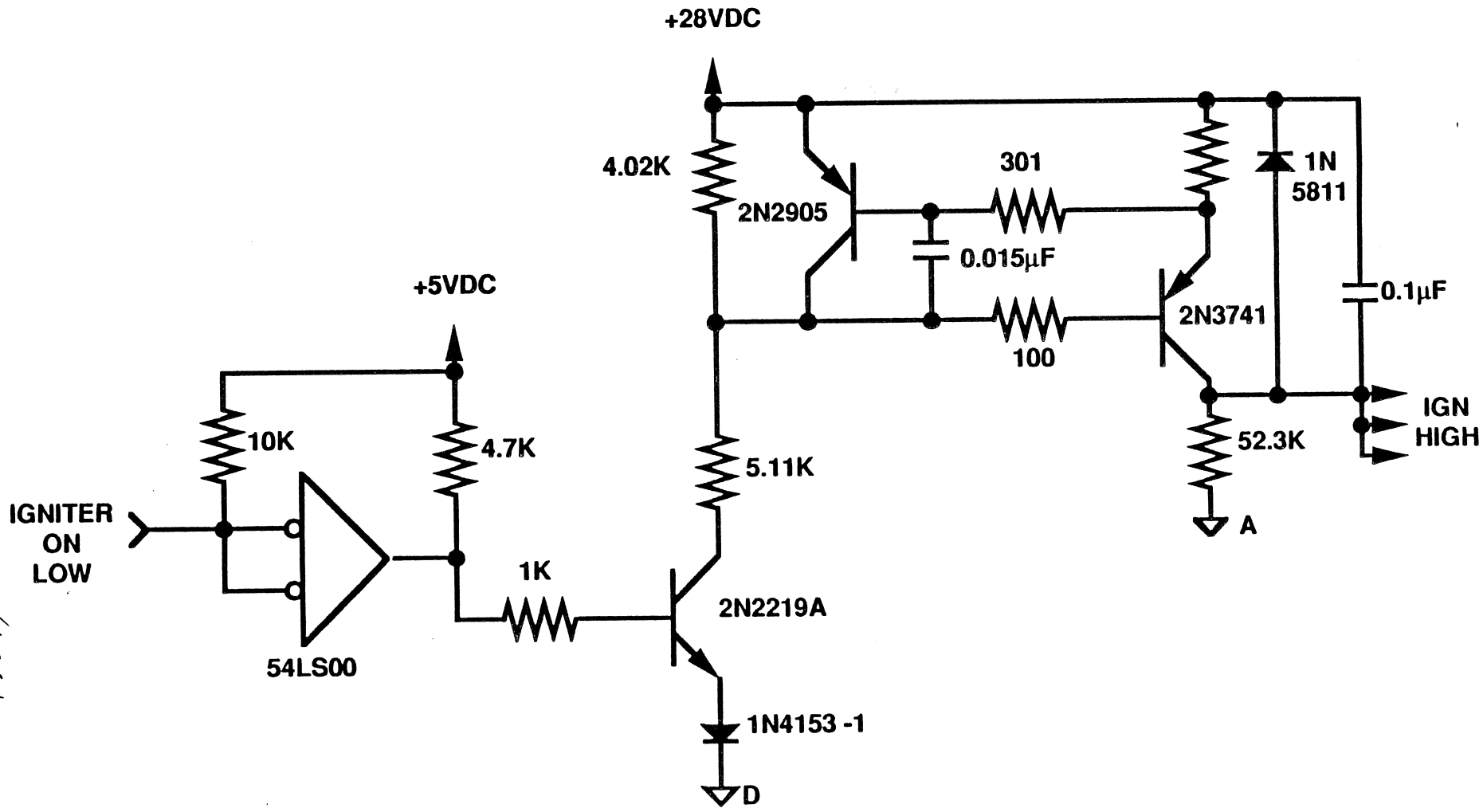
The Igniter Driver provides +26 VDC command signals to the Igniters. It does this in response to an ON/OFF logic level signal. The driver stage contains a current limiter to protect against overload. Figure 3-54 is a schematic of the Igniter Driver. The Igniter Driver circuit is the driver for the ignition on command that comes from the ON/OFF Register on OE1. The one driver circuit controls all three igniters (main chamber, oxidizer preburner, fuel preburner) in the engine system. The driver is controlled by a logic level signal and delivers 26V limited to 0.049 amps nominally.

3.3.5.5.3 Igniter Monitor

The assembly contains three identical Igniter Monitor circuits. One for each Igniter in the engine. Each circuit receives pulses from the Igniter Power Supply. The monitor verifies that the pulses are of proper magnitude and frequency and reports with a logic level signal when both conditions are proper.

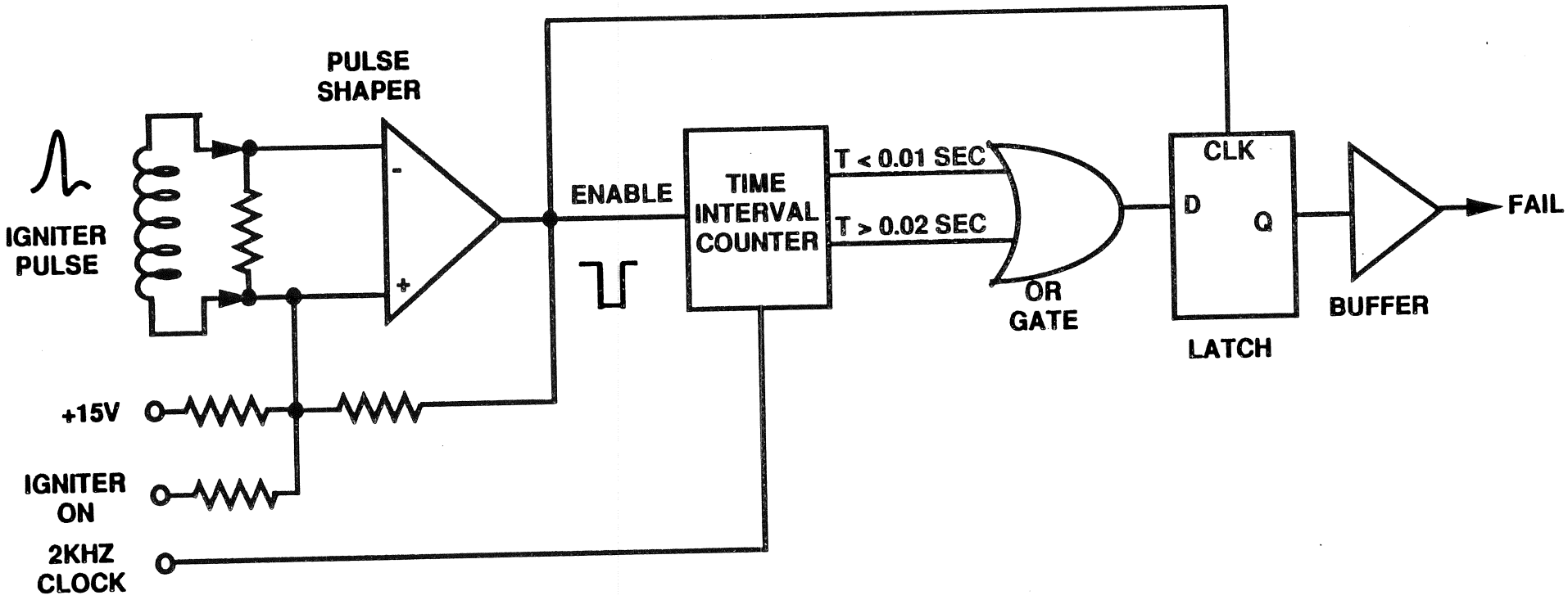
The Igniter Monitor is shown functionally in Figure 3-55. The circuit receives pulses from one of the three Igniter Power Supplies. The supply contains an oscillator which is used in the process of generating the high voltage used to fire a spark gap. The input pulse amplitude is indicative of the voltage amplitude and the pulse rate is indicative of the oscillator frequency.

The circuit input stage has a 2.4-volt threshold. If the pulse amplitude exceeds this level the stage (a comparator with hysterisis) will trip and the output will be a reshaped pulse at logic levels. This pulse will be used to gate the counter. The counter counts 2kHz cycles. It will indicate if the number of cycles between consecutive pulses is less than 50 or greater than 100. If either of the failure conditions exist, then the fail indication is set.



IGNITER DRIVER

FIGURE 3- 54



IGNITER MONITOR BLOCK DIAGRAM

FIGURE 3 - 55

3.3.6 POWER SUPPLY ELECTRONICS

The Power Supply Electronics function is two-fold. First and foremost, the Power Supply Electronics converts the vehicle-supplied electrical power to the individual voltages required to power the SSMEC Block II electronics. The second function is to supply the controller electronics with control signals that can be used to assure an orderly startup and shutdown of the controller.

The Power Supply Electronics receives its primary power as 3-phase 400Hz 115VAC power with +28VDC as a backup for selected special functions.

The voltage outputs per channel of the Power Supply Electronics are:

	Input Source	
Function	AC	DC
Processor +5V :	+5VDC ±5% @ 2.1A	+5VDC ±5% @ 2.1A
Logic +5V :	+5VDC ±10% @ 16.9A	
Memory +5V :	+5VDC ±10% @ 2.26A	+5VDC ±10% @ 2.26A
+15V :	+15VDC ±3% @ 1.25A	
-15V :	-15VDC ±3% @ 1.25A	
+15V (C) :	+15VDC ±3% @ 0.039A	
-15V (C) :	-15VDC ±3% @ 0.062A	
+5V (C) :	+5VDC ±10% @ 0.69A	
Servoswitch/		
Igniter 26V :	+26V ±2VDC @ 2.5A	
Solenoid Hold A:	+16VDC +16%/-20% @7.21A	
Solenoid Hold B:	+8VDC +16%/-20% @4.82A	
Solenoid Pull A:	+29VDC +16%/-20% @8.35A	
Solenoid Pull B:	+24VDC +16%/-20% @8.35A	
P/S Control		
Voltage A :	+39VDC +16%/-20% @0.063A	
P/S Control		
Voltage B :	+34VDC +16%/-20% @0.055A	

Any given channel (A or B) only supplies the Solenoid Pull, Solenoid Hold and the P/S Control Voltage defined for that channel. Channel A and channel B power supplies are different on these three voltages.

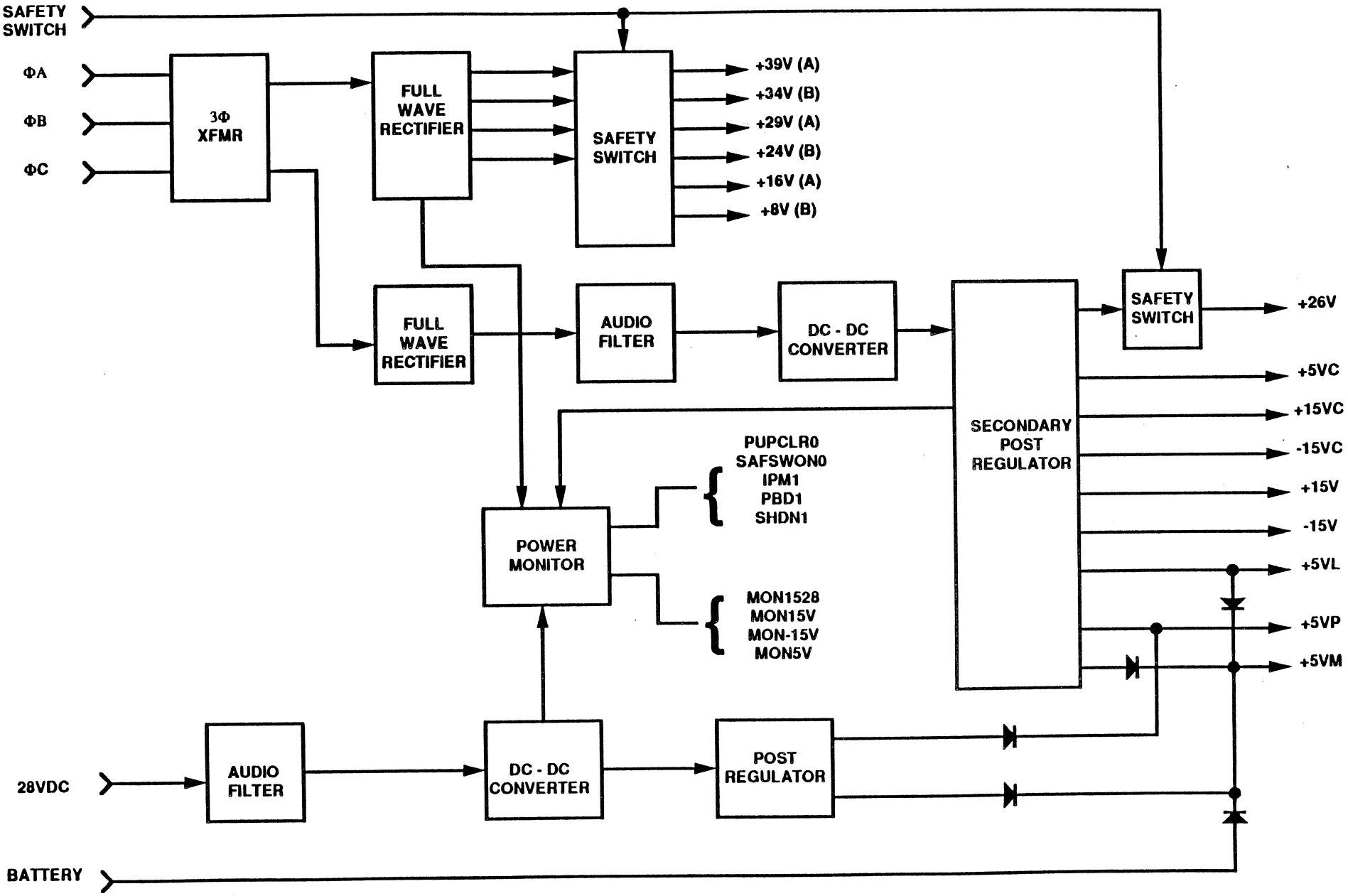
In addition to the above listed voltages the Power Supply Electronics shall also provide:

- Safety switches on +39V, +34V, +29V, +24V, +16V, +8V and +26V outputs
- Current limiting and short circuit protection on all outputs
- EMI protection per MIL-STD-461 as modified by SL-E-002
- Memory, FDR and processor hold-up from +28VDC for 115VAC failure
- Memory and FDR back-up from battery for loss of 115VAC and 28VDC
- Hold-up of regulated outputs for 100 microsec while powering down
- Overvoltage protection for 5VDC outputs
- Hot spot temperature sensor
- Input/output power isolation
- Secondary voltage monitoring
- Sequencing of control signals

Figure 3-56 is a block diagram of the Power Supply Electronics. The schematic is 34069312 for channel A and 34069313 for channel B. The power supply assembly is 34070361. Although located in the main chassis, one other assembly should be considered a part of the Power Supply Electronics and that is the Voltage Monitor Assembly (VMI). The VMI schematic is 34076190 and the assembly is 34076192.

The Power Supply Electronics is composed of five major functional areas packaged on ten printed wiring assemblies per channel. The functional areas are:

- Input Transformer Assembly
- Pulse Width Modulator and Filter Assembly
- Post Regulators
- DC Hold-up Supply
- Power Supply Monitor



POWER SYSTEM BLOCK DIAGRAM

FIGURE 3- 56

3.3.6.1 Input Transformer Function

The Input Transformer Assembly consists of:

- o Dog House Filter
- o 3-Phase Power Transformer
- o Power Safety Switch
- o O.E. Voltage Rectifiers
- o Monitor Voltage Rectifiers
- o In Rush Current Limiter and 28VDC Rectifier
- o Temperature Sensor (telemetry)

Figure 3-57 is the block diagram of the Input Transformer. In this block diagram the Dog House Filter contains the 3- phase 400 Hz EMI filter elements and Transorbs for input voltage spike protection. The 3-phase transformer is a gapped "E" core transformer for in rush current control, designed for 550 watts max. power capability. The transformer has a multi-voltage tapped output. The rectifier/filter assemblies take the AC voltage from the secondary of the transformer and converts them to the solenoid voltages, the monitor operating voltages and the 28V for the DC/DC converter. The power safety switch is a 3-pole switch that is in series with the output voltages for the solenoid drivers. This switch is used to cut these voltages off when the Watch Dog Timer times out or an O.E. voltage fails. The switch is driven by a signal from OE1. The 28VDC rectifier output feeds to the in rush current limiter which adds series resistance to the 28V line to the DC to DC converter which limits the rate of change of the input curr Once the input filters are charged the series resistor is shunted out by th FETs in the current limiter.

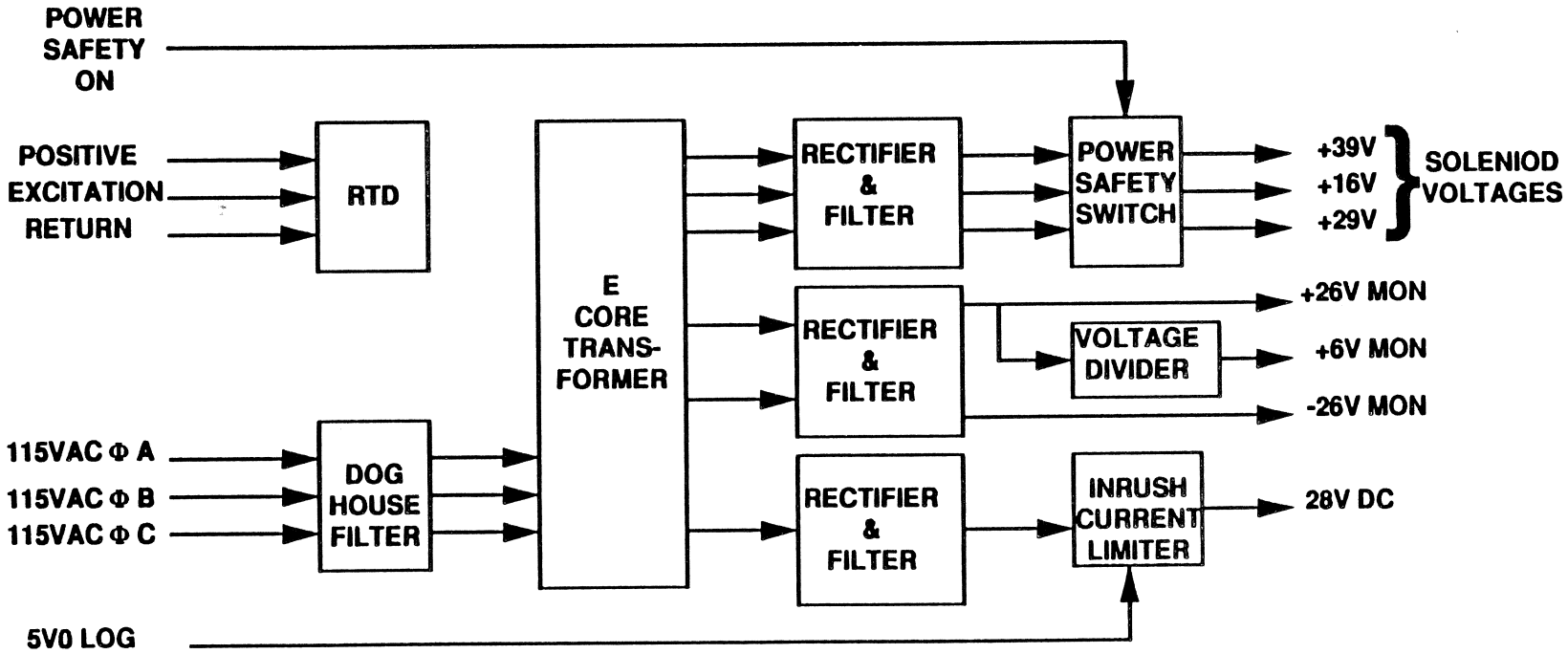
The last function in the input transformer assembly to discuss is the temperature sensor that monitors the temperature of the assembly. The temperature sensor is a 100-ohm RTD that is wired to the outside world and read by the spacecraft telemetry system. It represents one of the hottest spots in the controller.

3.3.6.2 Pulse Width Modulator and FIlter Assembly

The Pulse Width Modulator (PWM) and Filter are made up of three sub-functions:

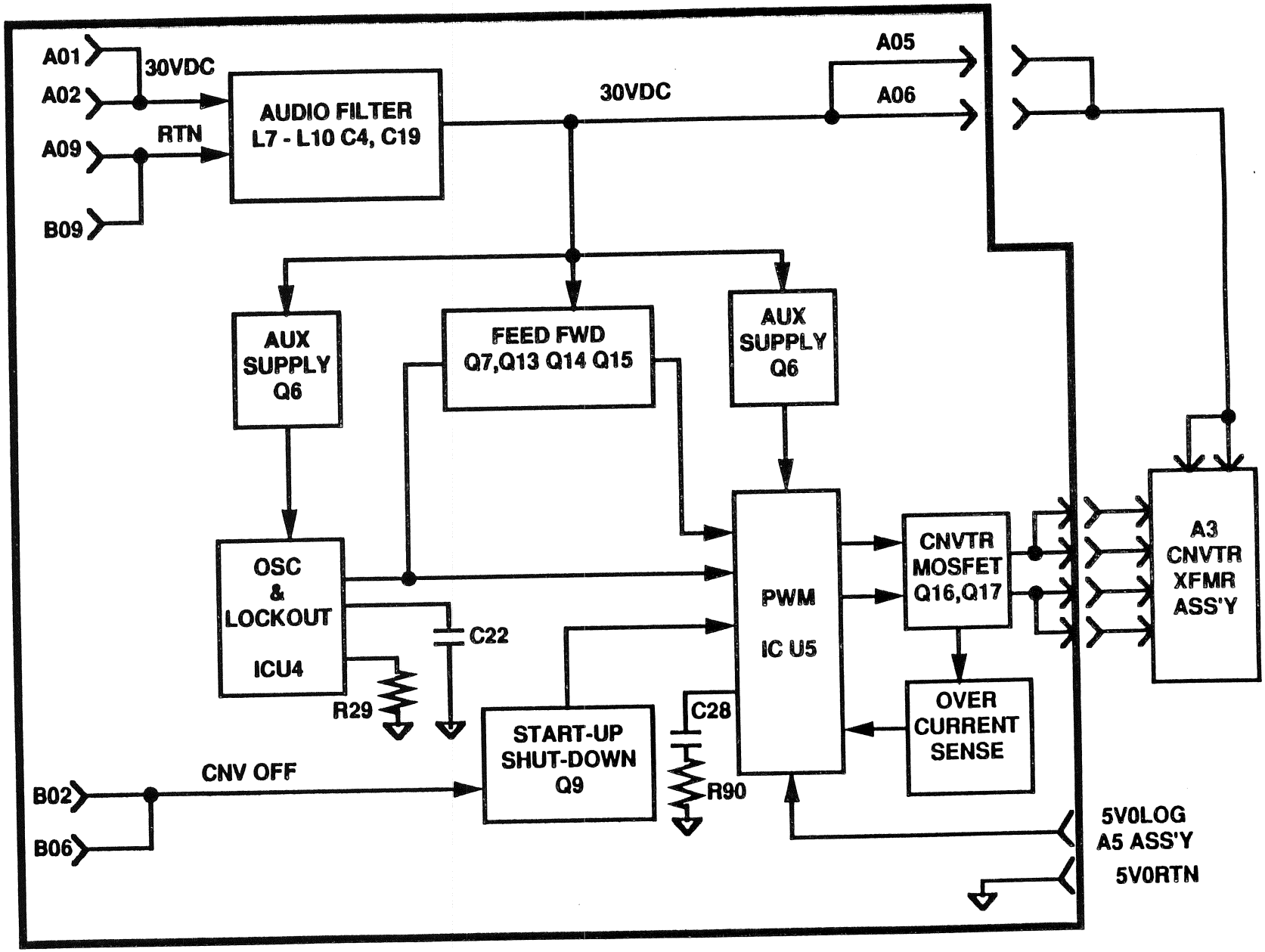
- o The Audio Filter
- o The Pulse Width Modulator and DC/DC Transformer
- o The Rectifier and Post Regulator Circuits

Figure 3-58 is the PWM block diagram.



INPUT TRANSFORMER ASS'Y

FIGURE 3-57



PULSE WIDTH MODULATOR & FILTER ASS'Y

3.3.6.2.1 Audio Filter

The Audio Filter is a multi-stage LC filter that is designed to prevent audio noise from entering or exiting the power supply. A secondary function is to provide a source of energy to maintain the controller voltages for 100 microseconds after the AC voltage has been turned off. The normal 30.0VDC output of the Audio Filter feeds to the PWM and the DC-DC transformer.

3.3.6.2.2 Pulse Width Modulator

The 30VDC from the Audio Filter is routed to a voltage supply for the oscillator and lockout circuit, a voltage supply for the Pulse Width Modulator Circuit, and the Feed Forward Circuit. The oscillator and lockout circuit establishes the frequency of the PWM at 25kHz and turns the PWM off anytime the 30VDC goes below 20VDC. The PWM circuit adjusts the ON time of the two converter MOSFETs in propoprtion to the input voltage amplitude in order to maintain a constant voltage out of the DC-DC transformer. The system +5V0LOG is used for feedback control from the outputs from the power supply. The overcurrent sensor reduces the pulse width out of the supply when an overcurrent condition is sensed. The startup, shutdown circuit turns the PWM circuit on or off based on a signal from the Power Supply Monitor Circuit.

3.3.6.2.3 DC-DC Transformer

The DC-DC Transformer is a toroidal transformer with a center-tapped primary and a multi-tapped secondary. The transformer is driven by the 30VDC from the audio filter switched by two MOSFETs from the PWM.

3.3.6.2.4 The Rectifiers and Filters

Coming off the secondary of the DC-DC Transformer are seven center tapped windings. Each winding goes to a full wave rectifier and all but one go to post regulators. The one winding that does not go to a regulator is the 5VDC logic voltage. This voltage is fed back to the PWM to regulate the overall DC-DC Transformer output. The seven voltages from these rectifiers and filters are: 8.9VDC, +19.5VDC, -19.5VDC, +34VDC, -34VDC, +5.0VDC and 34VDC.

3.3.6.2.5 Post Regulators

Six of the output voltages from rectifiers and filters go to post regulators for further regulation. Figure 3-59 is a block diagram of how the post regulators are arranged. From the diagram it can be seen that the +26VDC not only has a post regulator, it also has a power safety switch in series with the regulator. It can also be noted that one set of ±15V regulators is set up for in-channel use while another set of ±15V regulators has series diodes in the regulators' outputs in order that they be diode "OR"ed to form channel C ±15V.

From the diagram it can be seen that there are four +5V post regulators. The +5V0LOGC regulator has a diode in series with its output so that it may be diode or'ed to form channel C +5VDC. Because the processor has a +5VDC ±5% specification on its Vcc, the processor +5V has a 5% regulator.

Additionally, in order to survive the power transients, a +5V regulator powered from a +28VDC source is diode or'ed with the processor +5VDC and the memory +5VDC. The memory requires the back-up because the main memory is RAM.

From the diagram it can be seen that the memory +5V is tied to the logic +5V through a diode. This very high current diode is there to pull down the logic +5VDC if there is a short on +5V0MEM. This is done to prevent destroying the RAMs which cannot have their input pins, which are driven from +5V0LOG, exceed the RAMs Vcc (+5V0MEM) by greater than 1.0VDC.

3.3.6.4 28V Hold-Up Supply

The 28V hold-up supply is used to supply back-up power to the processor +5V and the memory +5V. Figure 3-60 is a block diagram of the 28V hold-up supply. The +28V hold-up supply is composed of three functions.

- o Converter Oscillator - Transformer
- o Converter Disable
- o Rectifiers

POST REGULATORS

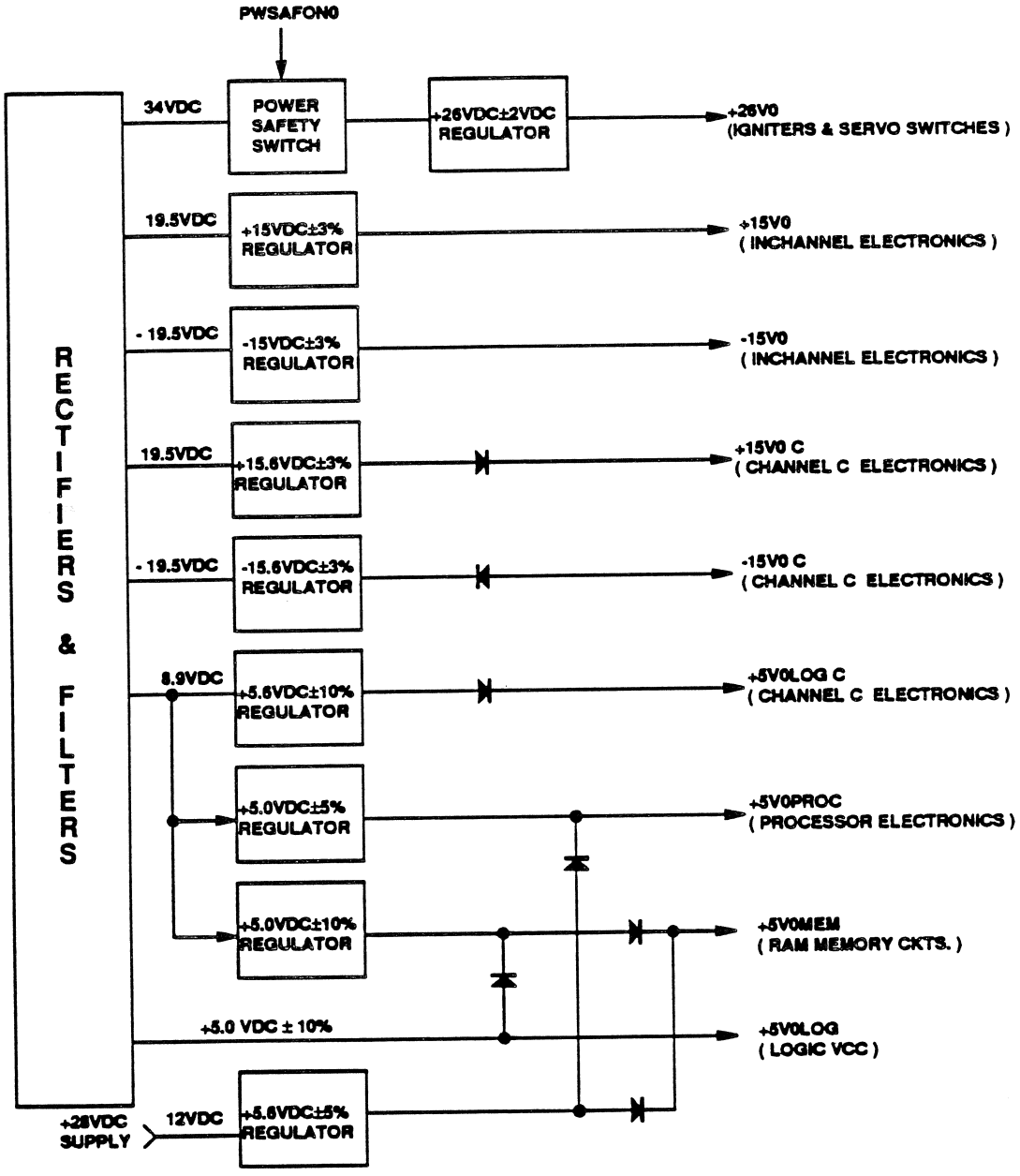
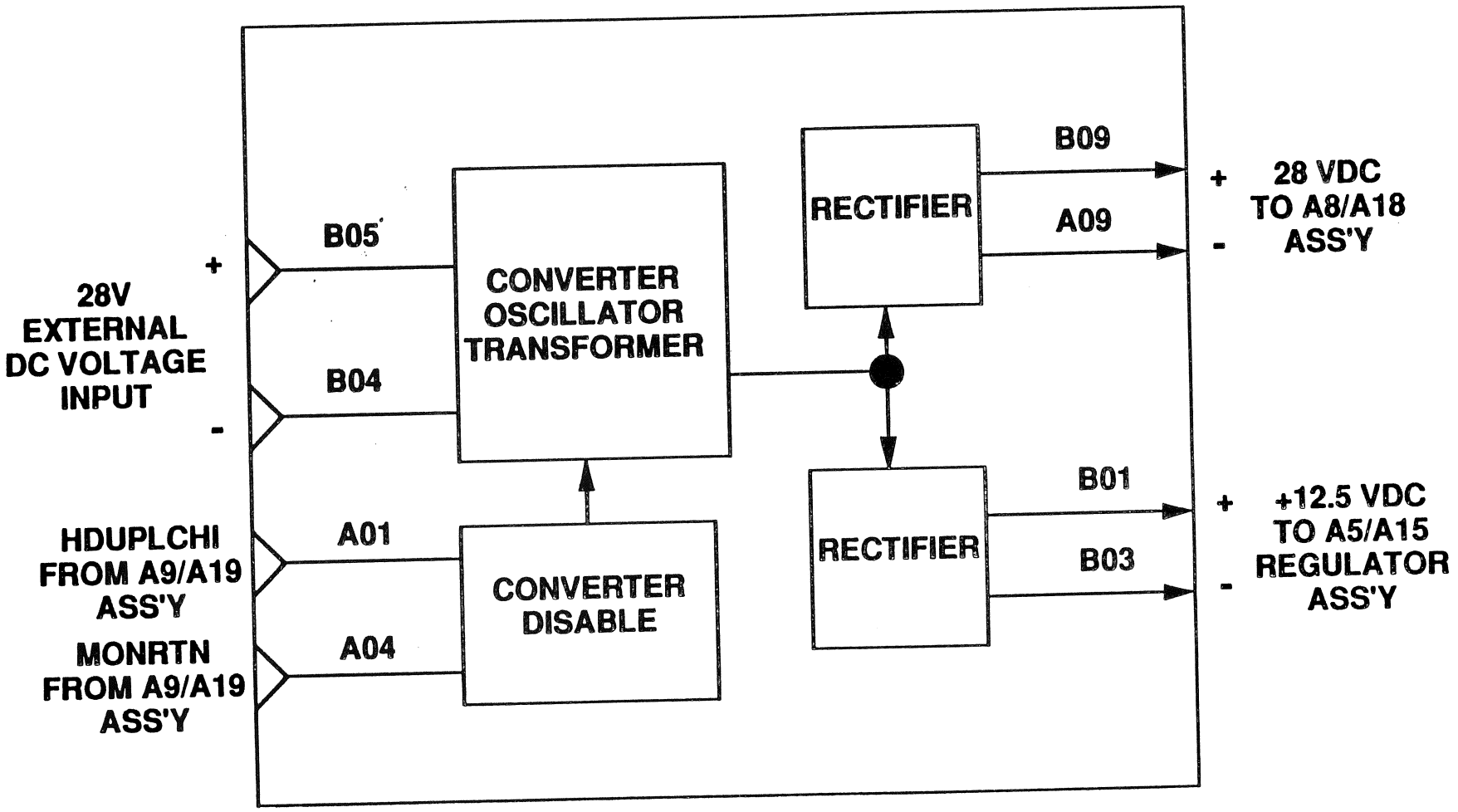


FIGURE 3 - 59



PROCESSOR/MEMORY HOLDUP SUPPLY

FIGURE 3 - 60

3.3.6.4.1 Converter Oscillator - Transformer

The transformer in the +28V hold-up supply provides isolation of the +28VDC from the controller electronics and positive feedback to the oscillator on the primary side of the transformer. The oscillator drives two transistors that are connected to the ends of the center-tapped transformers primary. The center tap is connected to the +28VDC input HI-side. The secondary of the transformer in addition to the feedback has two center-tapped windings that drive full wave rectifiers.

3.3.6.4.2 Rectifier

There are two full wave rectifiers connected to the transformer secondary and they supply +12VDC to the +5V regulator for the memory and processor in Figure 3.3-58 and +28VDC for use in the power monitor circuitry.

3.3.6.4.3 Converter Disable

The converter disable shuts down the back-up supply whenever the +5 volts to the memory or processor +5 volts goes too high. The converter is shut down by HDUPLCHI which comes from the power supply monitor +5 volts overvoltage protection circuit.

3.3.6.5 Power Supply Monitor

The power supply monitor can be broken up into two areas: the inboard chassis and the main chassis area. The inboard chassis monitors deal primarily with the incoming voltages and current and the operation of the power supply electronics, while the main chassis electronics deals primarily with the proper sequencing on and off of the controller electronics.

3.3.6.5.1 Inboard Chassis Monitor

Figure 3.3-61 is a block diagram of the inboard chassis power monitor electronics.

3.3.6.5.1.1 AC Bus Filter and IPM Filter

The AC bus filter is a passive LC filter that is powered by the MON6V rectifier on the input transformer assembly. The filter has a divider network output that provides 5.9VDC and 2.5VDC. The 5.9VDC goes to the greater than 130VAC (GT130) and less than 95VAC (LT95) comparators. The 2.5VDC goes to an active filter (IPM) to further smooth the signal. The output of the IPM filter is sent to IE3 for monitoring and to the greater than 120VAC (GT120) comparator.

INBOARD CHASSIS POWER MONITOR

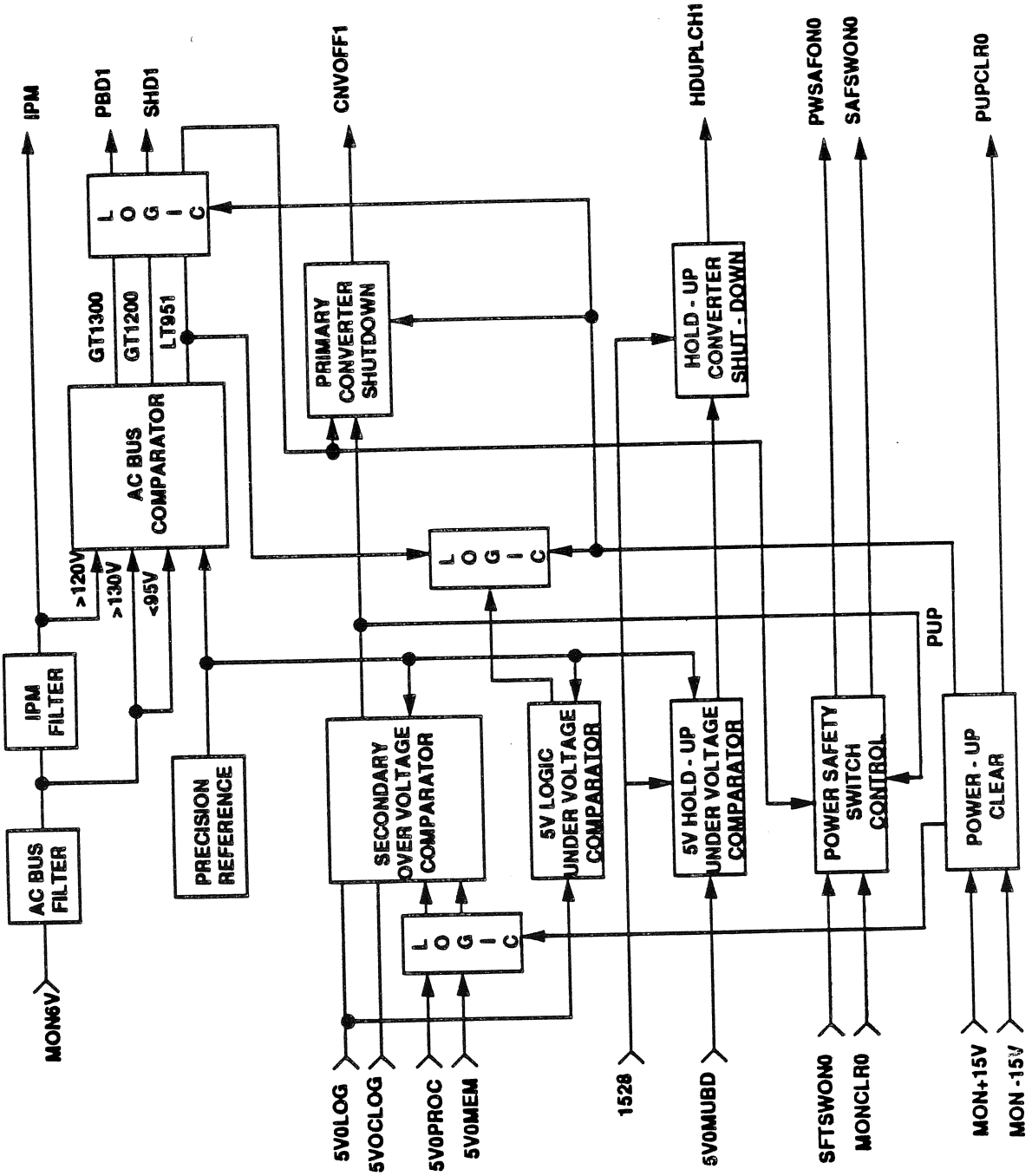


FIGURE 3 - 61

3.3.6.5.1.2 Precision Reference

The precision reference provides a precision +10VDC signal to all of the comparators in the inboard monitor circuit. The supply is powered by either MON1528 or MON15V.

3.3.6.5.1.3 AC Bus Comparators

Three comparators are used to trip at 130VAC, 120VAC and 95V truncated sine wave. The 130VAC comparator has 11.4VAC hysteresis, the 95V comparator has 17.8VAC hysteresis and the 120VAC comparator has 1.6VAC hysteresis. Hysteresis was reduced on the 120VAC comparator due to the additional filtering of the IPM filter. A transistor inverter is used on the negative going 95V comparator input.

3.3.6.5.1.4 Secondary Overvoltage Comparator

Four secondary supplies are monitored for overvoltage, +5V0LOG, +5V0CBD (before OR'ing diode) +5V0PROC and +5V0MEMBD (before OR'ing diode). Steady state trip level is set by R22, R23, and R24 to 5.92V. Hysteresis is 1.9 volts (2.1V for +5V0CBD and +5V0MEMBD).

3.3.6.5.1.5 +5V0LOG Undervoltage Comparator

This comparator, U5-1, trips (sends a true LOW signal) when the +5V0LOG drops to +4.0VDC. Hysteresis is 50mv. After the AC bus (primary) converter has started, if the +5V0LOG drops below 4.0V the converter is shut down. During initial power-up, 5V0LUV0 is disabled.

3.3.6.5.1.6 5V Hold-up Overvoltage Comparator

The comparator for the +5V hold-up supply overvoltage protection is powered by the hold-up +28VDC. The reference for this comparator is the 10V reference since it is also powered by a voltage derived from +28VDC. The 5V hold-up overvoltage comparator shuts down the hold-up DC-DC converter when the hold-up +5V exceeds +5.9VDC.

3.3.6.5.1.7 Hold-up Converter Shutdown

The hold-up converter shutdown circuit applies +15VDC to the optical coupler on the hold-up DC to DC converter through a 499 ohm resistor.

3.3.6.5.1.8 AC Bus Logic

If the AC bus exceeds 120VAC (but not 130VAC) for more than 20msec, or if it exceeds 130VAC, PBD1 and SHDN1 are are issued and the converter is turned off. Either overvoltage signal true also turns off the Power Safety Switch.

When the AC Bus drops below 100V truncated sinewave, PBD1 is issued for 100 microseconds (min). On the falling edge of PDB1, SHDN1 is issued shutting down the converter if the AC stays down. If the AC bus does not stay down for more than 100 microseconds the SHDN1 signal is not issued and the converter is not shut down.

3.3.6.5.1.9 Primary Converter Shutdown (CNV0FF1)

The converter is shut down by: (1) an AC bus or secondary regulator overvoltage; (2) 100 microseconds after an AC bus undervoltage, or (3) a 5V logic (5V0LUV0) undervoltage.

3.3.6.5.1.10 Power Safety Switch Control

The power safety switch control signal PWSAFON0 is true low and is normallly turned on by SFTSWON0 a logic signal from OE1. It is turned off by SFTSWON0 false, MONCLR0, an AC bus overvoltage, or a secondary supply overvoltage.
This circuit is designed to be glitch free during system power-up or pow down.

3.3.6.5.1.11 Power-Up Clear

This circuit sets all monitor flip-flops, one-shots, and start-up/shutdown logic gates to the required state. During power-up it stays LOW up to 5.7msec after initial power application. During AC bus shutdown, it goes LOW as soon as MON+5V starts to decay, holding all logic in the proper state. An internal signal, PUPDRV, turns off shorting JFETS in the secondary overvoltage and converter shutdown circuits when PUPCLR is HIGH, but turns them ON when PUPCLR is LOW or unpowered.

3.3.6.5.2 Voltage Monitor Assembly (VMI)

The VMI assembly is the main chassis portion of the power supply monitor. The VMI schematic is 34076190 and its assembly number is 34076192. The VMI assembly deals primarily with the generation of signals required to properly turn power on and off the rest of the controller electronics, in particular the processor and memory. The voltage monitor assembly (VMI) is powered from the inboard chassis MON+5VDC and MON+15VDC which come on ahead of the normal +5VDC and +15VDC and hold up longer because of their light load. Figure 3-62 is a block diagram of VMI.

3.3.6.5.2.1 +10VDC Precision Reference Supply

This circuit provides the precision voltage that is used as a reference by the voltage monitors. The output is set by adjustment during calibration.

3.3.6.5.2.2 Operating Voltage Monitor

This circuit performs the function of monitoring the 5 primary voltages used in the controller and indicates if they have reached proper levels during initial turn-on or turn-on after a power interruption. This circuit is composed of 5 comparators.

3.3.6.5.2.3 Input Signals

The input signals to the voltage monitor assembly are:

- o +5V0LOG - the +5VDC to all of the logic circuitry
- o +5V0MEM - The +5VDC to the main memory and FDR
- o +5V0PROC - The +5VDC to the 68000 mircoprocessor
- o +15V0 - Controller +15VDC
- o -15V0 - Controller -15VDC
- o PBD1 - Power Bus Down from the Power Supply Power Monitor circuitry located in the Power Supply Cavity
- o PUPCLR0 - Power-up Clear signal for all Power Monitor logic circuits from the Power Supply Cavity. This signal is held LOW initially to allow for settling
- o SHDN1 - Shutdown is generated in the Power Supply Cavity 100 usec after PBD1 goes HIGH unless PBD1 returns LOW
- o 28OK1 - 28V Hold-Up Power OK from the Power Off Indicator on card OE1
- o GSECLR0 - Ground Support generated CLEAR signal

VM1 VOLTAGE MONITOR BLOCK DIAGRAM

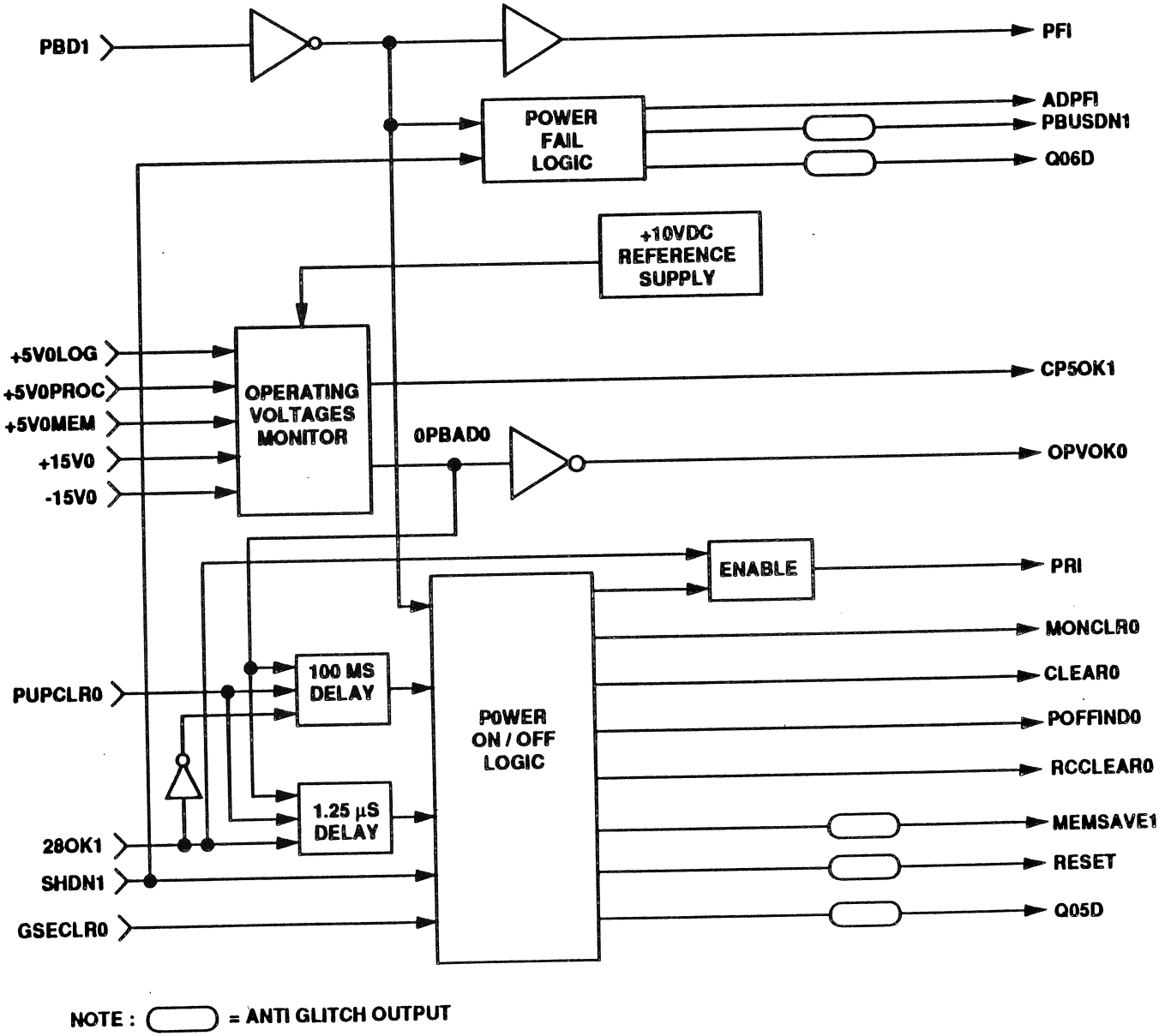


FIGURE 3- 62

3.3.6.5.2.3 Initial Power-Up Sequence

During initial Power-Up PUPCLR0 is momentarily LOW allowing the Power Monitor to stabilize. All flip-flops, one shots, deglitch FETS and logic output states are set to their desired state. 28OK1 is LOW as are PBD1 and SHDN1. When all monitored power supplies are above their minimum tolerance, OPVBAD0 goes HIGH starting both the 1.25-microsecond delay and the 100-millisecond delay. 28OK1 is LOW so the 100-millisecond delay is enabled. After a 100-millisecond delay:

- o MEMSAVE1 goes to 0 - enabling the memory
- o MONCLR0 and CLEAR0 go to 1 - enabling a logic
- o RESET0 goes to 1 375ns later - enabling the processor
- o PRI0 which is normally generated by RESET0 going to 1 is blocked by 280K1 being 0. This causes the processor to remain in the RAM mode until a valid VEEI

  command is received.
- o The power On/Off logic is also set-up to detect a power down.

3.3.6.5.2.4 Power Down (28-volt DC Off)

When the 3-phase 400Hz 115VAC input to the contgroller goes below 95VAC, the inboard chassis monitor causes PBD1 to go to the 1 state. PBD1 true is inverted and sent to the in-channel CIE as the power failure interrupt PFI0. PBD1 also goes to the power failure logic to generate the cross channel signals ADPFI1 and PBUSDN1. ADPFI1 and PBUSD1 are signals that have anti-glitch circuitry.

100 useconds after PBD1 goes true SHDN1 will go true if the 115VAC has not returned above 108VAC. SHDN1 true generates CLEAR0, RESET0 and MEMSAVE1 in the power on/off logic. Should the 3-phase bus have an interruption and recover in less than 100us, SHDN1 will not be received but PBD1 will be received and PFI0 will have been asserted.

The PFI0, ADPFI1 and PBUSDN1 cannot be negated unless the MONCLR0 and CLEAR0 signals are asserted. To assert these signals without a SHDN1 signal the power On/Off logic contains a one shot that is triggered by PBD1 going false (bus exceed 108VAC) and PUPCLR0 being false. The one shot causes the power on/off logic to generate a 1.25- microsecond MONCLR0, CLEAR0, RESET0 and MEMSAVE1. These 1.25-microsecond pulses clear PFI0, ADPFI1 and PBUSDN1. They also generate a PRI0 (power recovery) at the end of the reset pulse, but the PRI0 is blocked by the Enable because 28OK1 is not true.

3.3.6.5.2.5 Power Bus Down (28 Volts On)

If PBD1 goes HIGH (indicating loss of prime power) a power failure interrupt (PFI0) is sent to the processor. The processor initiates the shutdown routine. If the back-up power source is up and the prime power bus stays down for approximately 100 microseconds, then the normal power down sequence is completed and 28OK1 is set high. The voltages to the voltage monitor portion of VMI go down soon after the prime bus goes down. This set OPVOK0 HIGH and the complement (OPVBAD0) LOW. ADPFI1, PFI0, PBUSDN1, and RESET0 are asserted along with MONCLR0 and CLEAR0.

3.3.6.5.2.6 Power Recovery (28VDC On)

During initial Power-Up PUPCLR0 is momentarily LOW allowing the Power Monitor to stabilize. All flip-flops, one shots, de-glitch FETS and logic output states are set to their desired state. PBD1 and SHDN1 are low. When all monitored power supplies are above their minimum tolerance, OPVBAD0 goes HIGH starting both the 1.25 us delay and the 100 millisecond delay. With 28OK1 asserted, because +28V has been on during the entire time the AC was off, the 1.25-microsecond delay will be enabled. At the end of the 1.25-microsecond delay:

- o MEMSAVE1 is negated.
- o MONCLR0 and CLEAR0 are negated.
- o RESET0 is negated 375 nanoseconds after CLEAR0 negation.
- o PRI0 is asserted at the end of RESET0 and enabled to the processor because 28OK1 is asserted.

The controller must have been on at least one time for 28OK1 to be asserted. With the PRI0 interrupt enabled the controller will resume processing where it left off for the PFI interrupt.

3.3.6.5.2.7 Overvoltage Shutdown

Any time any of the AC overvoltage conditions or the +5-volt DC overvoltage conditions are met PBD1 and SHDN1 will be generated simultaneously, and the DC/DC converter will be shut down. This does not allow an orderly shutdown of the system and the system should always come on operating out of RAM memory.

3.3.6.5.2.8 GSECLR0

This function allows Ground Equipment to CLEAR the controller logic, normally for testing purposes.

3.3.6.5.2.9 Output Signals

Output signals are:

PFI0(P1B42) - Power Failure Interrupt

ADPFI1(P1C23) - Alternate Digital Processor Power Failure Interrupt is latched by the cross channel CIE.

PBUSDN1(P1C24) - Cross Channel Power Bus Down Interrupt is monitored by software in real time (cannot glitch).

MEMSAVE1(P1C36) - Memory Save (Protect) inhibits memory operation when high. Enables memory written when low.

RESET0(P1B45) - Used by the processor to synchronize the dual pair processor. Cannot glitch.

PRI0(P1C34) - Power Recovery Interrupt - a 375ns (minimum) pulse indicating that the power bus has recovered from a transient and that hold-up power stayed good.

POFFIND0(P1C22) - This is a monitor signal primarily used in testing the Power Off Indicator (POI).

MONCLR0(P1B43) - This is a System Clear signal used by the Power Supply Monitor circuitry. It is used to control the Power Safety Switch.

CLEAR0(P1B44) System Clear signal that forces all register, flip-flops and other logic elements in the "Clear" state at power down.

OPVOK0(P1B41) - Operating Voltage OK, primarily a logic monitor signal indicating +5V0LOG, +5V0PROC, +5V0MEM, +15V0 and -15V0 are all above their minimum tolerance.